TeraPixel APS for CALICE

Progress meeting 9th Dec 2005

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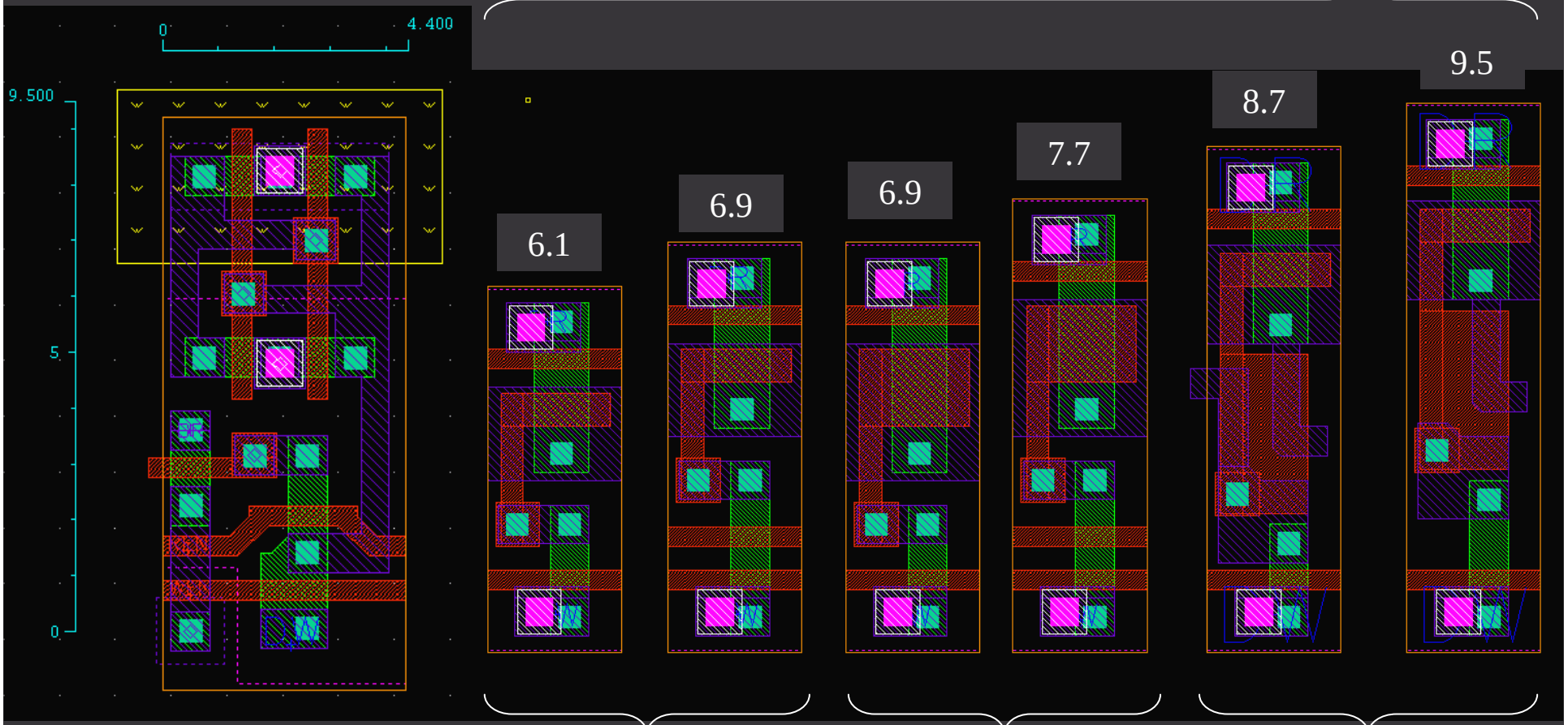
SRAM vs DRAM



SRAM

DRAMs

SIMPLE (~OPIC)

DRAMs

LONGER GATE

DRAMs

CPOD CAP

DRAM lifetime simulations

Process corners: Typical, worst-power (wp), worst-speed (ws)

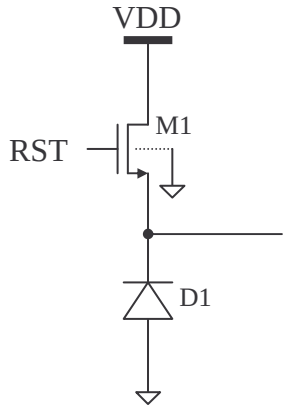
	SIMPLE	SIMPLE+2 W	LONG	LONG+2W	CPOD	CPOD+2W
Lifetime (typ)	2.5 ms	5.5 ms	4.5 ms	9.7 ms	5.2 ms	11.2 ms
Lifetime (wp)	0.2 ms	1.8 ms	0.38 ms	3.3 ms	0.4 ms	3.4 ms
Lifetime (ws)	2.4 ms	4.8 ms	4.0 ms	8.1 ms	5.2 ms	10.4 ms

Applying negative 'off' bias to reduce leakage further:

	SIMPLE	SIMPLE+2 W	LONG	LONG+2W	CPOD	CPOD+2W
Lifetime (typ)	2.8	5.6	5.1	10.1	5.9	11.7
Lifetime (wp)	3.4	6.7	6.5	12.8	6.7	13.3
Lifetime (ws)	2.3	4.5	4.0	7.8	5.2	10.24

(Excel sheet:pitch-size-noise-lifetime.xls)

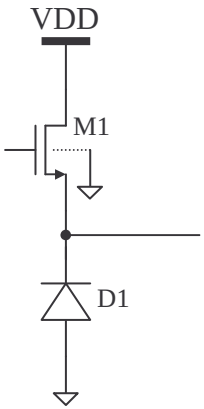
Diode operation



- Pulsed Reset
  - In-pixel self-reset circuit? More complex.
  - Hard/soft reset
  - Large output voltage range (~1.7v)
  - 210e threshold à 9mV drop in diode voltage

- Continuous Reset
  - Logarithmic response
  - May take several us to reset
  - Small output voltage range (200mV)
  - 210e threshold à 9mV drop in diode voltage

Diode reset characteristic



Wired Reset

Pulse height increases logarithmically with # electrons

100ns charge collection time

Exponential recovery characteristic

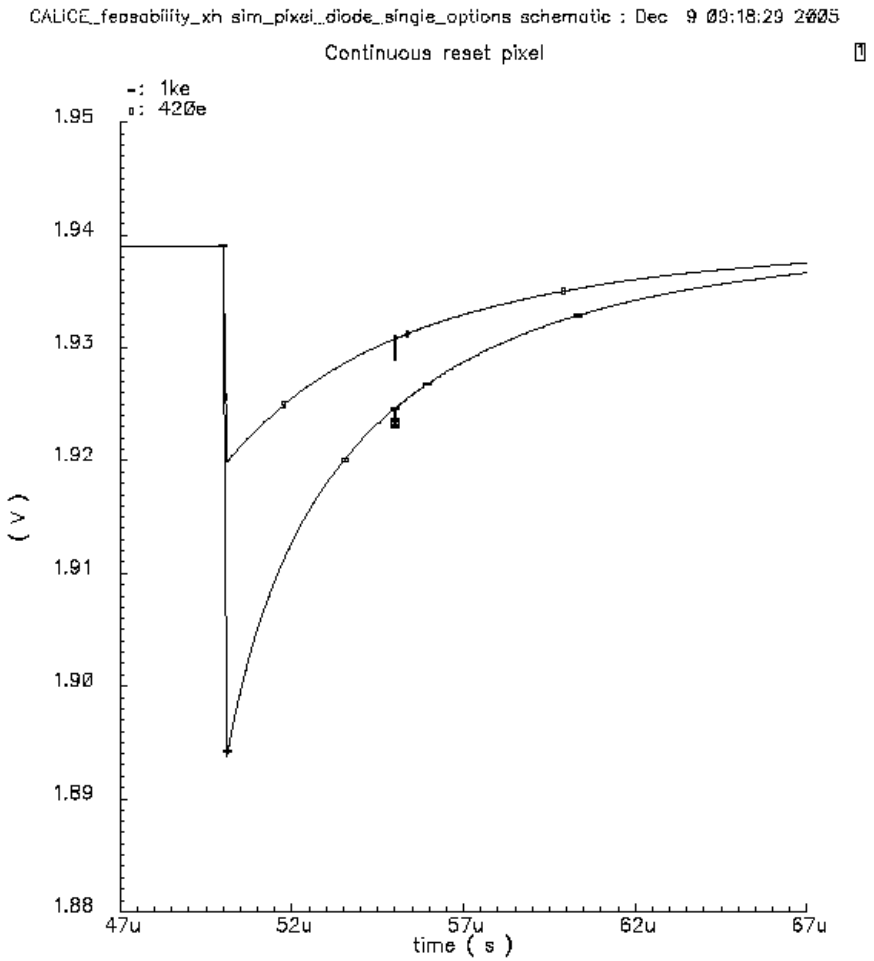
Pulsed Reset

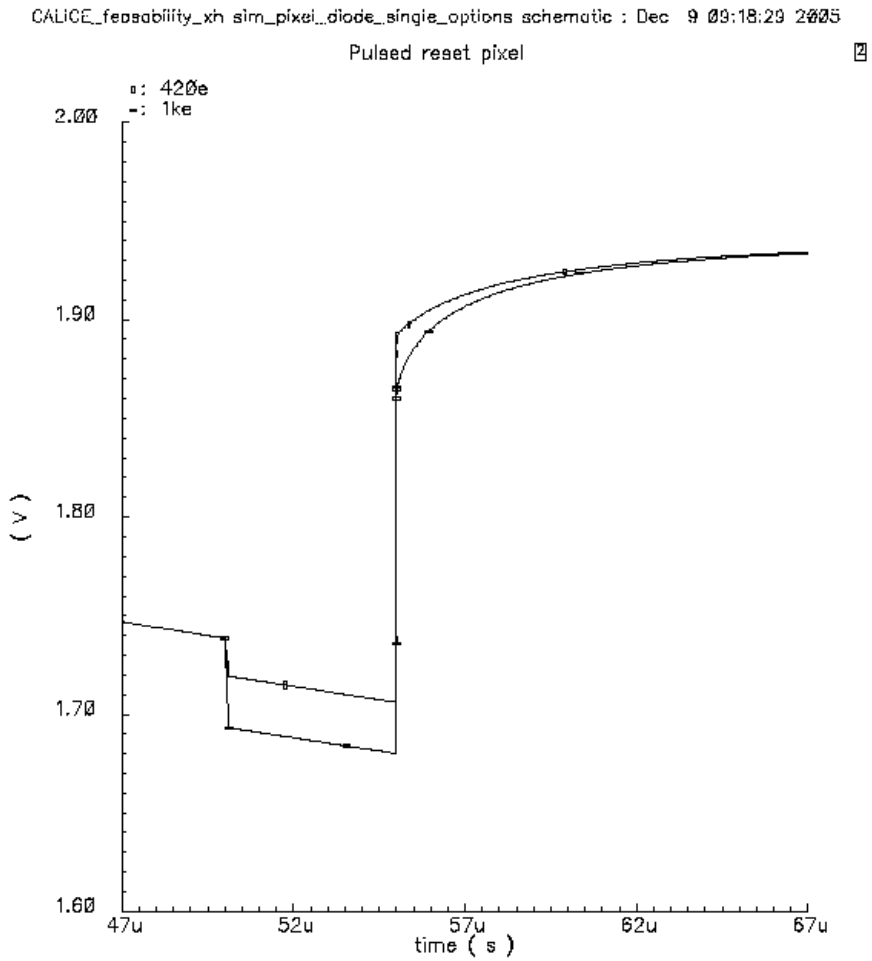
Pulse height increases linearly with # electrons

(Reasonable approximation with three Ae^{-ax} terms)

Reset is applied

Simulations

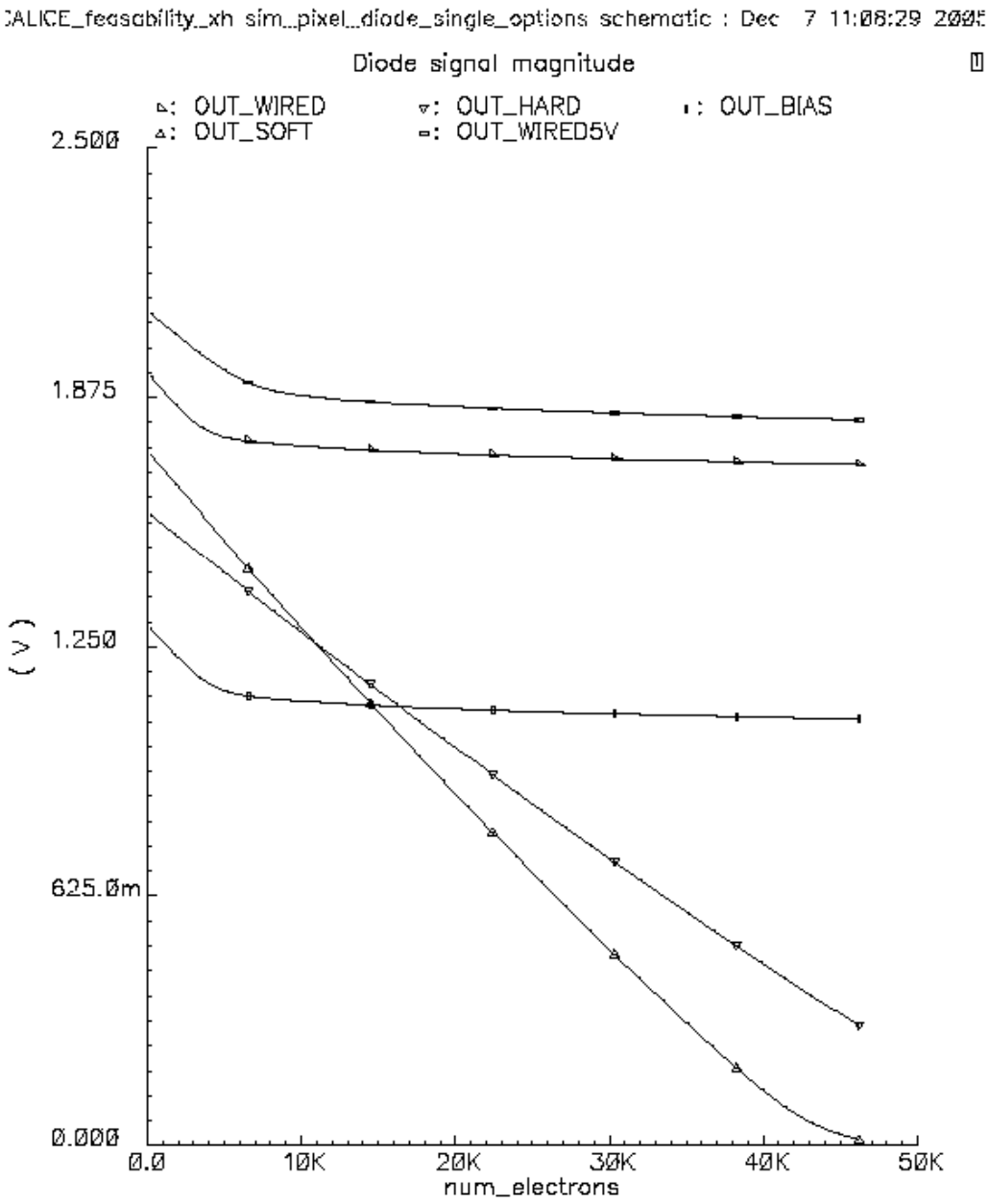




Parametric plot

Log response
continuous reset pixels

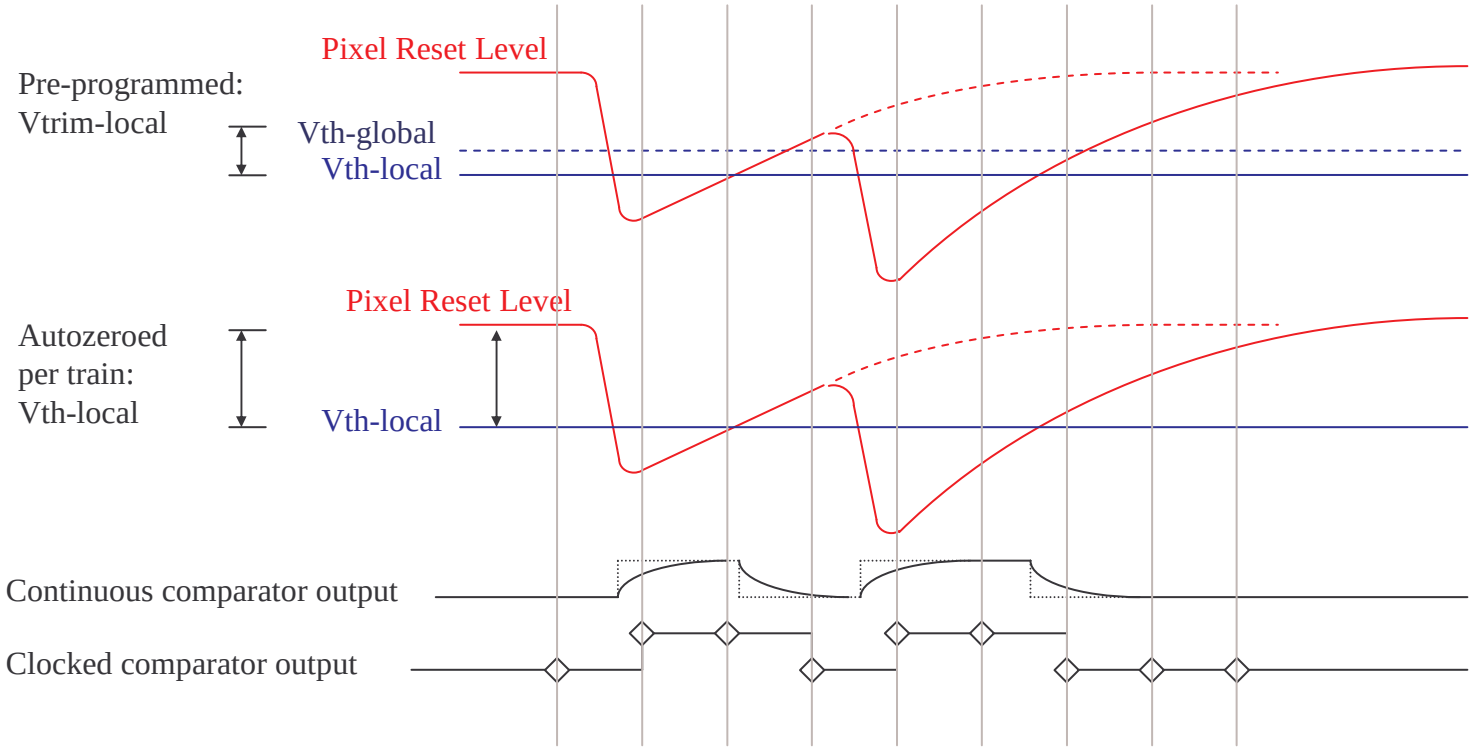
Linear response pulsed
reset pixels



Comparator Types

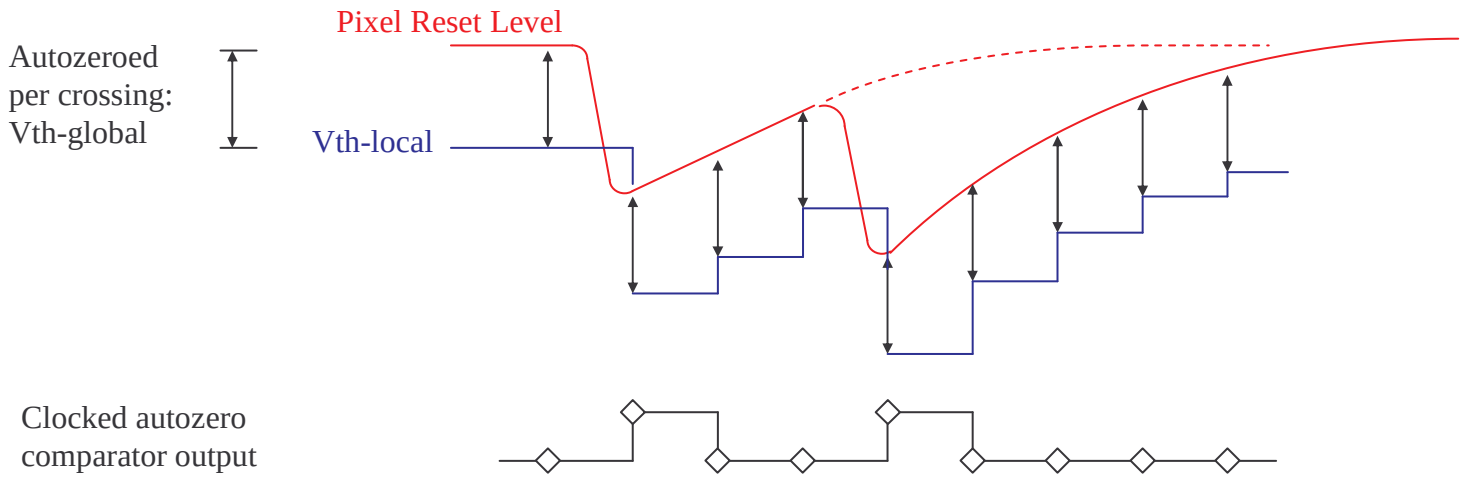
- Voltage comparator, fixed threshold
  - Clocked
  - Continuous current
- Voltage comparator, moving threshold
  - Clocked
- Differentiation comparator
  - Continuous current

Voltage comparator: Fixed Threshold



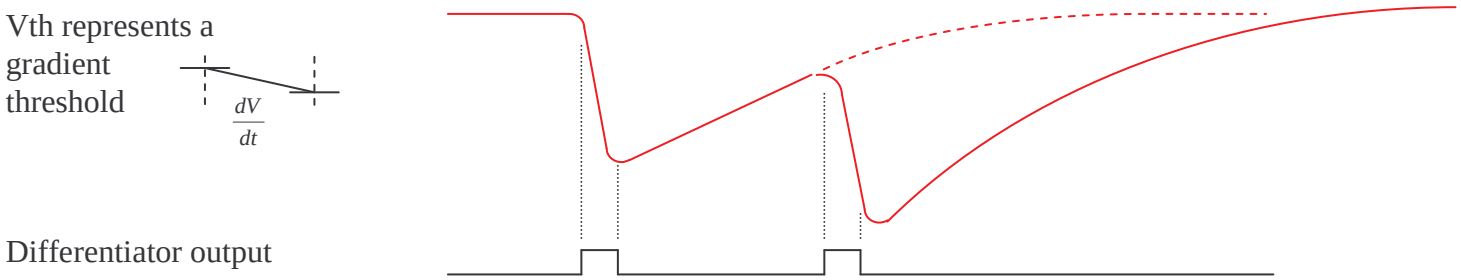
- Continuous (low current, asynchronous) or clocked (current spikes)
- Pixel/localised offset trim: Programmed & stored, or possibly auto-calibrated between pulse trains?
- As used in OPIC, but not suitable for CALICE

Voltage comparator: Moving Threshold



- Clocked circuit (current spikes)
- Real-time pixel value is sampled each clock cycle: Vsample + Vth gives local threshold for comparison
- Detects each hit once
- Immune to pixel reset rate
- Clocked design typically 2 clock signals (sometimes more, or non-overlapping schemes necessary)

Differentiating Comparator



- Continuous operation (asynchronous output)
- Capacitive coupling gives a current proportional to rate-of-change of the voltage input
- Detects each hit once (asynchronous – duration of charge collection – is linear ramp an accurate model?)
- Immune to pixel reset rate
- (Needs circuit development)

Questions…

- Take diode reset model and investigate probability of pile-up
  - Assume wired-reset style pixel
  - Is pile-up rate acceptable?
  - Large signal
- Physics simulations à # electrons figures for a 50um pixel with 4 diodes
  - Max & Min signals on individual diodes for 1 MIP
  - Necessary threshold level for optimum crosstalk
  - 4 diodes preferred from electronics view – is this enough for the physics?
- Is my hit modelling reasonable?

Multiple diodes

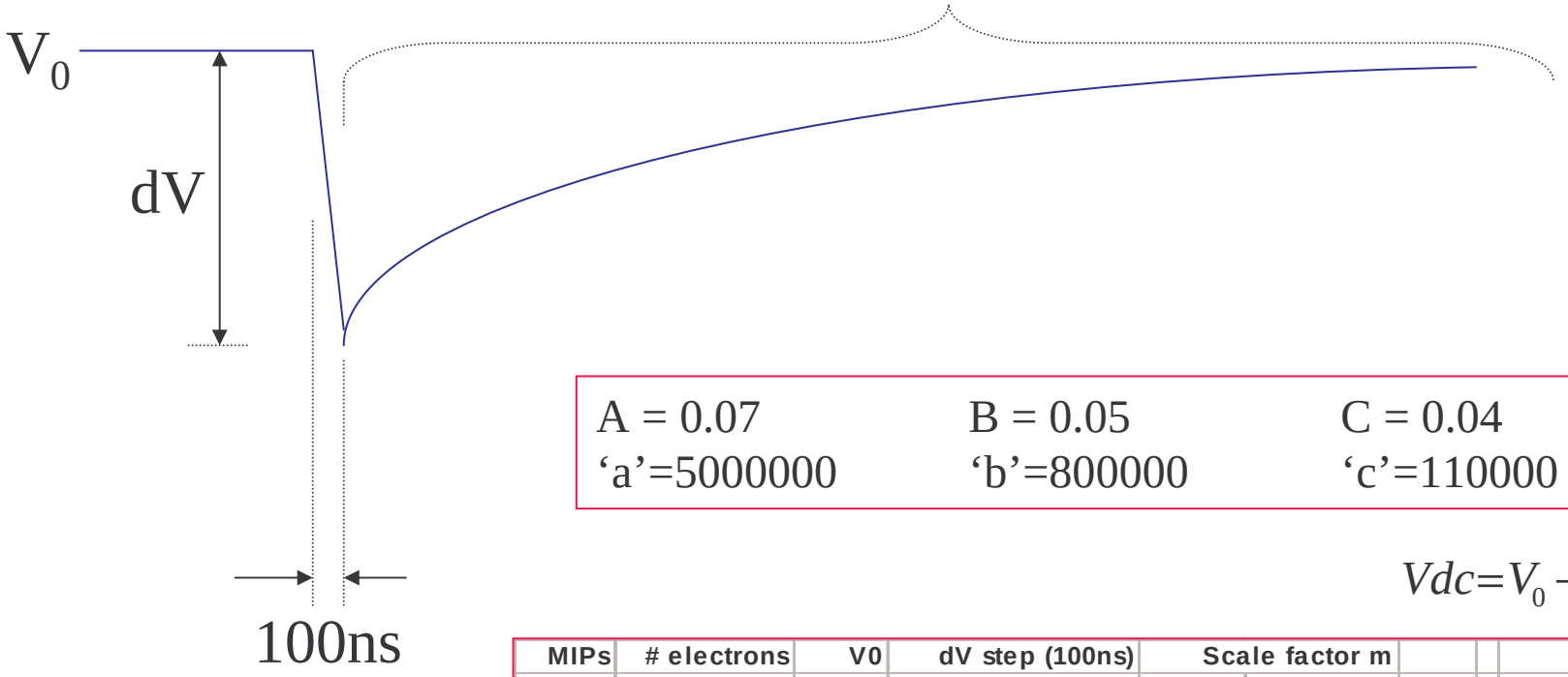
- N diodes, analog signal addition
  - Forked source-follower circuit (0.9 * Σ)
- N diodes, Individual select
  - Rotational selection wires 1 diode to pixel comparator and logic
- N parallel diodes, single collecting node
  - StarTracker: 25um pixels, 4 diodes, ~15fF node capacitance
  - Iimas: 32um pixels, 2 diodes,

Summary / Design Choices

- **Diodes:** **Parallel / Analog-sum** / Seq. select
- **Pixel size:** 25um / 40um / **50um**
- **Number of Diodes:** 1 / **4** / more
- **Reset:** Switched / **Continuous**
- **Comparator:** Fixed threshold / **Adaptive threshold**
- **Comparator:** Continuous / **Clocked**
- **Memory:** SRAM / **DRAM**
  - Variant: SIMPLE / LONG / CPOD

REFERENCE: Diode behaviour approximation

$$y = Vdc + m \cdot \left(Ae^{-at} + Be^{-bt} + Ce^{-ct} \right)$$



A = 0.07	B = 0.05	C = 0.04
‘a’=5000000	‘b’=800000	‘c’=110000

$$Vdc = V_0 - dV$$

MIPs	# electrons	V0	dV step (100ns)	Scale factor m			Vdc
1	420	1.939	19.15	mV	0.120		1.920
3	1260	1.939	56.78	mV	0.356		1.882
5	2100	1.939	92.42	mV	0.579		1.847
7	2940	1.939	123.37	mV	0.773		1.816
9	3780	1.939	145.97	mV	0.914		1.793
11	4620	1.939	159.57	mV	0.999		1.779