TeraPixel APS for CALICE

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ASIC Specifications

ASIC1

50 micron pixels
5/15um EPI (decide which now & fix)
Eg (128x128 = 6x6mm) * 4 pixel designs?
4 diodes per pixel, analog sum
Minimum signal 1 MIP
→400 electrons (giulio to confirm)
→Threshold ~ 200 electrons (giulio to confirm)
Maximum signal ~10 MIPs (guilio?/paul/nigel?)
In-Pixel Comparator
→To "fire" within 100ns of threshold crossing
→To recover/reset within 400ns
→Target noise rate 10^{-5}
Timestamp:
→~4k unique time codes at 150ns update rate
→12bits [enough for proof of principal?]
→Does not have to be a global signal,
…could be position-dependant/decoded
In-Pixel Memories:
→Minimum 4
→12bit resolution [to match timestamp resolution]
→Maximum 4
→In-pixel memory-management WRITE and READ

ASIC2

50 micron pixels
15um EPI
1 large area, single pixel design
4 diodes per pixel, analog sum
Minimum signal 1 MIP
→400 electrons (giulio to confirm)
→Threshold ~ 200 electrons (giulio to confirm)
Maximum signal ~10 MIPs?
In-Pixel Comparator
→To "fire" within 100ns of threshold crossing
→To recover/reset within 100ns
→Target noise rate 10^{-6}
Timestamp:
→~14k unique time codes at 150ns update rate
→16bits [tbd]
→Does not have to be a global signal,
…could be position-dependant/decoded
In-Pixel Memories:
→Minimum 4
→16bit resolution [to match timestamp resolution]
→Maximum 16
→In-pixel memory-management WRITE and READ

ASIC Specifications

ASIC1

Test structures
– single reticle / several structures?
Low power in mind
Maximise charge collection
→minimise NWELLs in pixel
Maximise active area
Flip-chip solder/bump pads
Edge pads for wire/bump bonding
May use extra control & power signals for debug
May use external components
No data reduction on-chip

Sparse readout
→Row,column+timestamp
→1200 max row/col length
→11bits each row & col address
→22+16=38bits per hit
→Pipelined for max readout rate
98ms available for readout
5ms realistic for DRAM lifetime
No data storage at periphery?
Parallel data output off-chip (standard logic level

ASIC2

Test sensors for beam tests
– full reticle / stitched(?)
Implement low power circuits
Maximise charge collection
→minimise NWELLs in pixel
Maximise active area
Flip-chip solder/bump pads
Localised central area of pads?
Minimise control & power signals
Minimise external components
Data reduction on chip?

Sparse readout
→Row,column+timestamp
→1200 max row/col length
→11bits each row & col address
→22+16=38bits per hit
→Pipelined for max readout rate
98ms available for readout
5ms realistic for DRAM lifetime
Temporary data store in periphery?
High speed serial LVDS tx off-chip

Scope of ASIC design work at RAL

Includes (design)

Pixels & peripheral ASIC circuitry

→Full ASIC 1 spec to be agreed prior to design work (~May 2006)

→Full ASIC 2 spec to be agreed prior to design work (~June 2007 (tbc))

IDR & FDR for each ASIC

Interim & final pixel/die NWELL profiles for physics simulations

Peripheral/example PCB circuit schematics

Solder/bump bond pads (to spec ←)

Off-chip drivers (to spec ←)

Excludes

Identify PCB/Assembly house

→ required for spec of bump bond pads

Bump bonding feasibility & techniques searches

All aspects of long/high-speed PCBs

→ May define transmission protocol / off-chip driver requirements

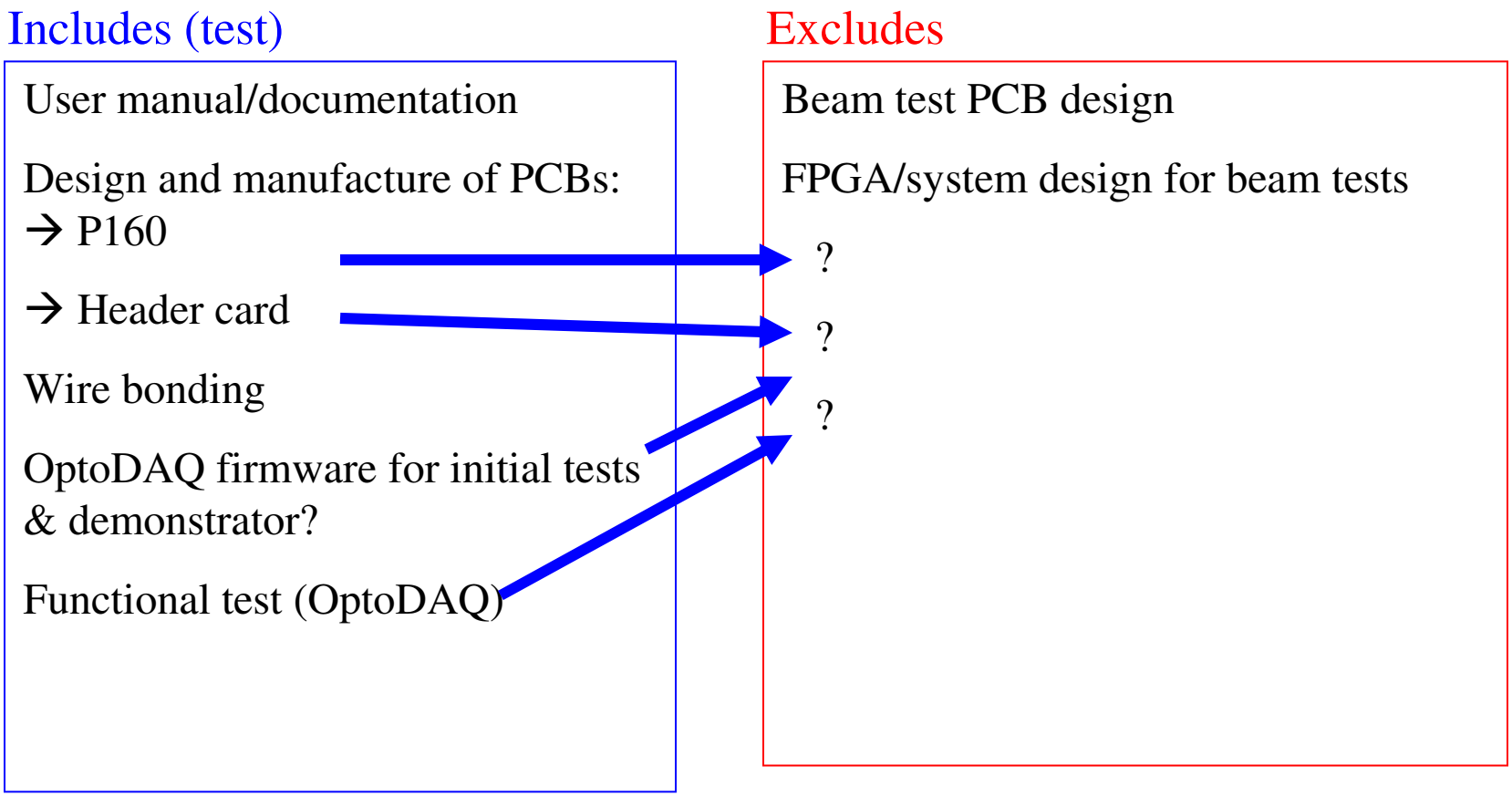
Controller FPGAs

System-level design

Physics simulations

Thermal modelling

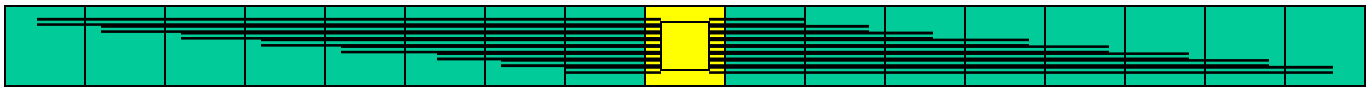
Scope of ASIC testing at RAL



Greatest Risks to ASIC design

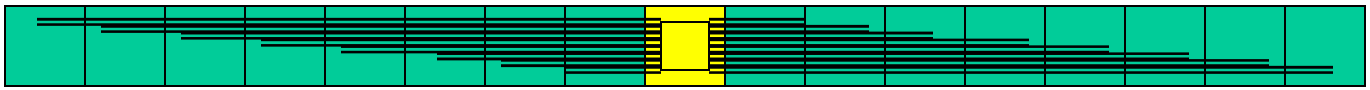
- In-pixel Memory management (read/write select
  - Asynchronous state machine?
  - N-Stage shift register (lots of transistors!)
  - Local centralised controller?
- In-pixel comparator (to meet noise rate at low power
- Analog Sum
  - Forked Source follower – needs characterising
  - Other circuits?

Memory Management: Local Controller



- 1 in 2N pixels is a Dead Pixel called a “Local Controller”
- The local controller is hard wired to every comparator and memory register in its jurisdiction (2N pixels)
- The local controller manages the Hit Flags and register enable signals, such that it will fill its pixel’s registers sequentially as hits occur.
- During readout, a token passes through the column of “Local Controllers” – these sequence the readout of their “hit” registers and send row/column addressing to the column base to reconstruct complete hit data.

Memory Management: Local Controller



- Reduces complexity of pixel logic
  - Fewer Nwells in pixel → better charge collection
  - Removes most of digital logic from pixel (good for analog signals)
  - Allows room to relax constraints on comparator circuit (better circuit)
- Dead Pixels, arranged as columns contribute to overall dead area
- Large routing overhead
  - 4 registers
  - N pixels
  - N+4N horizontal signal lines!
  - 4N hit-flags in controller
- Any logic/SRAMs even acceptable in the controller as charge is not collected!
- Acceptable dead area?
  - Preferred as a column of dead pixels?
  - Or scattered as reduced charge sensitivity?

Assuming controller is double-sided:
N=8 → 40 signals, 32 HitFlags @ 6% dead area
N=12 → 60 signals, 48 HitFlags @ 4% dead area
N=16 → 80 signals, 64 HitFlags @ 3% dead area

M1/M3/M5 take 20 signals each (N=12)
@0.8um each = 16um width tracking

N=12 → 24+1 * 50um = 1.25mm column set
(single stitch unit?)

Towards Lower Power

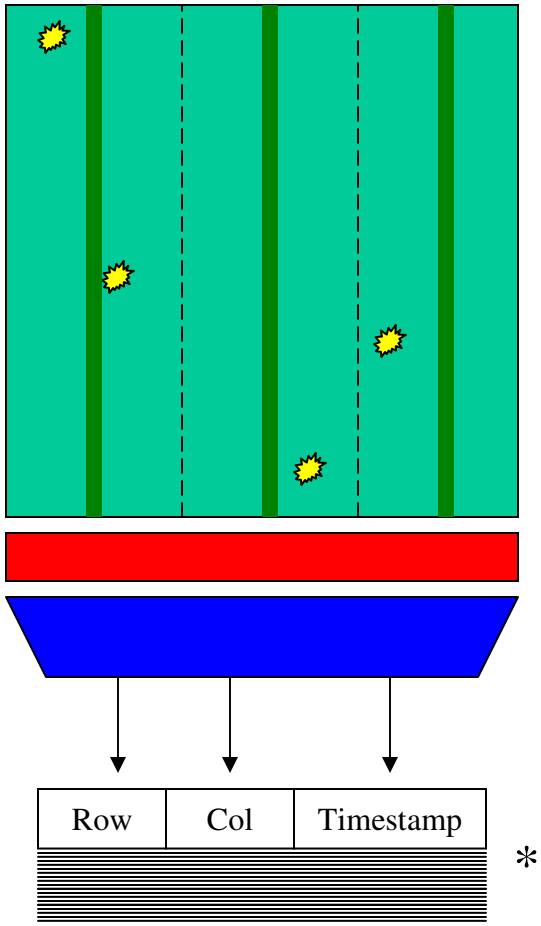
Techniques to “recycle” charges often employ inductor based circuits
Other techniques avoid inductors
→ Adiabatic Charging: Stepwise charging/discharging reduces energy dissipation by factor of N, using N voltage charging steps (/tank capacitors)

Summary

- Techniques do exist, would require more reading & simulations to see whether the CALICE chips could benefit
- Power efficiency should be a secondary focus for first ASIC
- Once pixel design is proven, second ASIC could develop and implement power-saving techniques

NP “Zipper” Logic may suit a stepwise clock?

(end)



*(nHits)