Tera-Pixel APS for CALICE

SRAM Column Concept

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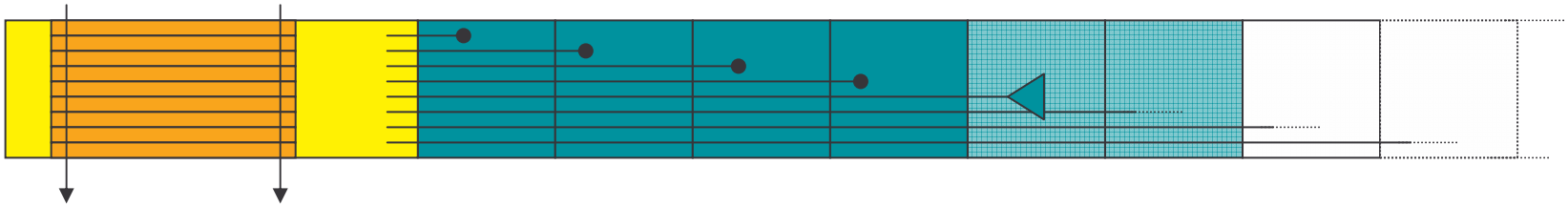
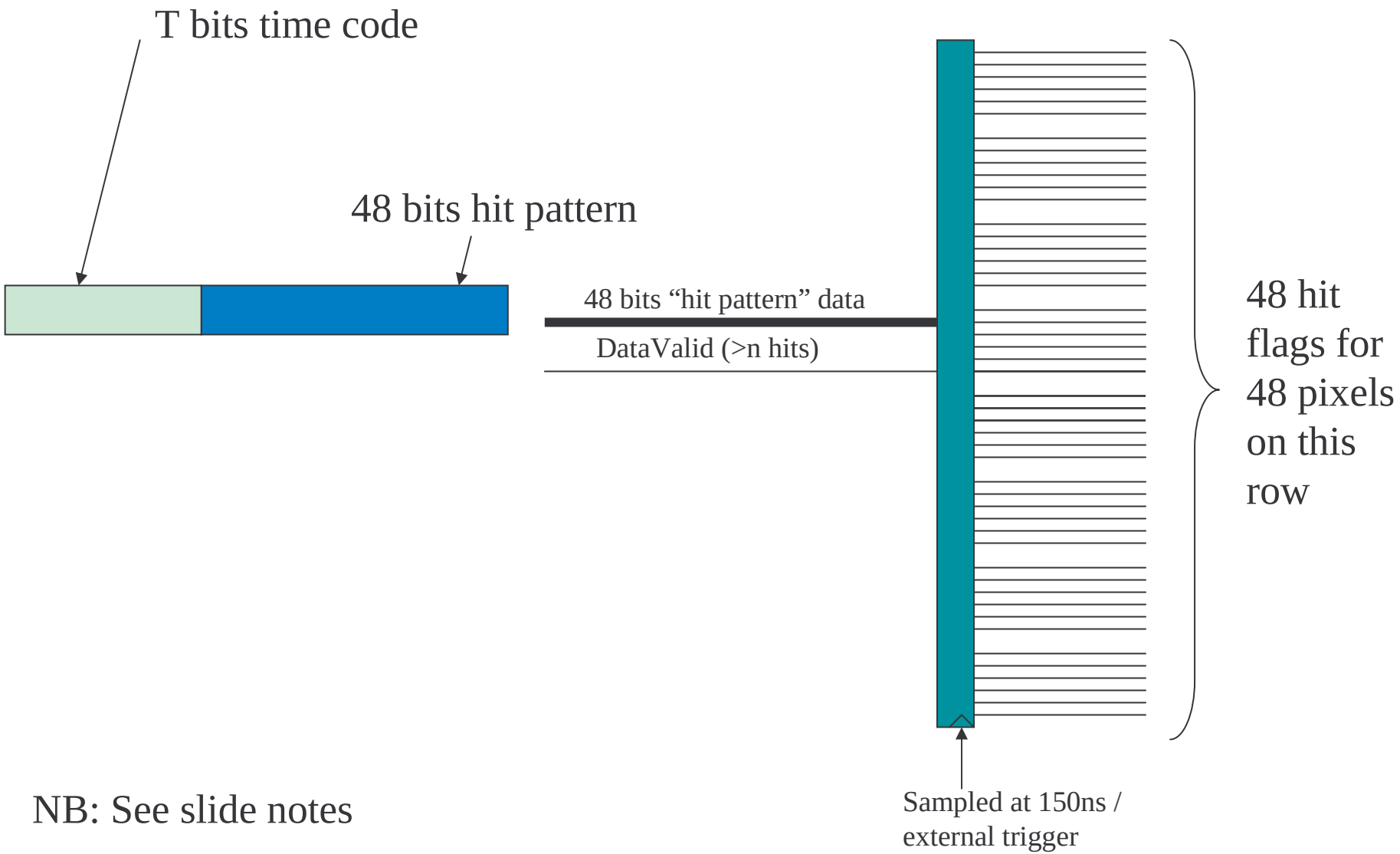
Centralised storage: Overview



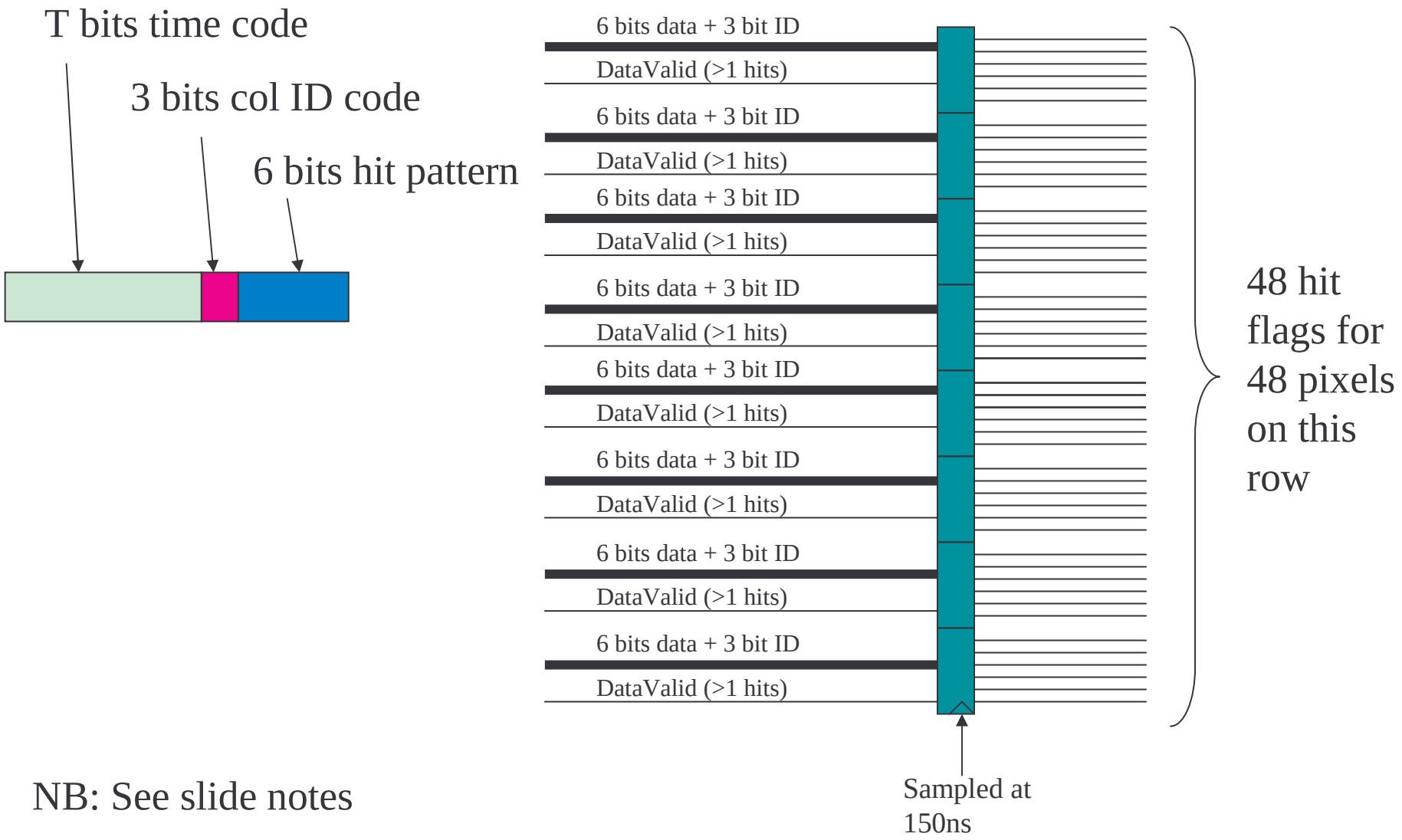
- Pixels contain diodes, analog circuits and comparators
- “Hit” signals are routed horizontally to readout columns
- Readout columns store pattern hit information with timestamp in the register bank
- Data held in the register bank is read all the time at high speed (~60Mhz)
- No timing code distribution to all pixels (power hungry)
- No memory cells inside the pixel! (More room for clever comparator, threshold trimming?)
- Example: 50 pixels served by a 3-pixel wide control column à 6% dead space

Hit Pattern Storage



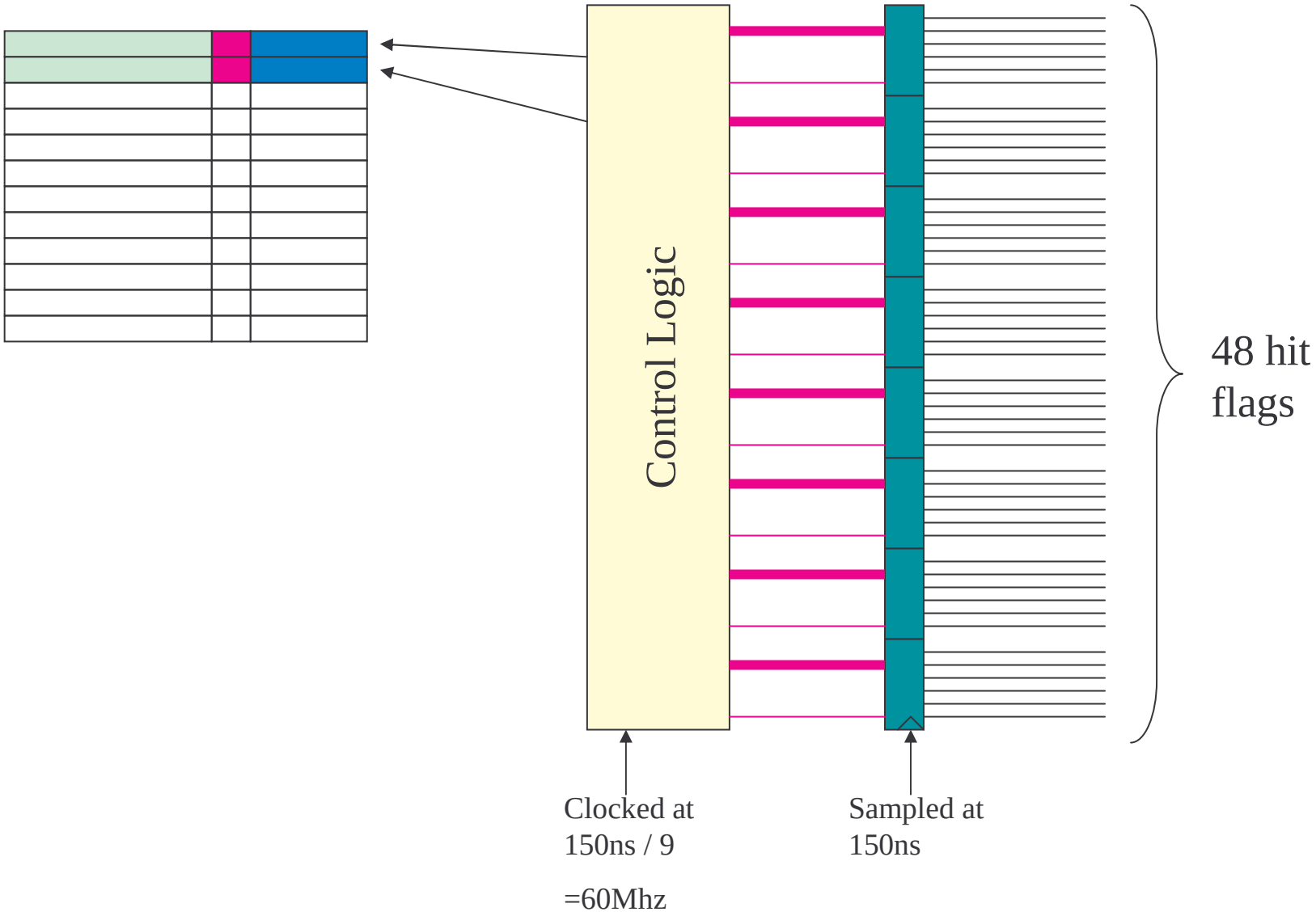
NB: See slide notes

Hit Sub-Pattern Storage

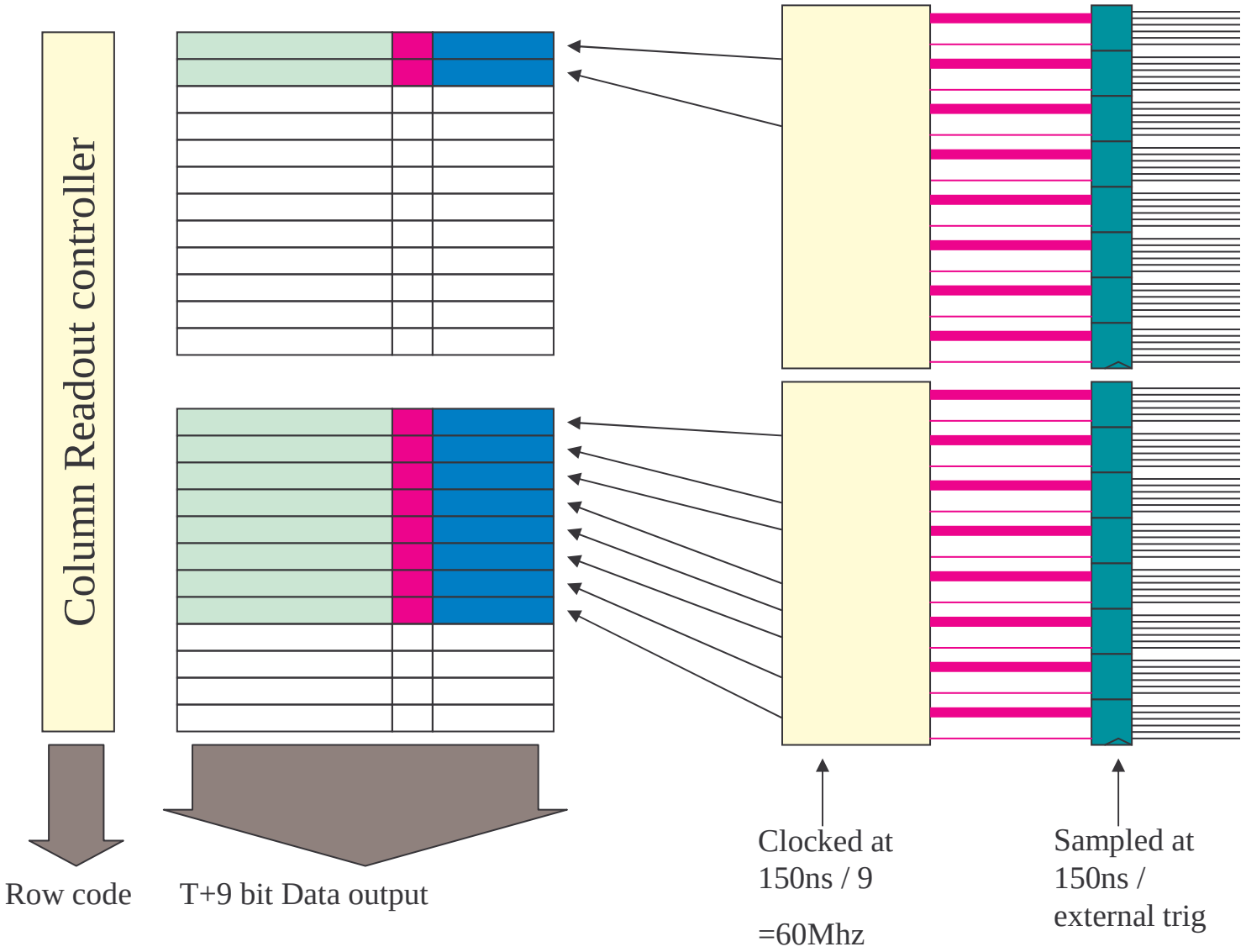


NB: See slide notes

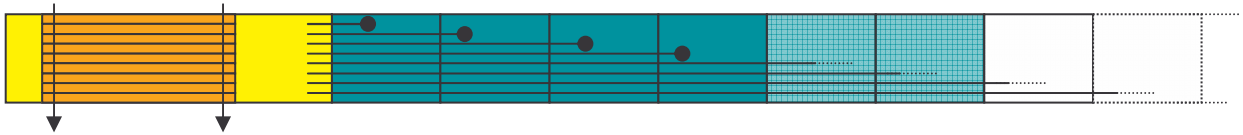
Hit Pattern Column Storage



Hit Pattern Column Readout



Centralised storage: Debate



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- Removes digital logic. memories & complexity from pixel area
- Less Nwells in pixel will help sensitivity to charged particles
- Pixel essentially then contains just analog circuits (sum+comparator)
- Logic design is not constrained by need to minimise Nwells, and by the need to locate these Nwells in specific regions of the pixel.
- Timing code only distributed to control column (not every pixel) thus saving significant power dissipation
- Data readout only operates in one central column – less circuits/multiplexing à lower power
- Trigger clock distribution to restricted area, not every pixel à less skew, lower power

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- Requires very high density of local routing to/from “column controller” pixel.
- Removing memories from the pixels uses silicon area that will contribute to overall sensor dead space.
- Suits smaller technology *(0.35um allows less dense routing, and larger logic, meaning a “local controller” can command less pixels, increasing overall dead space)* hence higher costs & greater risks
- Needs feasibility calculations to determine how many registers per row are required to meet expected noise & physics rates.
- May not meet overflow probability spec à needs to be checked!
- Control column likely 100-200um wide, but will command ~2.5mm pixel area

Centralised Storage Feasibility?

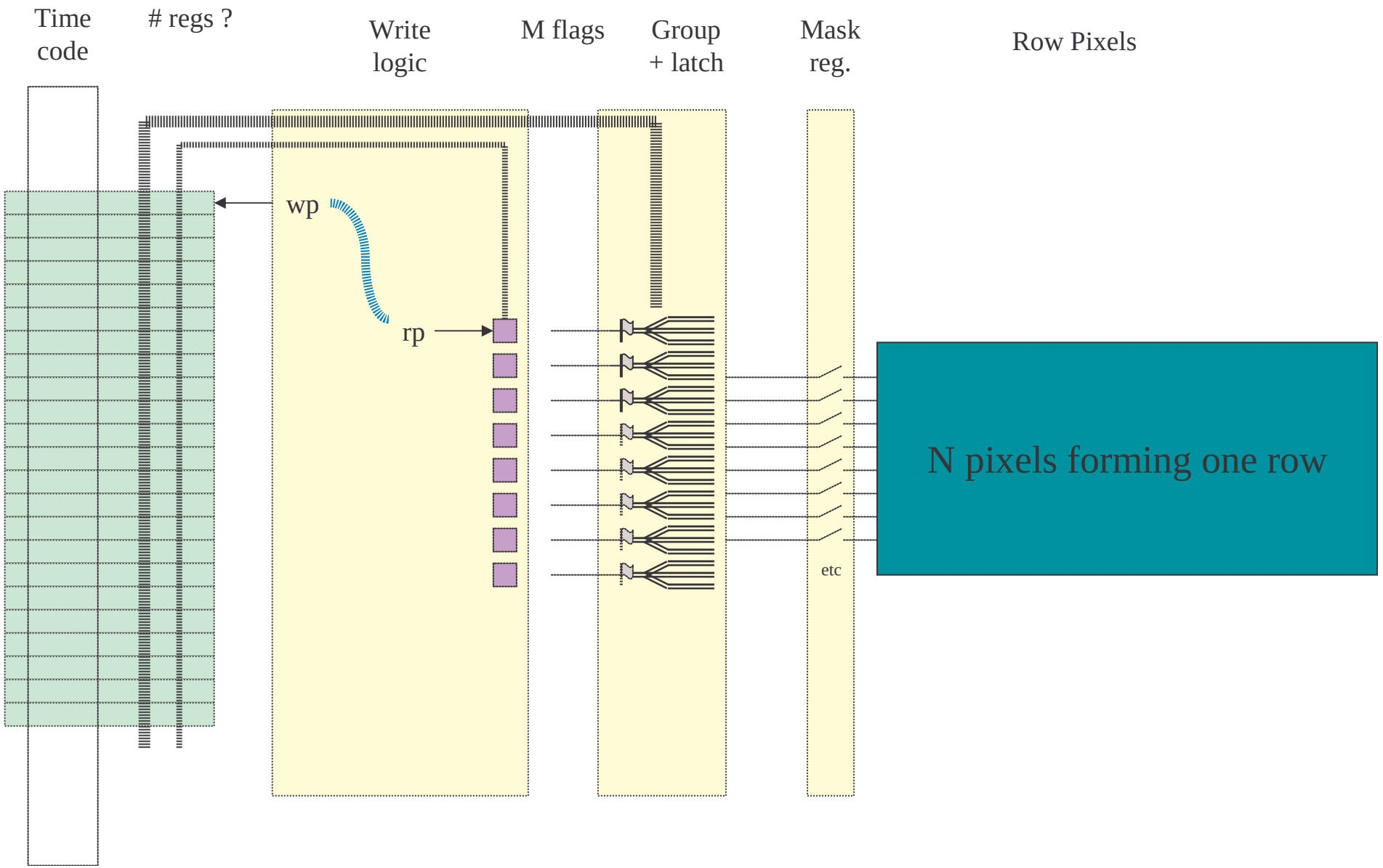
Consider N=48 pixels on the same row sharing a controller (4-6% dead space)
Pixels are grouped into M=8 sub-sets
A sub-set corresponds to N/M = 6 pixels
If >1 pixels in a sub-set is hit, then that sub-set hit pattern is logged with time & id code
Controller has S storage registers which can be used for hit pattern logging
Noise hit rate 10e-5 à 10e-6
How many registers (S) are required per row to match the 4 regs-per-pixel requirement?

Adding extra full registers is more difficult, and would be costly in silicon area
Adding extra bits to accommodate larger hit-patterns is less costly in silicon area

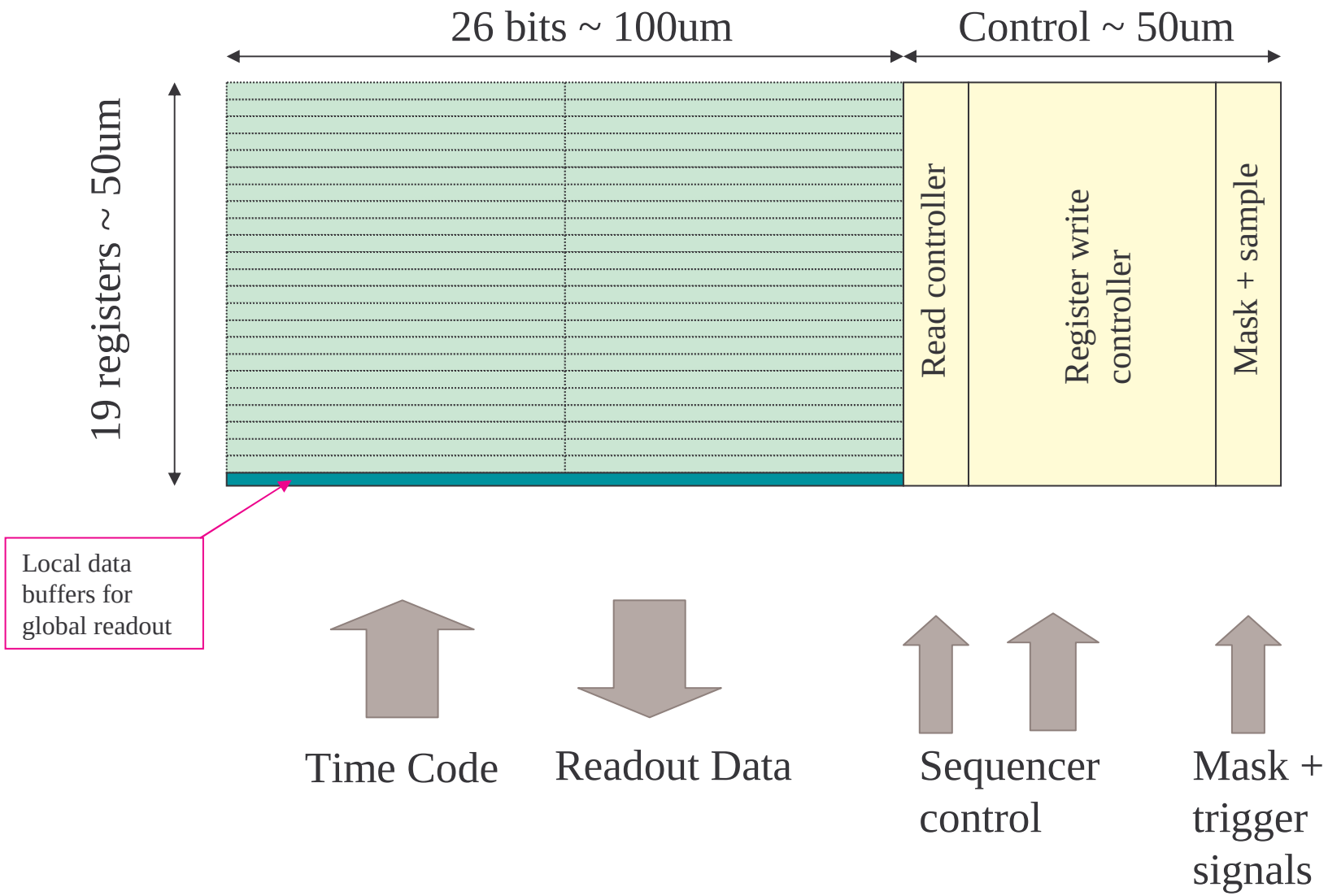
Comments

Presumably there is some optimum for M, the number of sub-sets, to trade off data set size for real versus noise hits.
Can also change N to optimise dead space, allowing ~150 microns for the control column
Slight extra overhead of data decoding off-chip, but could easily be built in at FPGA level

Independent ROW controller



SRAM register bank size estimates



Mask register + Latch