Tera-Pixel APS for CALICE

Progress meeting, 17th May 2006

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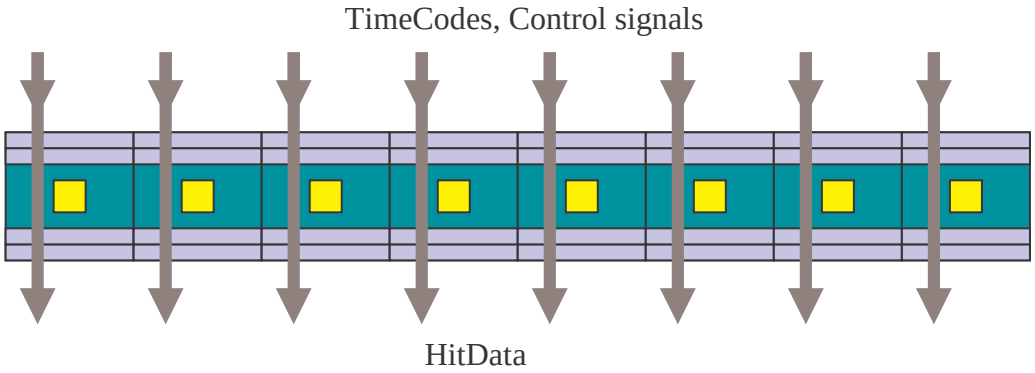
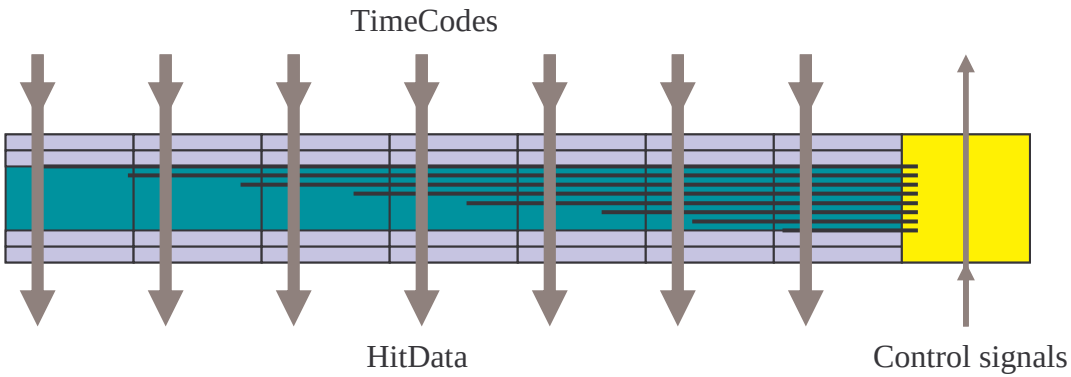
Bump Bonding

- Gold stud + conductive glue
- 100um pads (may be able to bump to standard pad cells)
- Heat (>175º) + Pressure
- Hand alignment & trials à extra effort req’d
- Physical size may be problematic
  - 2inch hotplate
  - Would eventually need very large cavity reflow oven
- Indium requires special wafer processing



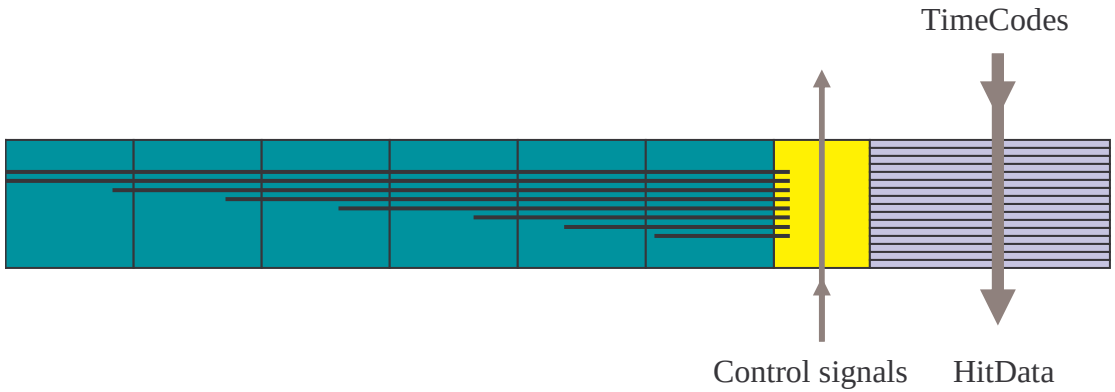
Fully Independent pixels

-DRAMs only à max 4 regs per pixel
-Most regs not used
-Time code & data sense circuits required for every column (N)
-Control logic complex à large area
-Significant dead space in every pixel à poor charge collection



Centralised controller

-DRAMs only à max 4 regs per pixel
-Time code & data sense circuits required for every column (N)
+Complex control logic moved out of pixel
-Reduced dead space in every pixel à better charge collection
-Dead area ~6%



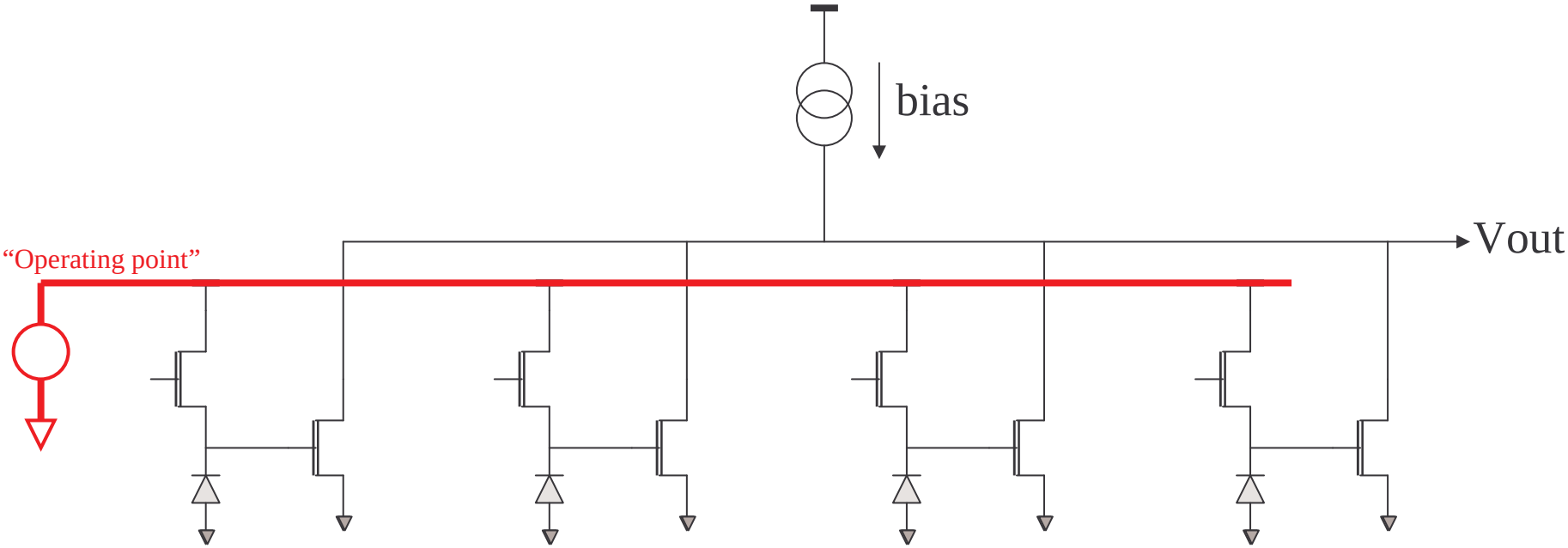
Centralised memory + controller

-SRAMs can be used in dead areas
-Limited storage facility (calc overflow prob!)
-Only 1-in-N time code & data sense circuits
+Complex control logic moved out of pixel
-Reduced dead space in every pixel à better charge collection
-Dead area ~6%

See separate PowerPoint

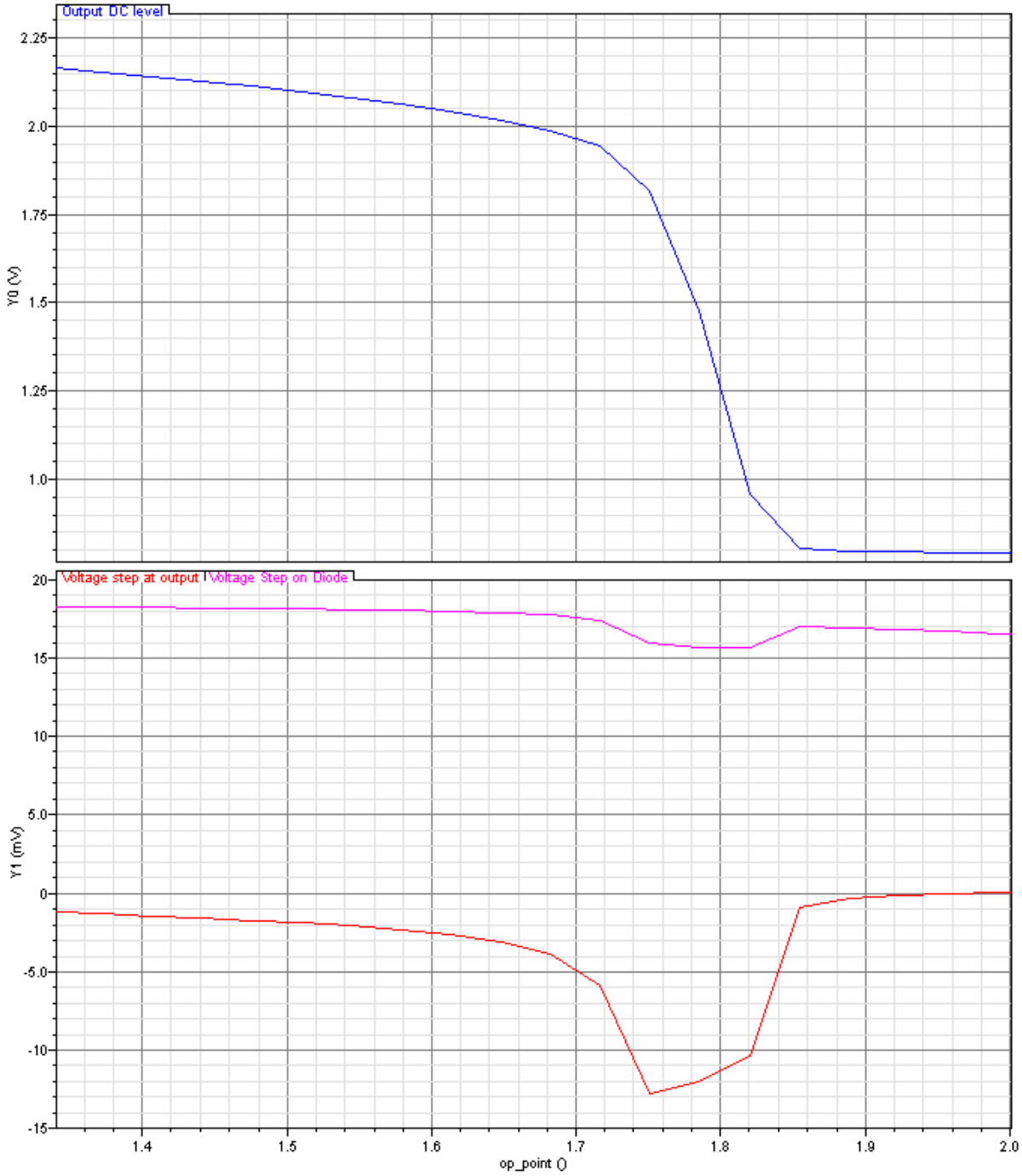
Key — Pixels containing diodes — Active Control logic — Memory cells

Analog Sum



Analog Sum

450 electrons
1 diode collects all
Sweep diode reset point

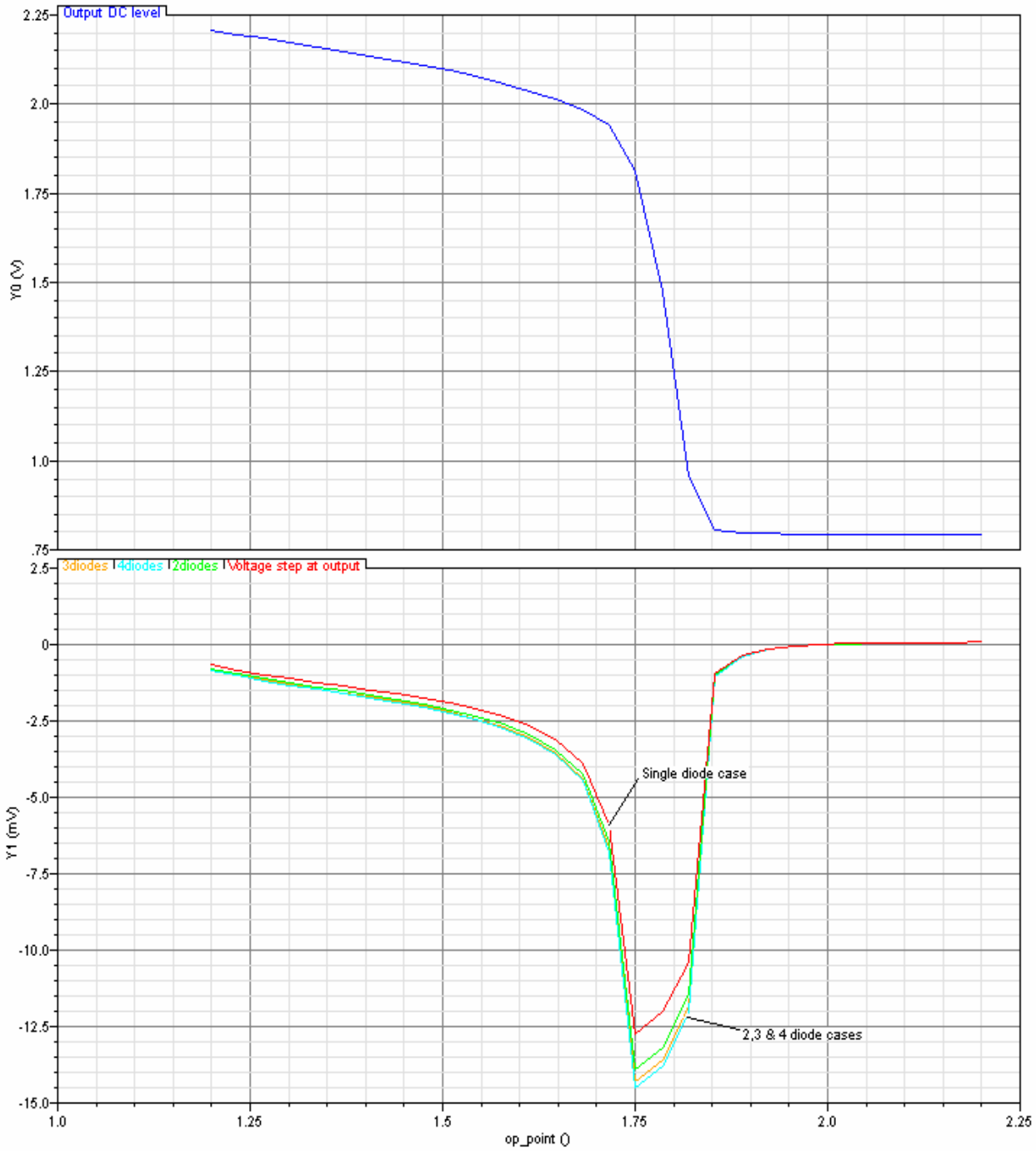


Analog Sum

450 electrons

- 1 diode collects 450e
- 2 diodes collect 225e
- 3 diodes collect 150e
- 4 diodes collect 112e

Sweep diode reset point



Analog Sum

450 electrons
- 4 diodes collect 112e

Sweep diode reset point

4 cases: bias currents
- 250nA
- 500nA
- 750nA
- 1uA