Tera-Pixel APS for CALICE

Progress meeting, 12th July 2006 Jamie Crooks, Microelectronics/RAL

Phone meeting with Foundry (June 19th)

• Foundry Actions:

- Check the possibility of performing process splits in Shuttle run à Yes this is possible
- Check the availability of the corner model for Deep N-well Diode dnwell33 à *No model avail*.

-pending

- Check the availability of the GDS files of the following IO pad libraries:
 - staggered analog pads
 - PCI inline pads
- Check if Foundry offers large IO pads (100um x 100um) both for Analog and Digital
- Send Rutherford the shuttle schedule for the beginning of 2007

• <u>Rutherford Actions:</u>

- Send Foundry a draft of Calice project *à Sent example pixel GDS*
- Send Foundry Rutherford's requirements for TCAD tool both for MI3 and Calice projects.
 à Sent summary document (details from Guilio)
- Fill out and send Foundry the CIS Application General Questionnaire for Calice project (see attached)



Demo Pixel

Analog Pixel

- Voltage amplifiers disappointing
- Charge amplifiers may be more appropriate
- Autozero comparator may be too complex
 Clock line switching in every pixel
- Simpler comparator design possible if we can reset the pixel after a hit?



Charge Amplifier

- к Smaller Cfb à Larger output step
- J Charge-to-voltage gain is independent of Cd (hence can have 4 diodes in parallel)
- J Larger voltage step at output than seen before
- L Purely capacitive feedback requires a reset phase
- K Diode feedback provides resistive 'biasing' feedback
- L No corner of MonteCarlo models for diode
- L Parasitic feedback subject to layout and accuracy of 3D parasitic extraction tools!





