Summary/Dialogue

The double-sampling pixel has been shown to perform reasonably well, offering signal-to-noise ratio comparable to the pre-shape pixel, 20% less power and 50% less NWELL.

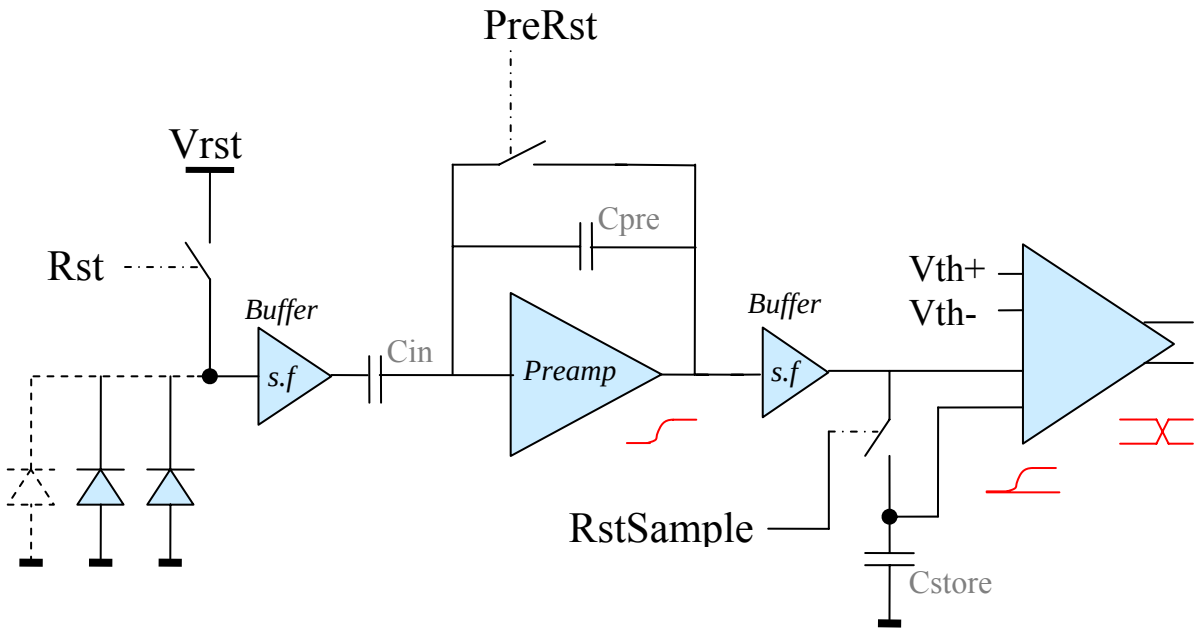
For comparison, signal-to-noise ratio is calculated to be approx 7 for a 250 electron signal collected on four 1.8um diodes for this pixel architecture. Noise must be considered twice (factor $\sqrt{2}$), since the output is sampled and both this sampled output and the real-time output form the differential input to the comparator.

Disadvantages to this pixel design are mostly concerned with the one-hit nature of the pixel circuits, that must be reset following a hit if they are to detect another hit – this introduces additional complexity into the row-controller logic, and if the whole sequence is squeezed into 150ns (to make the pixel blind for only one bunch crossing) the circuits barely have time to settle, introducing an error of order 10% to any subsequent signal hit. Furthermore, this error increases for larger predecessor signals, and can only be corrected by allowing longer for the reset – 300ns would suffice.

This pixel is very sensitive to additional capacitance at the input, which degrades the signal height – full parasitic extraction will be important to check the final layout and predict how it will function.

Signal magnitude may be most effectively increased by decreasing input capacitance (parasitics, careful layout) or by reducing the size of the feedback capacitor (where the techniques available and associated risks are the same as for the preshape pixel design).

PreSample Pixel Overview



Brief Operating Instructions

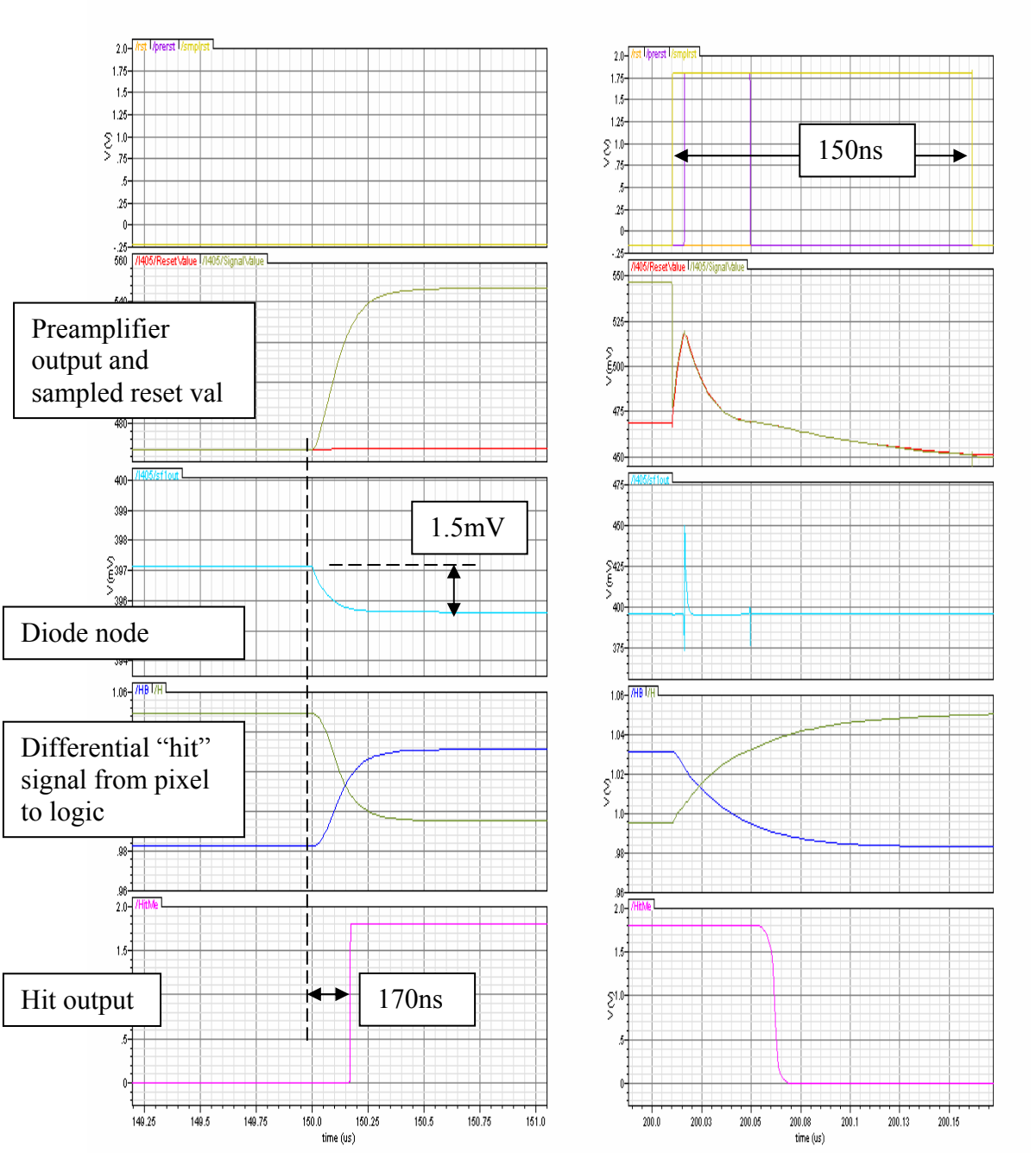
- The pixel diodes are reset prior to a bunch train. (The diodes are then not reset during the bunch train.)
- Immediately before the bunch train commences, or after a hit is detected the following 150ns reset/sampling sequence occurs:
  - The preamplifier is reset for 15ns
  - The preamplifier output settles (final value after 150ns depends on previous hit magnitude, bias currents and process variations)
  - The reset sample is taken after 140ns (or longer if possible to reduce error in sample)
  - The pixel is now active
  - If the preamp had not fully settled in the 150ns window a small error will develop between the signal and the reset sample; this error will be added to the magnitude of the next signal that arrives.
- The diode source follower buffers the pixel signal from transients during preamp reset.
- The diode node collects charge and is read in voltage mode, therefore additional capacitance on the diode node will decrease the voltage (and therefore signal) that is seen by the circuit.
- Decreasing Cpre would increase the signal magnitude (gain of charge amplifier is ratio of Cpre to Cin)
- Increasing Cin further would improve gain in the preamplifier but requires more current in Buffer and Preamp stages to reset correctly in 150ns.
- Current in the output source-follower should be adjusted to ensure the writing of the reset value to the Cstore capacitor can properly complete in 150ns.
- The comparator takes signal and threshold in differential form and outputs a low voltage differential hit signal that must be sensed with a secondary PMOS comparator at the input to the logic blocks, where it is converted to 1.8v logic.

PreSample Pixel simulation: Example Operation

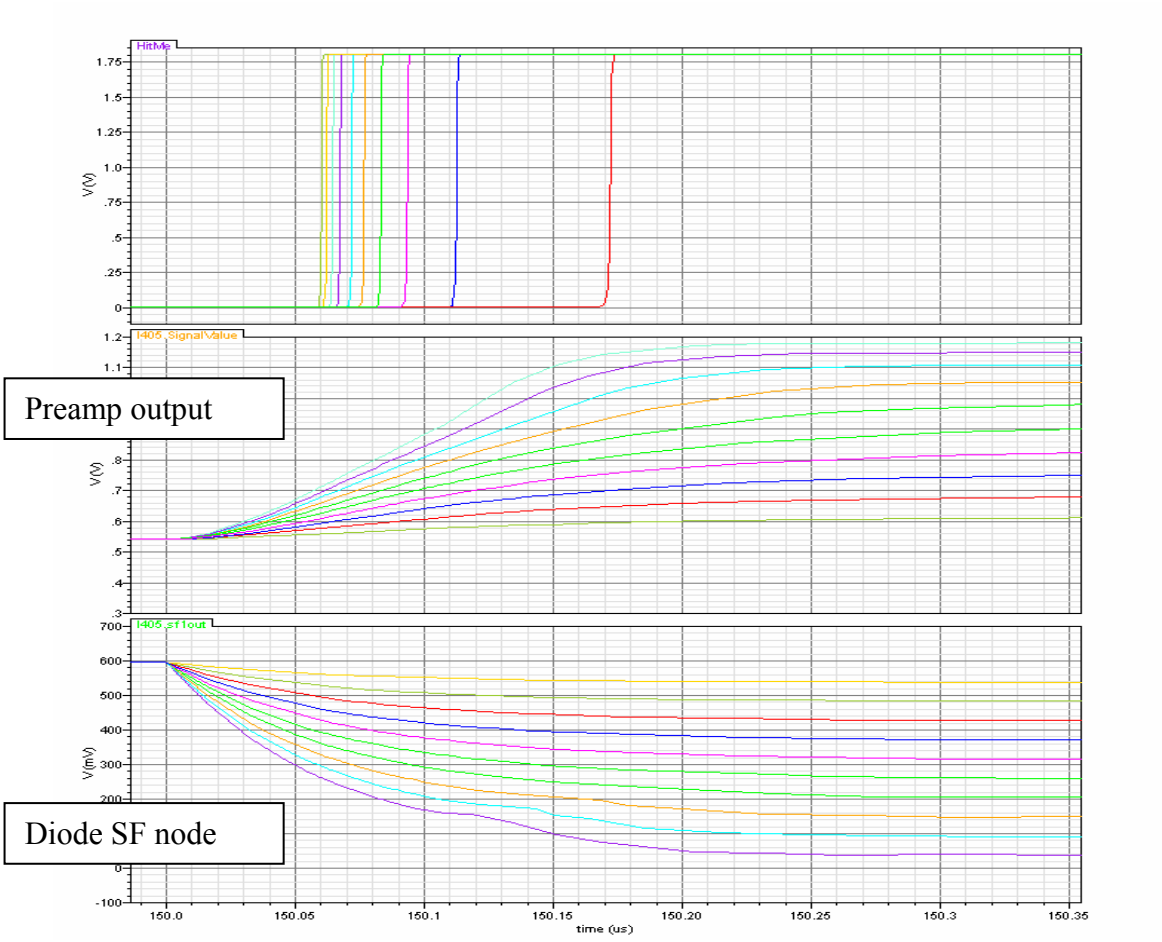
Circuit stimulus/scenario

Basic operation of the pixel circuits is demonstrated:

Results waveforms



Above: Pixel waveforms after the various stages, from MIP hit to logic "hit" decision, with the reset sequence illustrated on the right. In full-system operation the row controller logic would instigate the reset sequence (locally) immediately after the hit is sampled, such that the pixel is active again 150ns after the hit was detected.



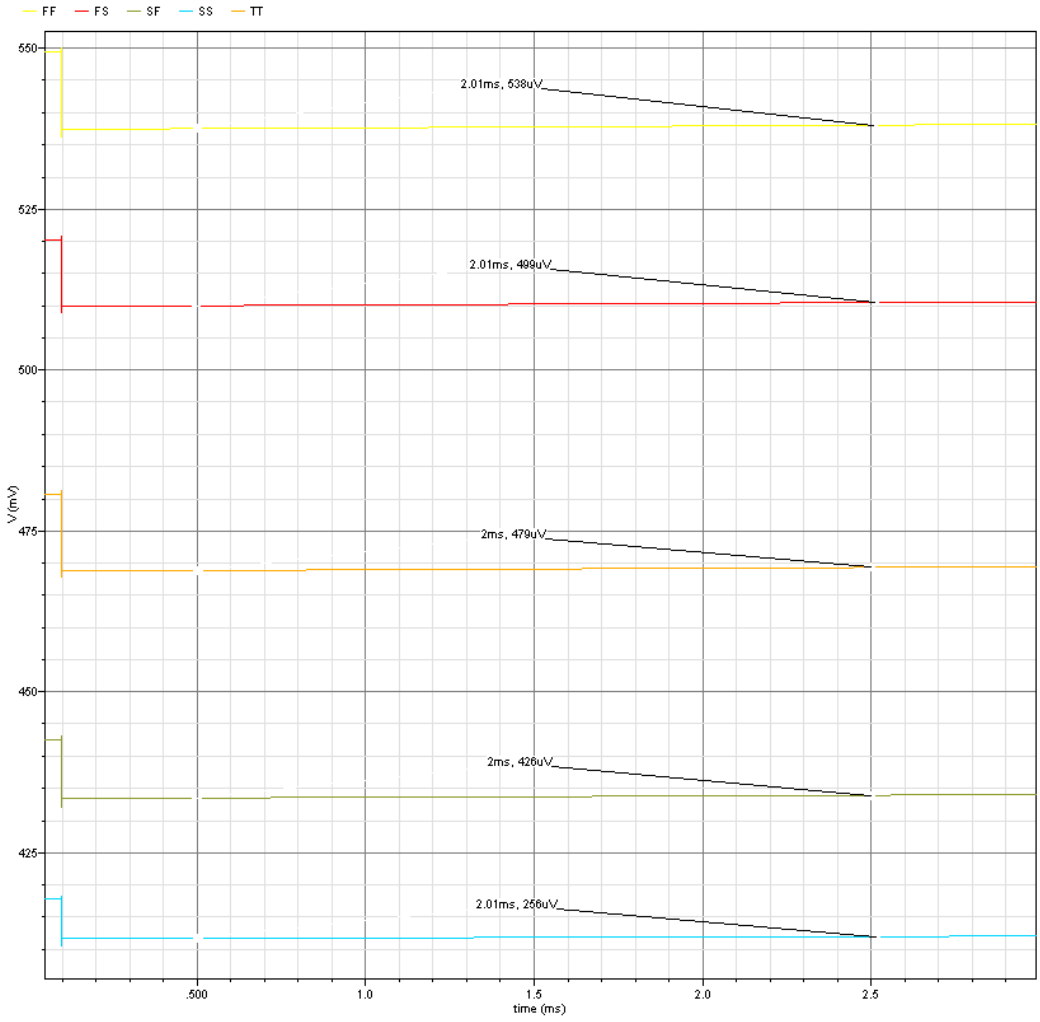
MIPs	#electrons	Signal pulse (final)	Delay to Hit (ns)
1	250	73	170
2	500	146	112
3	750	221	94
4	1000	300	84
5	1250	382	77
6	1500	473	72
7	1750	559	68
8	2000	624	65
9	2250	669	63
10	2500	705	61

Above: Typical results for signal sizes 1 to 10 MIPs.

PreSample Pixel simulation: Bunch Train Operation

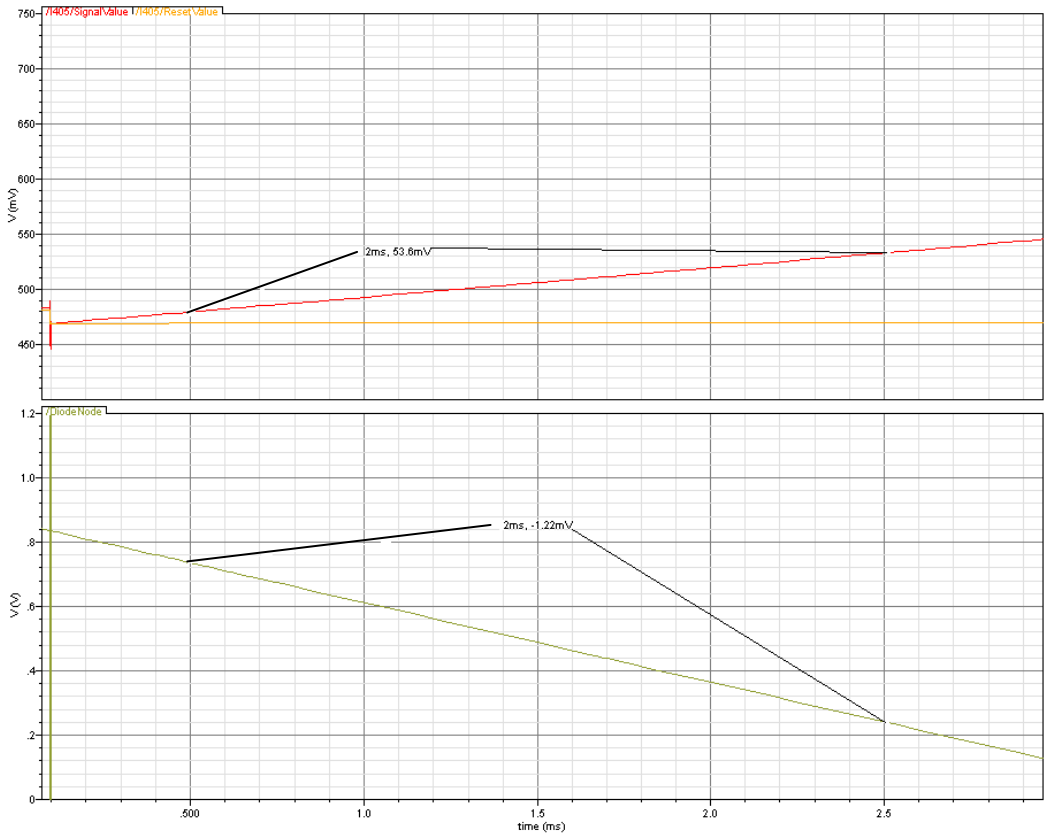
The pixel is simulated for the full 2ms bunch-train length.

Results Waveforms



Above: The reset sample leakage is seen to be small – checking all process corners indicates a worst case error of 500uV over 2ms.

The leakage from the storage capacitor is primarily through the switch to the signal output node on the other side – during bunch train operation, if there is no hit, this value should closely match that stored on the capacitor anyway, in which case the leakage will only act to track any movement in the output node. So whilst this simulation is probably an accurate indication of the system operation, it does not represent the leakage from the storage capacitor if it were used in any other location where the signal node were to move to gnd or vdd after a write.



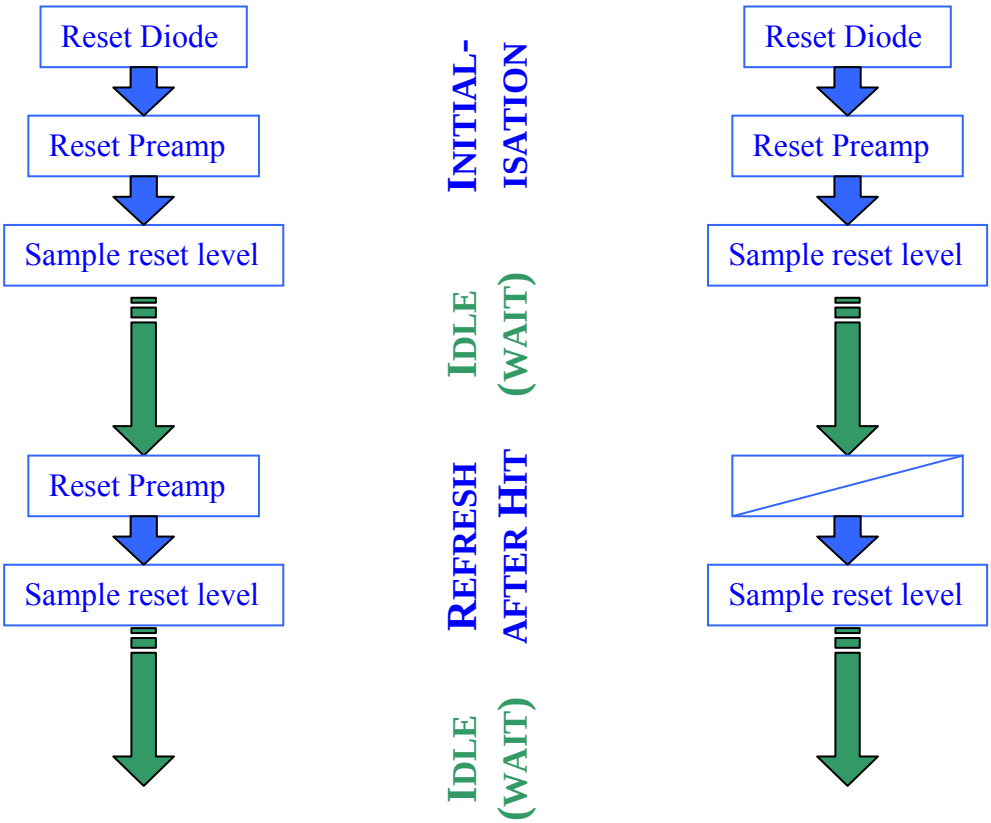
Above: Diode leakage contributes to a slow rise in the signal output over the 2ms.

Diode leakage in simulation is defined by the Gmin parameter which often results in misleading waveforms. Measured leakage results provided by the Foundry suggest that the leakage on the diode seen here is at least one order of magnitude greater than their pixel design (different diode size and implants).

The high gain of the amplifier in the preamplifier means this represents a significant error. If the actual diode leakage in the manufactured devices is significant (ie of the order suggested in this simulation) then a periodic reset or re-sampling of the reset level would be necessary to keep the signal error small. If the order of magnitude reduction is achieved as indicated by data provided, an error of 5mV across the duration of the full bunch train could probably be accepted?

PreSample Pixel simulation: Reset Sampling Errors

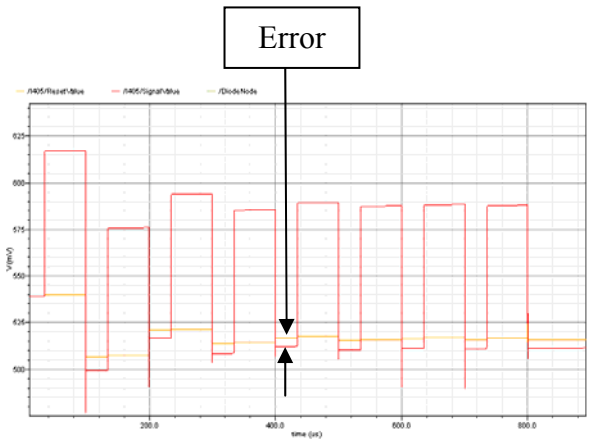
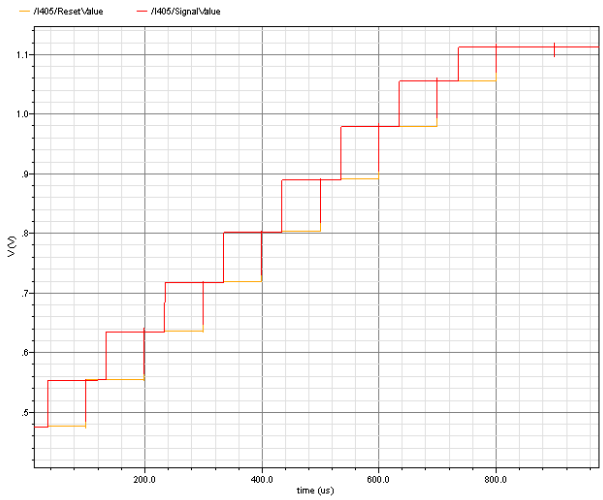
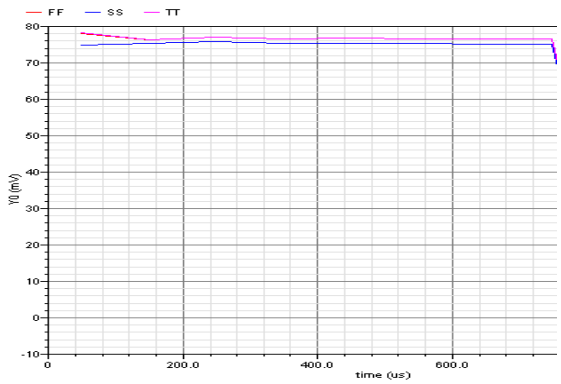
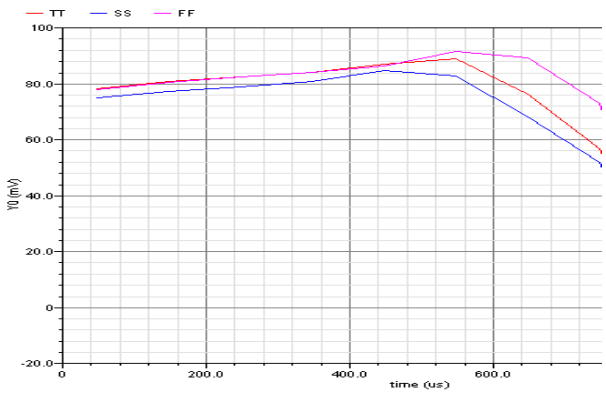
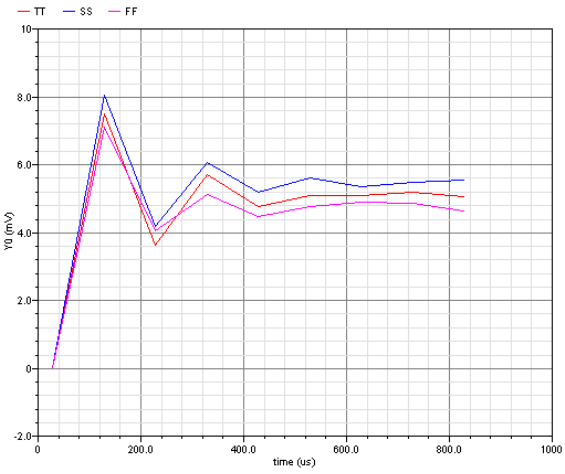
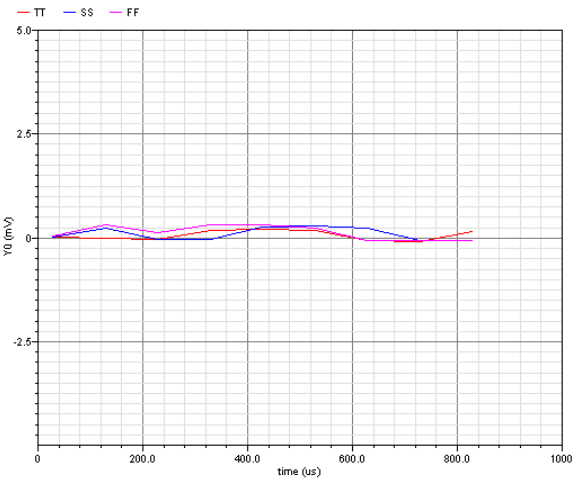
Two possible modes of operation are considered (these are illustrated by flow diagram below, and with waveform plots on the next page.



When the preamp is reset after a hit, the sampling of the reset level is subject to some error when squeezed into the 150ns timing window. Therefore the first reset sample is generally more accurate than those that follow a hit. This introduces an error to the (signal-reset) value that is compared with the threshold that applies to subsequent hits, if any.

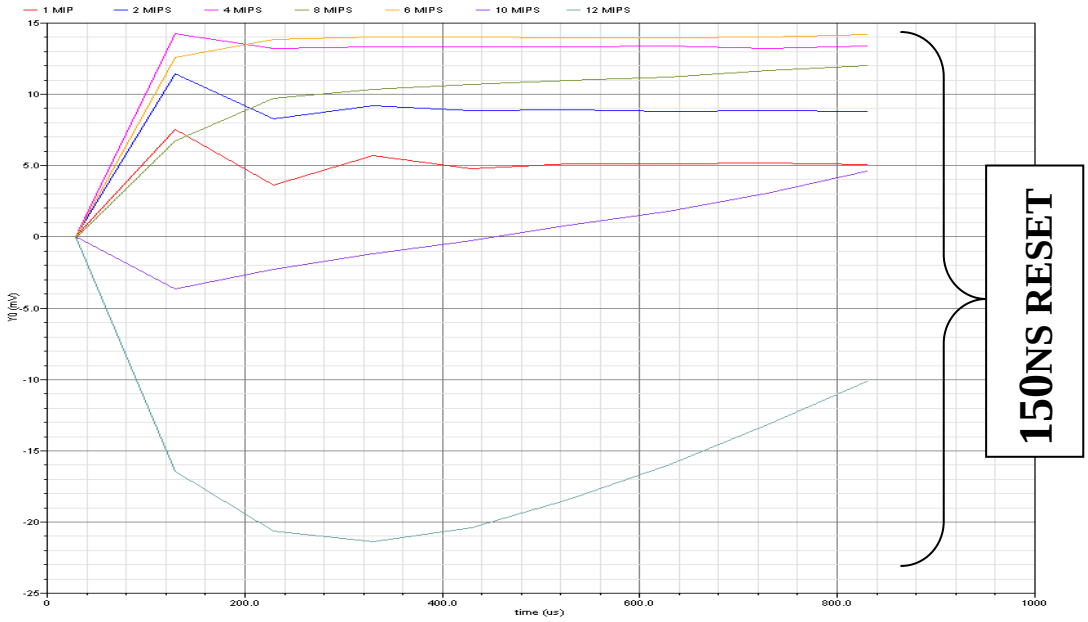
If the preamp is not reset, then its output reaches saturation quickly, with variation in gain approaching this point introducing errors in the signal magnitude.

Maximum signal to saturation defined by non-reset diode full-well capacity, order of 12,000 electrons	Maximum signal to saturation approx 7 MIPs, ie ~1800 electons
Signal error ~3mV	Signal error ~20mV
Reset sample error <9mV *(150ns timing, 10 MIP signal max)*	Reset sample error <0.5mV

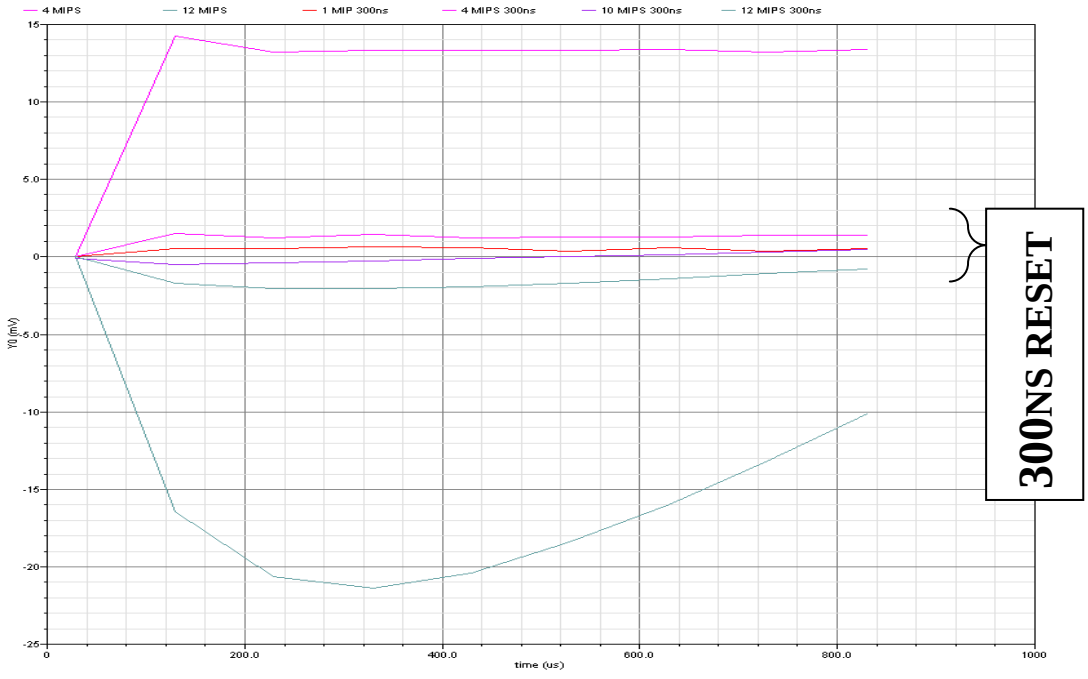
Preamp is reset; new sample is taken	Preamp remains active; new sample is taken
	
Transient Waveforms	
	
Signal magnitude	
	
Error between reset sample and signal prior to hit	

The signal & error graphs are created by sampling the transient waveforms at 100us intervals; so each of the 8 points plotted (and joined) represent a hit in the sequence.

Unfortunately the error introduced by resetting the preamplifier after a hit is not consistent, and varies depending on the magnitude of the previous signal.



Note that the first sample is near-perfect – this is because the preamplifier has sufficient time to settle before the reset sample is taken. The error develops because the preamplifier output is still moving at the moment the reset sample is taken. Allowing 300ns instead of 150ns to take this reset sample dramatically reduces these errors, illustrated below, with the two extreme cases from the above graph included for comparison. The maximum error is now ±2mV.



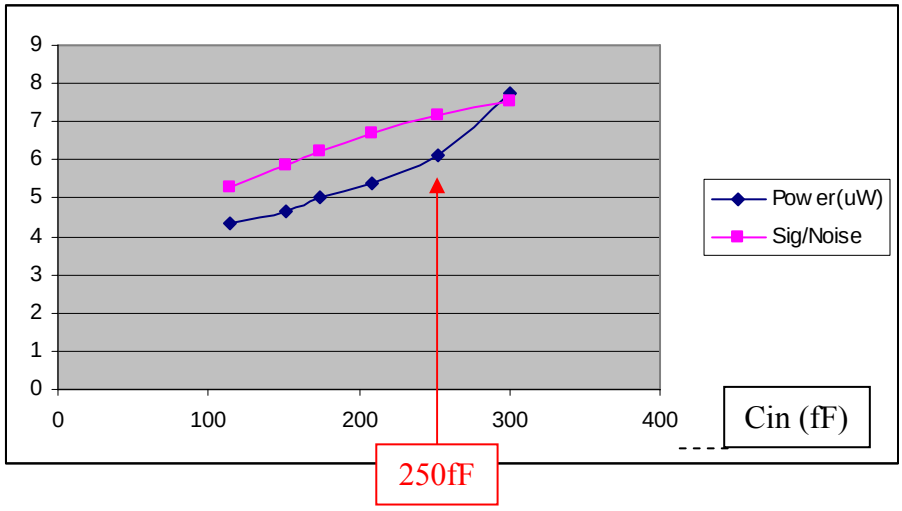
PreSample Pixel simulation: Power consumption

Pixel Source follower	Charge (Pre)amplifier	Output Source Follower	Comparator (in-pixel)	Comparator (off-pixel)
1.8v	1.8v	1.8v	1.8v	1.8v
0.9uA	1.3uA	1.2uA	1uA	750nA
1.6uW	2.4uW	2.2uW	1.8uW	1.3uW

Total power consumption = 9.3uW

The in-pixel comparator current may be reduced to match desired speed of operation with the line capacitance between the pixel and the logic – see the comparator results document for more details. The figures quoted here were those used to produce the results in this document (unless otherwise stated).

During the design process it was identified that the decoupling capacitor between the input source follower and the charge amplifier had the dominant effect on noise and also signal, but larger values required more power consumption to operate correctly. The following graph illustrates the results of this study:



The Cin=250fF case was chosen as the optimum – beyond this point the power consumption starts to rise significantly for little improvement in signal-to-noise. If a lower signal/noise were acceptable then the power could be reduced by maybe 2uW – but note that this is a design-time decision, since the value of Cin must be selected accordingly.

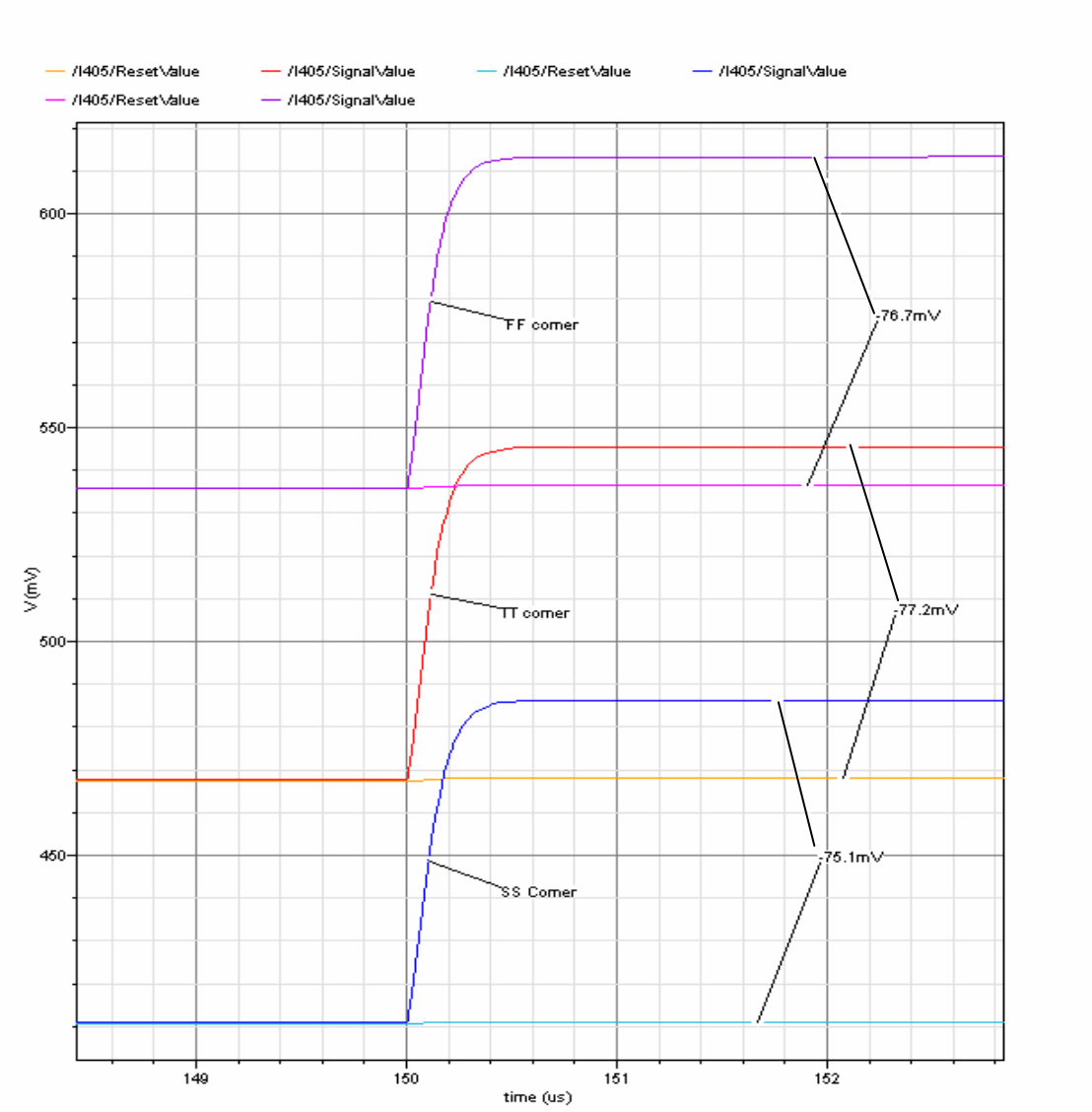
The figures quoted for power in this graph exclude the comparator, and therefore relate to the sum of the first three columns in the table above only. Noise is considered as sqrt(2) times that measured at the output of the "output source follower".

PreSample Pixel simulation: Process corner variations

Circuit stimulus/scenario

Transistor process corners are explored: 1 MIP signal (250 electrons).

Results waveforms



Above: Pulse height for the process corners is very consistent. Three corners are plotted for clarity, but results from all 5 corners are tabulated below. (Note that device corners exclude variations to feedback components, ie resistors and capacitors. These are considered separately in the manufacturing risks section).

	SS	SF	TT	FS	FF
MIP signal: (preamp pulse height) – (sampled reset value)	75.1mV	76.4mV	77.2mV	77.4mV	76.7mV

PreSample Pixel simulation: Noise Analysis

Circuit stimulus/scenario

Standard noise analysis is shown to illustrate the dominant noise sources in the circuit. Noise is measured at the shaper output / input to comparator. The pixel circuit is modified for noise analysis as follows

a) The reset transistor is disconnected from the diode, which is biased to 1v with an ideal voltage source
b) The preamplifier reset switch is replaced with a 1Tohm resistor to correctly set the DC operating point.

Results

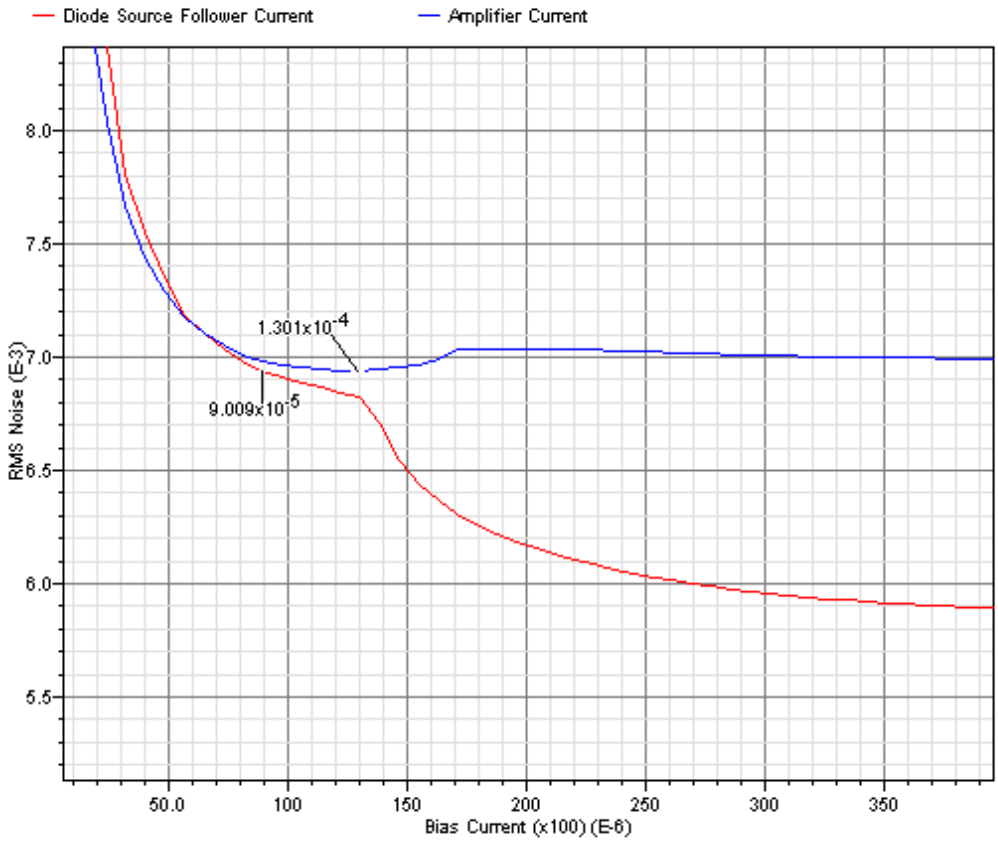
```
/I405/M3        id        0.0038202              30.31
/I405/M1        id        0.00350354             25.50
/I405/M1        fn        0.00310834             20.07
/I405/M2        id        0.00194574             7.86
/I405/M3        fn        0.00186377             7.22
/I405/M5        id        0.000857296            1.53
/I405/R0        rn        0.000817511            1.39
/I405/M7        id        0.000697706            1.01
/I408/M110      id        0.000647459            0.87
/I405/M5        fn        0.00064119             0.85
/I405/M6        id        0.000576871            0.69
/I408/M33       id        0.00057487             0.69
/I405/M2        fn        0.000420118            0.37

Integrated Noise Summary (in V) Sorted By Noise
Contributors
Total Output Noise = 0.00693863
```

The dominant noise sources are found to be the input devices in the diode source follower (M1) and the amplifier (M3). Contribution from R0 can be ignored.

Due to the sampling nature of this pixel architecture the noise seen at the output of the pixel circuitry must be considered twice, since it will be sampled on the reset-storage capacitor, and will be considered again at the other input to the comparator, thus a factor of $\sqrt{2}$ should be applied when evaluating signal/noise.

Noise in the two dominant input devices can be adjusted with bias currents. The plot below illustrates how the noise varies with the current flowing in the diode source-follower and also the preamplifier. The chosen bias points are indicated in the graph that relate to the 6.9mV figure quoted in the table above. There is still some benefit in increasing the current in the diode source follower, adding a further 2uW to the power consumption of the pixel would reduce the noise by ~0.7mV; this can be evaluated during the testing phase.

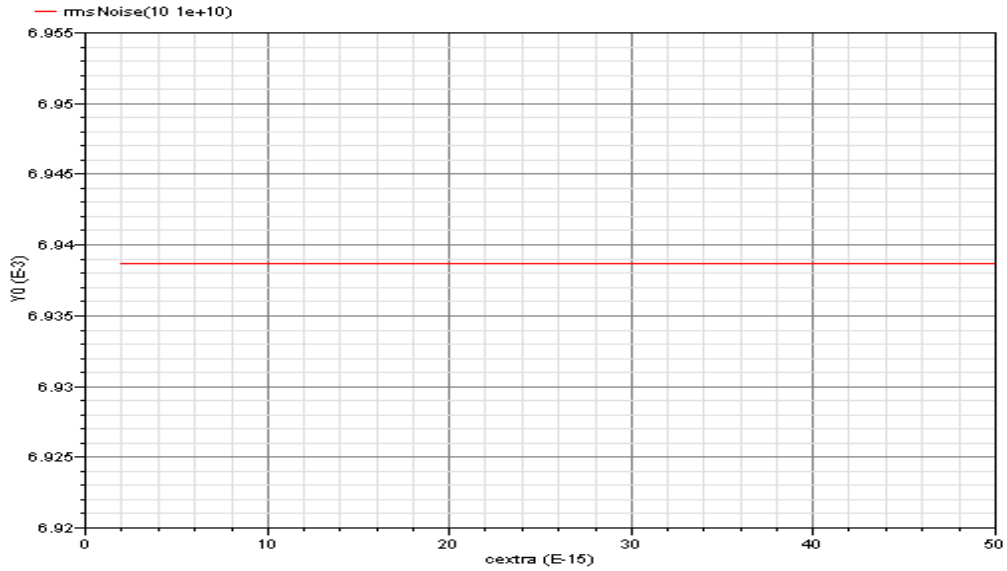


PreSampe Pixel simulation: Signal Vs Input Capacitance

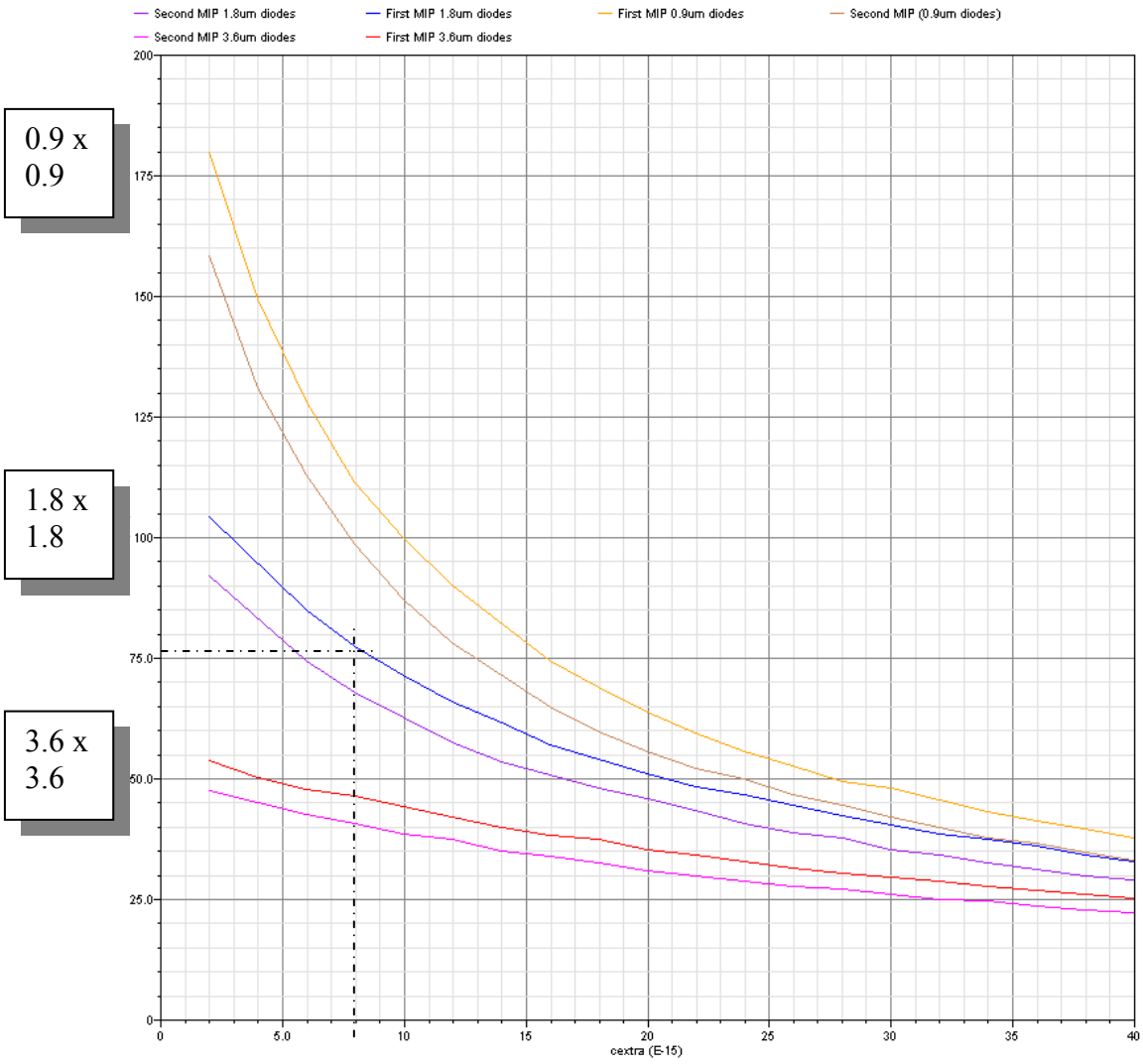
Circuit stimulus/scenario

Noise in pixel circuits is independent of the capacitance at the input node. However, the signal magnitude will be strongly dependant on the input capacitance, so it is this effect that should be investigated to plot signal/noise versus input capacitance.

Results waveforms



Above : Simulated noise at the input to the comparator with varying parasitic capacitance on the diode node.



Above: Signal (measured as difference between signal output and reset sample) as varies with the capacitance at the input node:

- The input signal is constant 1MIP=250 electrons.
- First and second MIP have been included to illustrate the effect of the reset sample error in this context.
- Square diodes of sizes 0.9, 1.8 and 3.6 micron have been simulated.

All other simulations in this document have been produced using value of Cextra=8fF and diodes measuring 1.8x1.8um, as indicated on the waveform above, yielding the 1MIP signal of ~75mV.

PreSample Pixel simulation: Transient Noise

Circuit stimulus/scenario

Results waveforms

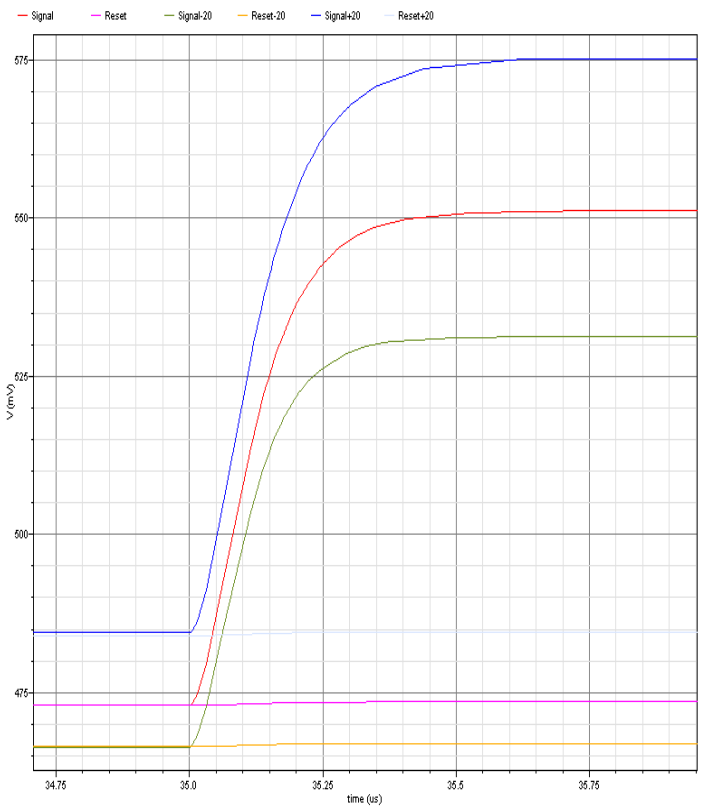
TO FOLLOW
UNBELIEVABLE RESULTS FROM SPECTRE SIMULATION

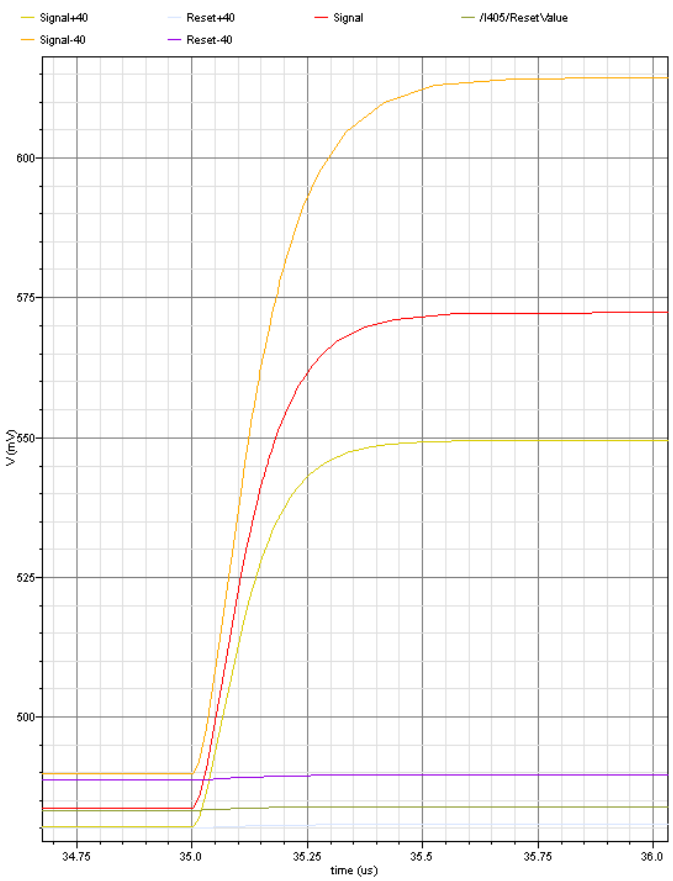
PreSample Pixel simulation: Matching/Manufacturing Risks

Circuit stimulus/scenario

Each passive component in the preamp and shaper circuit is varied individually to check the dominance of their value on the signal pulse. Those components that have the largest effect will contribute most to mismatch between pixels and should be most carefully considered during layout. [Those considered high risk have been evaluated ±40% and those with less expected effect ±20%]

Results waveforms

Preamp **Cin**		250fF +20% -20% Defines signal gain (ratio with Cpre) but is the larger, therefore less dominant player, matching should be good for large area device <u>Medium risk</u> **= (sig)±17%** *Note that larger Cin may need larger bias currents to operate the pixel correctly.*

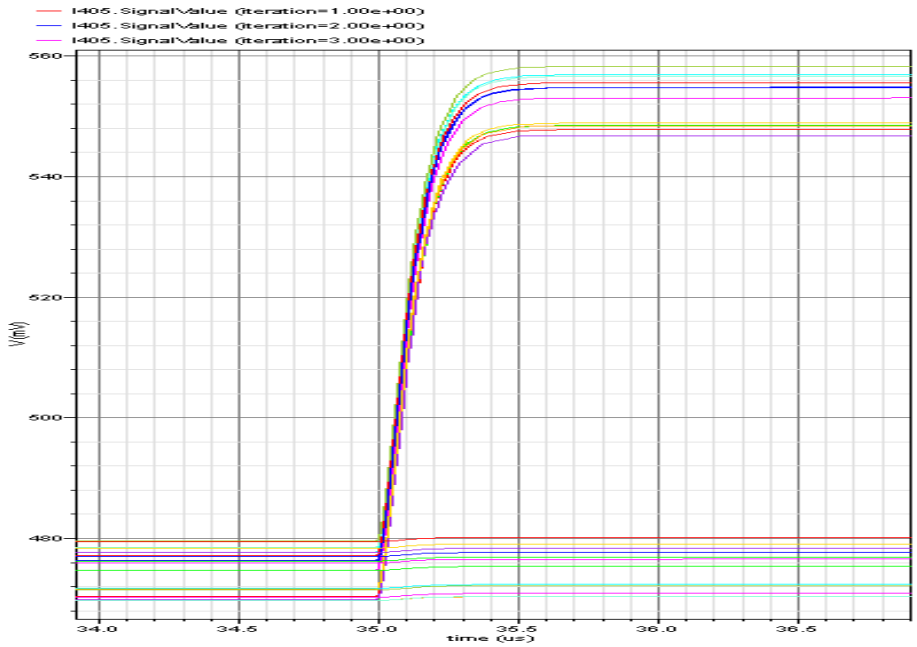
Preamp **Cpre**		3.6fF +40% -40% Critically defines signal gain (ratio with Cin). Matching of small capacitance will be poor, and effect on signal is significant: <u>High risk</u> Matching may be improved using two 7fF devices in series **= (sig)±30%**
Sample **Cstore**	The value of this capacitor would have no effect on the magnitude or accuracy of the reset sample. Variation of this value would affect the lifetime of the reset sample, and the time taken to charge/discharge, potentially adding further error to the final signal if the output source-follower were incorrectly biased [easily adjusted in test setup].	200fF +20% -20% <u>Low risk</u>

PreSample Pixel simulation: Mismatch

Circuit stimulus/scenario

Monte-Carlo simulation varies component parameters according to statistical models: Typical process corner; 1MIP (250e) input signal.

Results waveforms



[12 runs]	**Signal-Reset Sample**	
	First MIP	**Second MIP**
Mean	77.3mV	68.2mV
Std Deviation	0.78mV	0.81mV

These preliminary results from 12 runs show good matching between mismatch cases, indeed the error introduced by the reset sequencing is much more dominant than those caused by badly matched transistors.

This result is not surprising, since gain mismatch in the amplifier should not affect the charge gain (set by ratio of capacitors), and source-follower buffer stage gain would also be largely unaffected by mismatch.

→ LONGER MONTE-CARLO AND CORNERS TO FOLLOW (lengthy simulation results unavailable at time of writing)

PreSample Pixel simulation: Comparator Output

Circuit stimulus/scenario

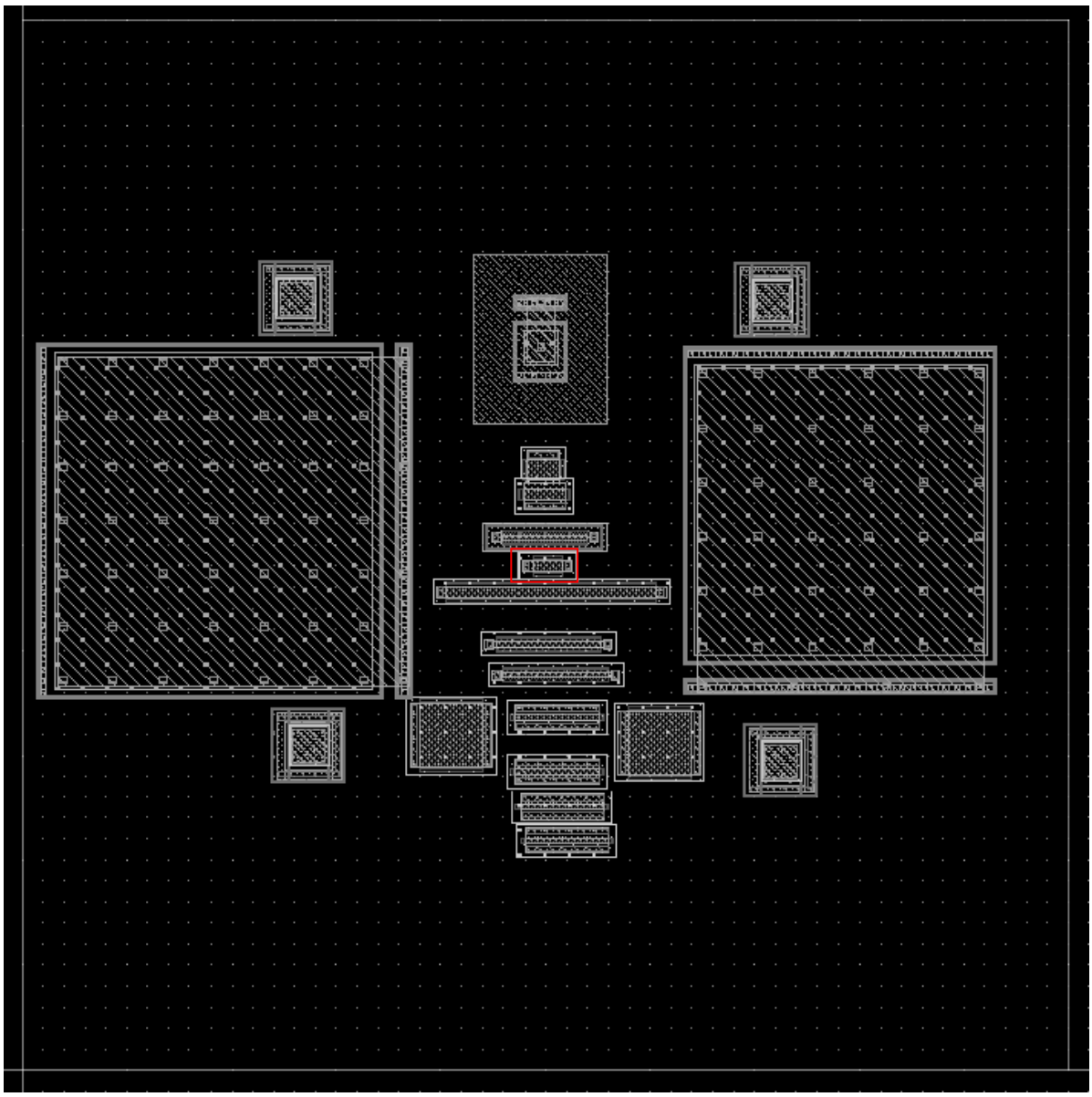
The in-pixel comparator uses only nmos devices, but this yields very low gain, hence the differential signals are effectively the output from a differential amplifier with low gain (approx 3), with a small additional noise contribution, but also some noise filtering.

Results waveforms

TO FOLLOW

Pixel Layout Placement

The plot below is a quick placement of all the pixel components in a 50 micron pixel boundary to check that they will fit. The large capacitors will dominate the pixel area, but there is sufficient space for careful placement. The central NWELL consists of a single PMOS transistor and well contact, which should fit into a 3.5x3.5 micron square: At present the transistor is long and thin, instead of a square, requiring an nwell measuring 1.3x6.3um – perhaps the diode placement could be optomised for this shape NWELL rather than using additional NWELL area to split the transistor into parallel fingers?



Issues Outstanding

- AC analyses of each circuit block
- Comparison against signal (collected charge) results to establish true suitability in signal/noise.
- Renato to try to reduce noise further, and verify noise simulation results with Eldo simulator
- Renato to simulate transient noise to investigate concerning equivalent simulation from spectre (unreliable?)
-