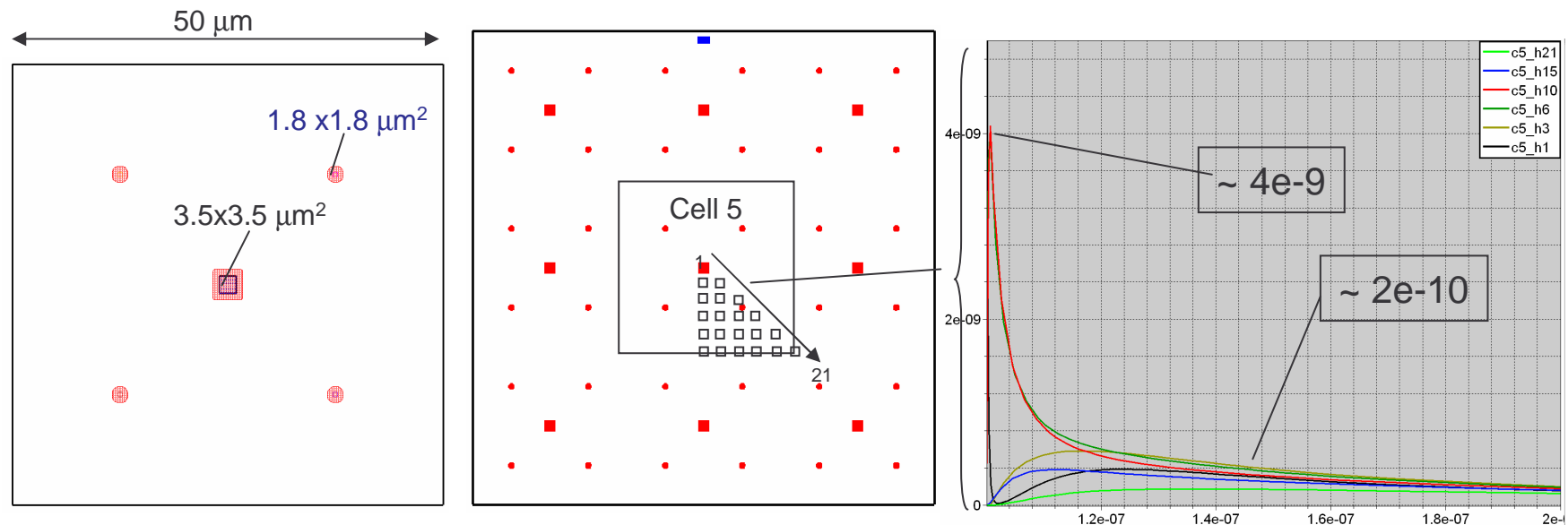# CALICE simulation results

G.Villani oct. 06

Progress on CALICE MAPS detector simulations:
- S/N analysis for recent results
- Optimization: discussions & conclusions
- Conclusions

CALICE simulation results

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50 μm

1.8 x1.8 μm^2

3.5x3.5 μm^2

Cell 5

1

21

~ 4e-9

~ 2e-10

Legend:
- c5_h21
- c5_h15
- c5_h10
- c5_h6
- c5_h3
- c5_h1

4e-09

2e-09

0

1.2e-07   1.4e-07   1.6e-07   1.8e-07   2e-0

Pixel layout

Transient   I$_d$

- 1.8 x 1.8 μm^2 diode size

- 21 hits simulated, 5 μm pitch

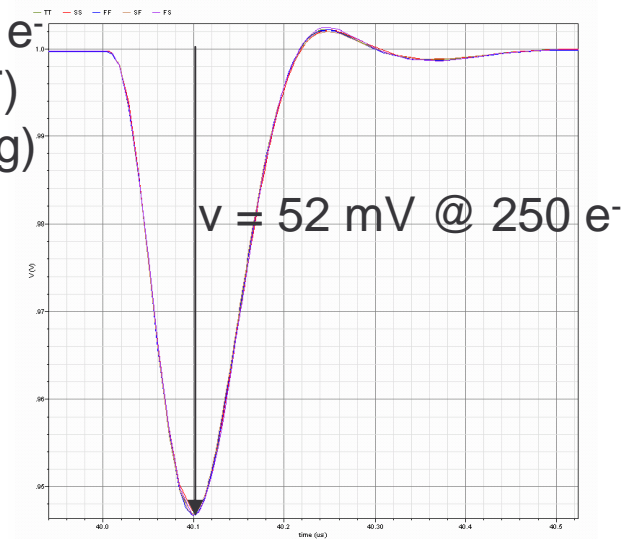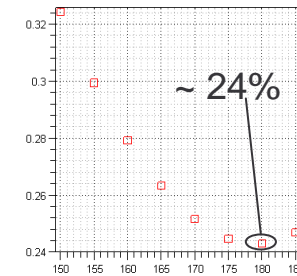- 121 extrapolated hits / pixel

- 961 extrapolated hits / cell

Bias
- Diode : 1.5V fixed
- Nwell: 3.3V
- Pwell: 0V
- Subs: floating
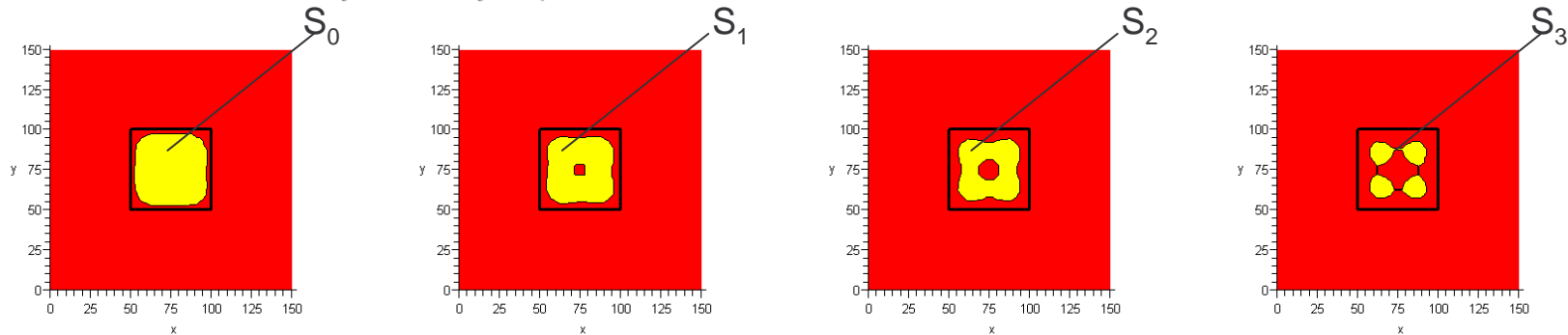
2

CALICE simulation results

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- $v = 52$ mV @ 250 e^-
- Noise $= 12$ mV (8 fF)
- S/N $= 4.33$ ($Sg = Ng$)
- $e^-_{in} \sim 57\ e^-$

~ 24%

$v = 52$ mV @ 250 e^-

S/N @ 150 ns can be increased by increasing the threshold. This reduces the effective pixel area (however it could be 'recovered' by the n layers)

S_0 S_1 S_2 S_3

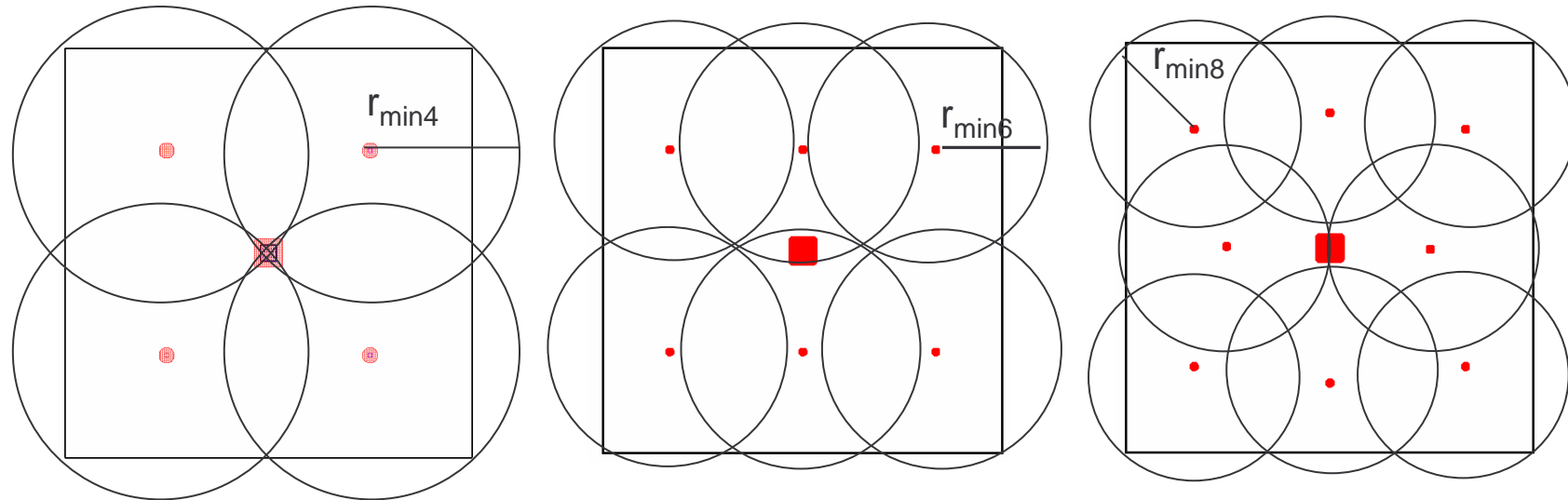Q_{thr} 225 => S/N ~ 4 Q_{thr} 250 => S/N ~ 4.4 Q_{thr} 275 => S/N ~ 4.8 Q_{thr} 300 => S/N ~ 5.2

Simulations for 3.6 in progress. However, achieving a S/N exceeding 10 for a reasonable pixel size seems to be very difficult with the current layout

CALICE simulation results

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r_{min4}

r_{min6}

r_{min8}

4 diodes   6 diodes   8 diodes

Layout optimization

q Improved diodes placement (minimum circle covering)

q The approach is to arrange the diodes within the square (pixel) to <u>minimize the maximum distance from any point within the square to any collecting diode</u>

q Solutions available for some tens of diodes
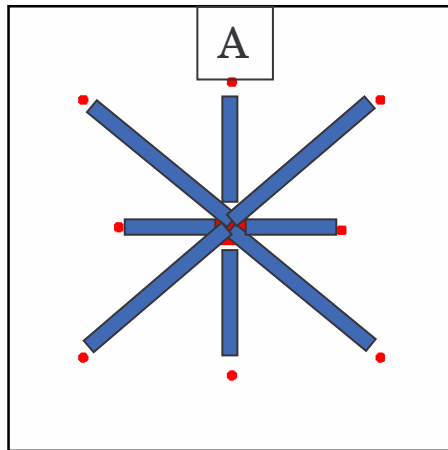
4

CALICE simulation results

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Nr$_{diodes}$ Size(μ)	4	6	8
0.9	2.54;17.2	3.81;14.55	5.08;12.55
1.8	10.17;16.75	15.26;14.1	20.35;12.1
3.6	40.7;15.87	61.06;13.2	81.41;11.2

Collecting area (μ^2) and maximum collecting distance (μ) for 4,6,8 diodes layout

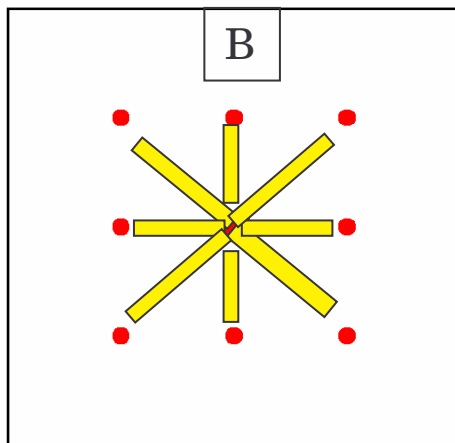# CALICE simulation results

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8 Diodes layout

A

- Σ lengths = 148.1

d_{max} = 12.55

Σ lengths [A] ~ 1.22 Σ lengths [A]

d_{max} [A] ~ 0.7 d_{max} [B]

B

- Σ lengths = 120.71

d_{max} = 12.5* 2

q 'B' better than 'A' for charge collection

q S/N :Noise [lenghts] needed

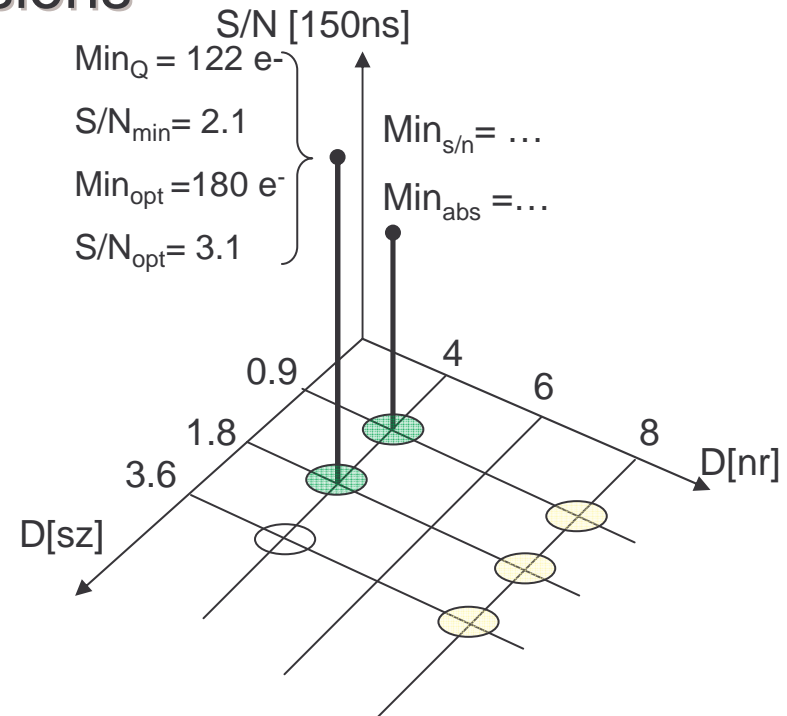| Σ lengths	4	6	8
0.9	70.7	108.3	148.1

q

6

CALICE simulation results

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Conclusions

- Increased diodes size to 1.8 x 1.8 μm^2 significantly improves charge collection performances.
- S/N achievable depends also on the % of area loss, but reasonable value seems to be ~ 4
- Increasing the diode size will help, but it is unlikely that S/N can exceed 10

S/N [150ns]

$Min_Q = 122$ e⁻

$S/N_{min}= 2.1$

$Min_{opt} =180$ e⁻

$S/N_{opt}= 3.1$

$Min_{s/n}= \ldots$

$Min_{abs} =\ldots$

0.9   4   6

1.8   8

3.6   D[nr]

D[sz]

Next step:

q Improvement in diode layout (i.e. 3.6 version and more diodes)

q To improve reliability of simulations (see above) it is strongly advisable to obtain process information

CALICE simulation results

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- Addenda: layout coordinates

- 8 diodes coordinates:
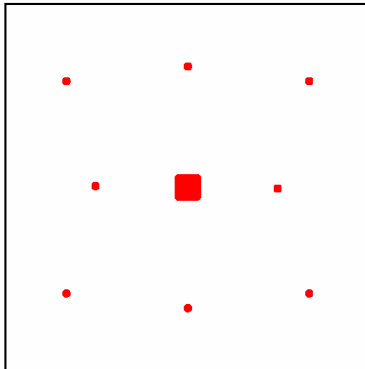
	10.45;42.2		39.55;42.2	
		25;37.65		
8.95;25				41.05;25
		25;12.35		
	10.45;7.9		39.55;7.9	