Tera-Pixel APS for CALICE

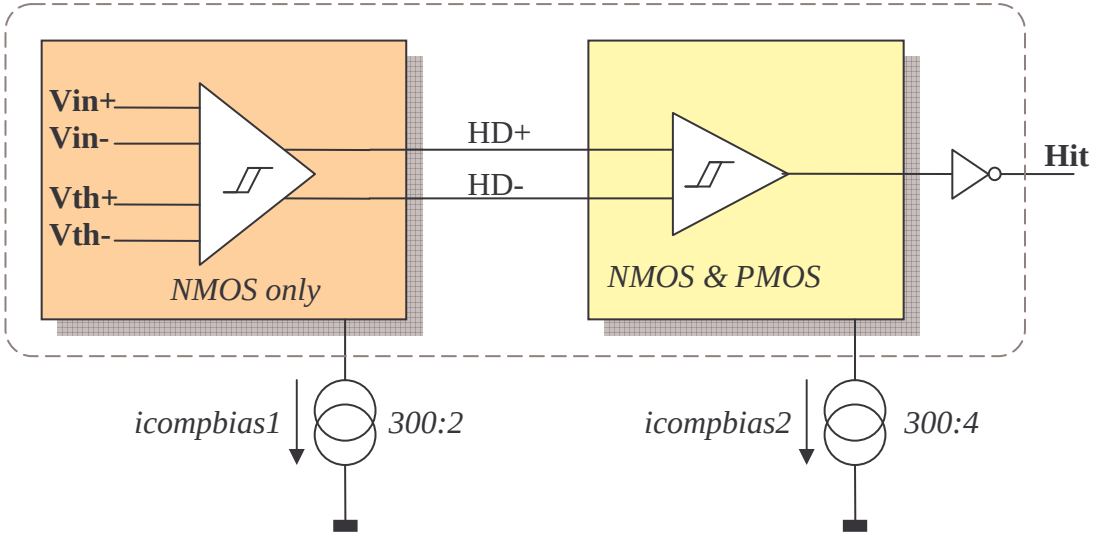
Progress

30th November 2006

Recent Activity

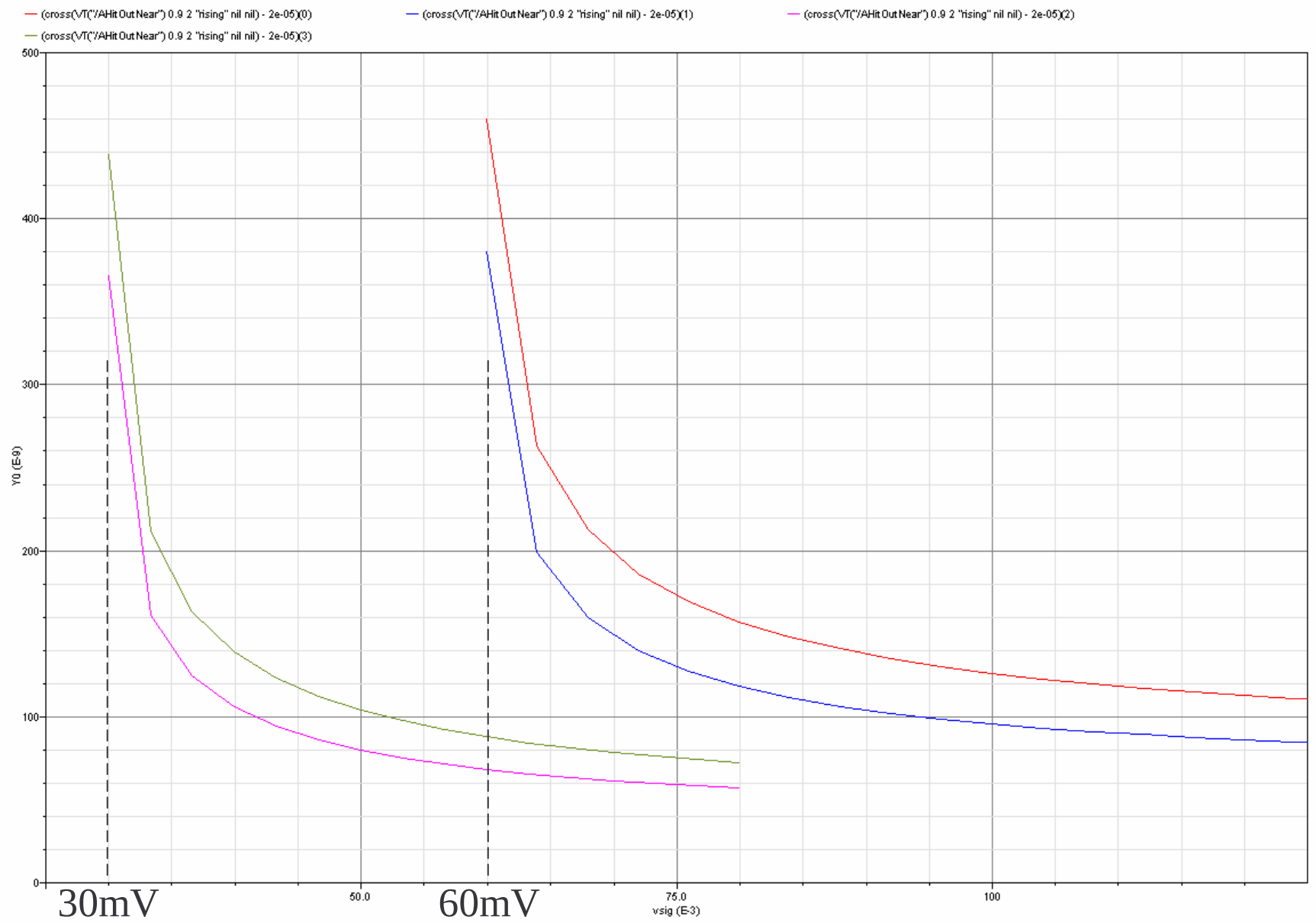
- Info from foundry
- Comparator fully characterised
- Monostable trigger

Comparator Overview

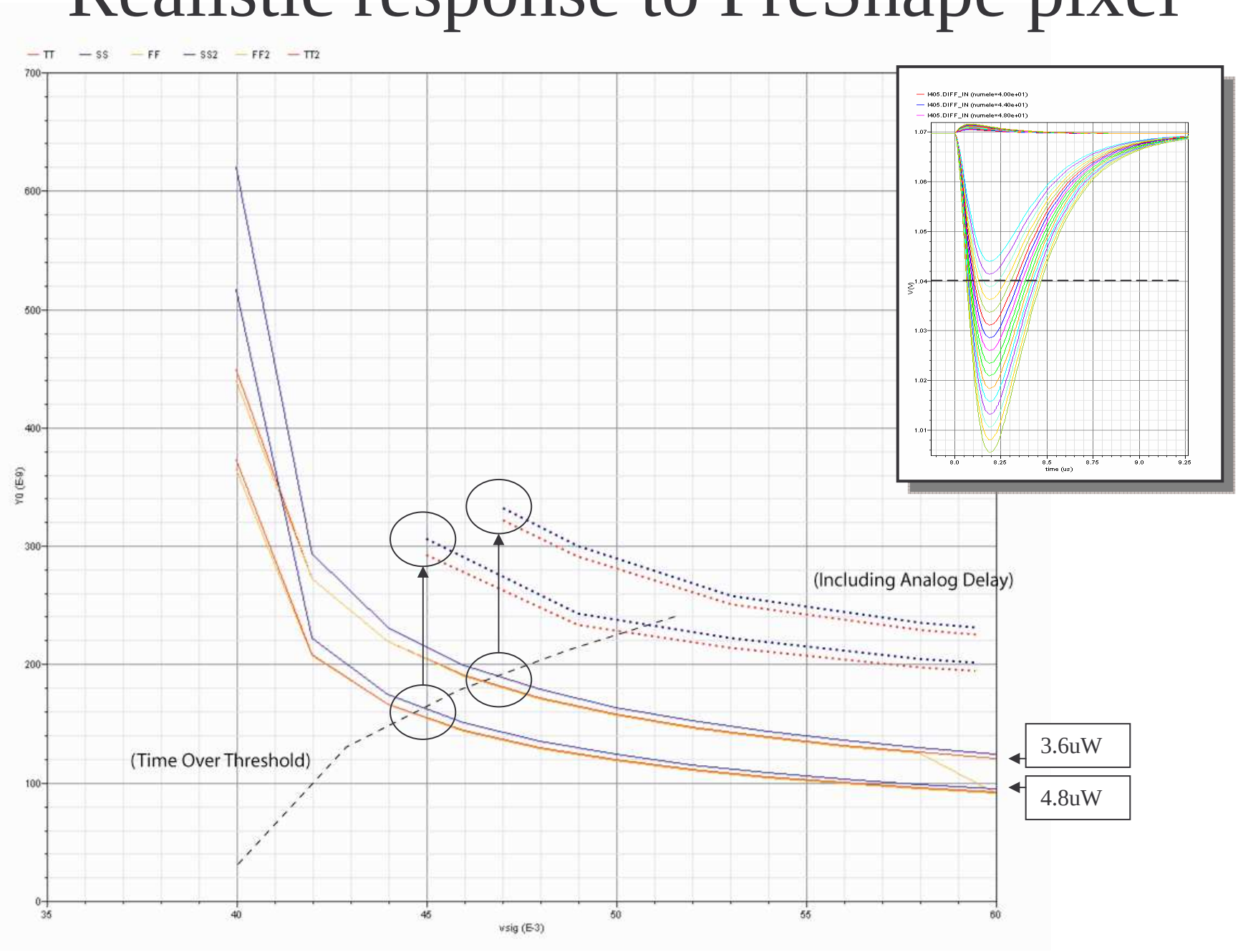


icompbias1	Current in each arm	Total current in first stage	icompbias2	Current in input stage (x3)	Current in output stage (x1)	Total current (both parts)	
100uA	333nA	666nA	100uA	1uA	333nA	2.0uA	3.6uW
200uA	666nA	1.33uA	100uA	1uA	333nA	2.6uA	4.8uW

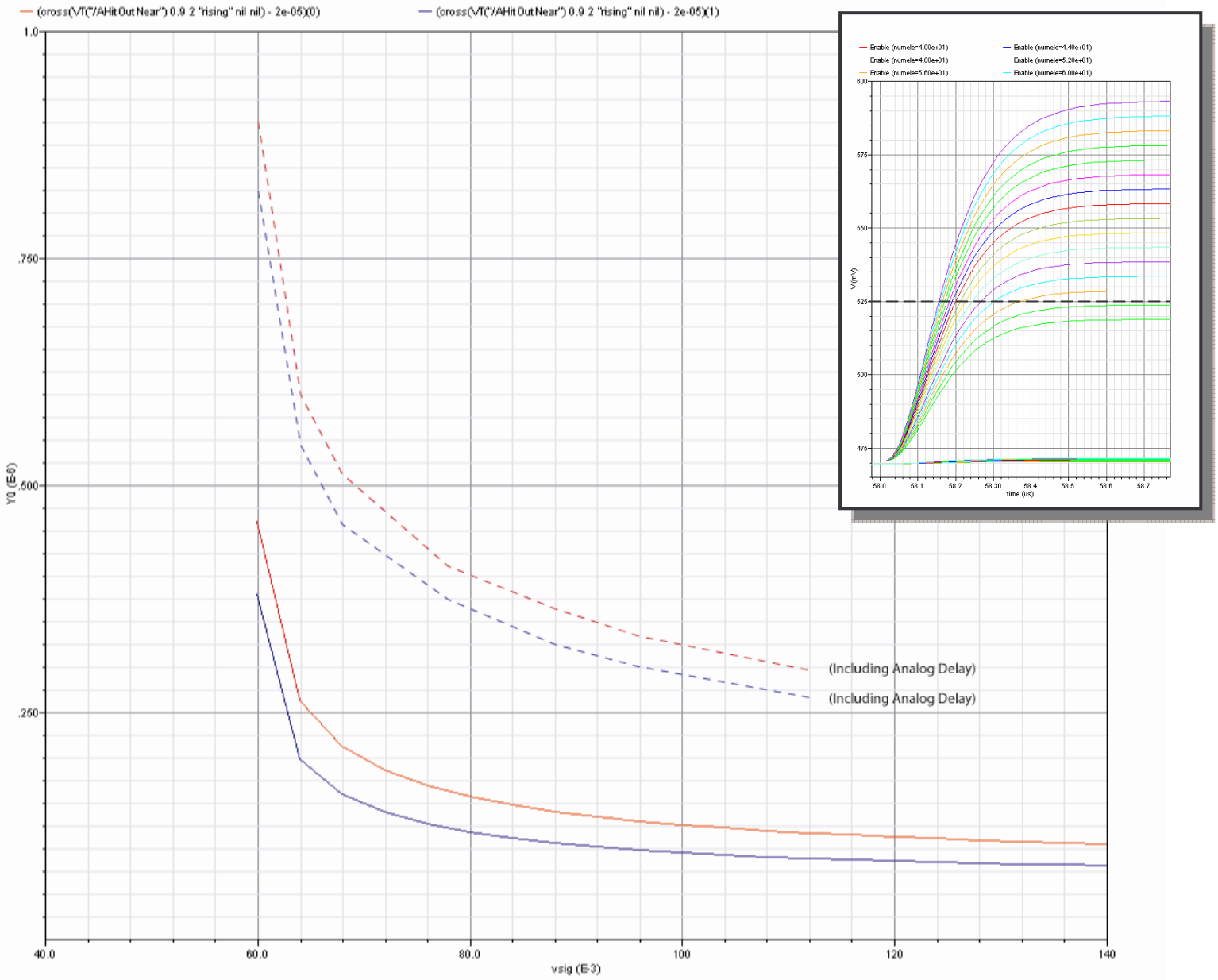
Comparator Response Time



Realistic response to PreShape pixel



Realistic response to PreSample pixel

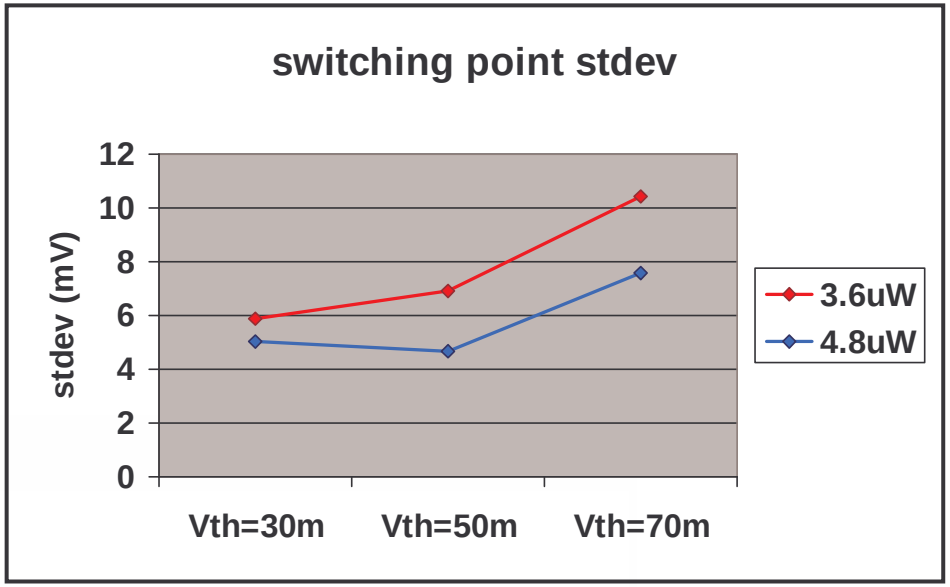


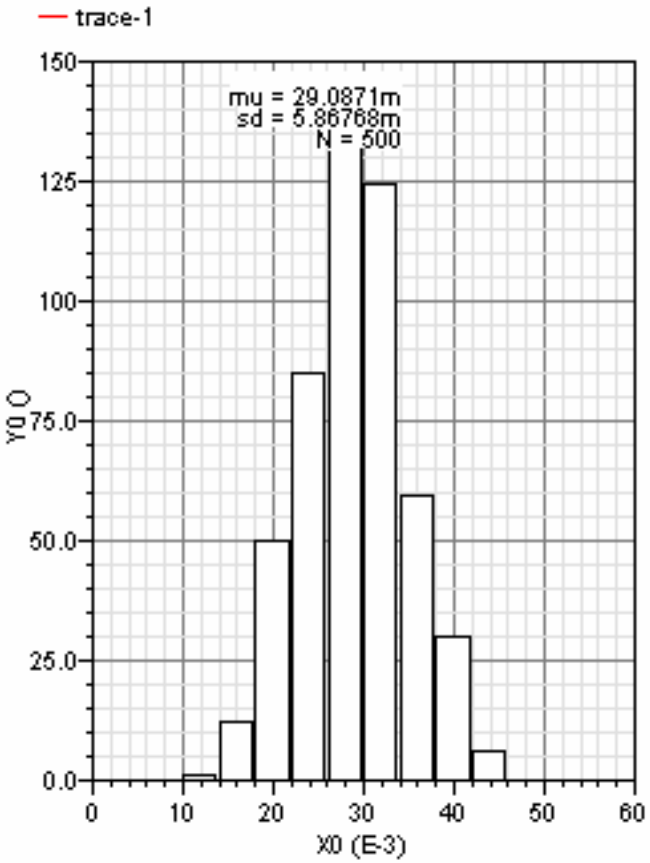
Noise

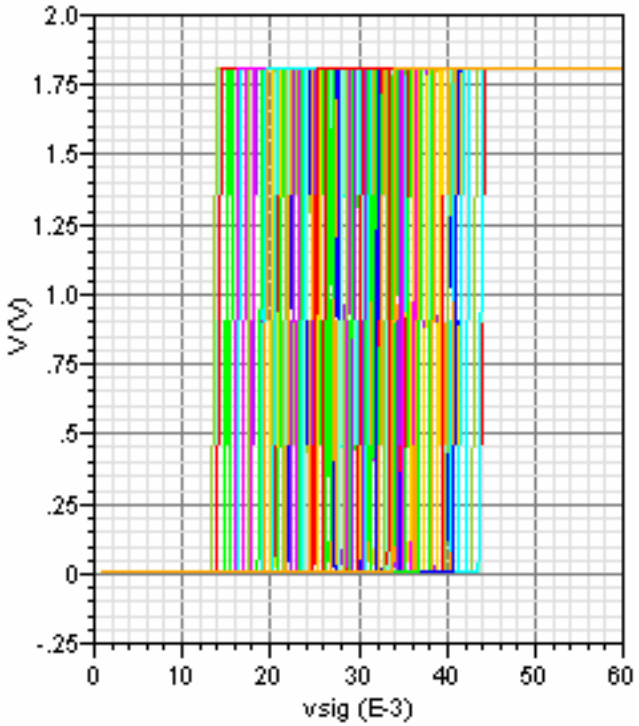
- Noise must be considered between the two comparator stages
  - it will be added to the signal before the high-gain second comparator stage.
- Several methods…
  - Hand calculations from standalone comparator and previous pixel simulations
    - PreShape noise addition 12e- yields ~27.7e-
    - PreSample noise addition 6e- yields ~27.5e-
  - Spectre simulations with analog pixel circuits
    - PreShape ~40e-
    - PreSample ~8e-
  - Eldo simulations with analog pixel circuits
    - PreShape ~27e-
    - PreSample ~21e-

Mismatch

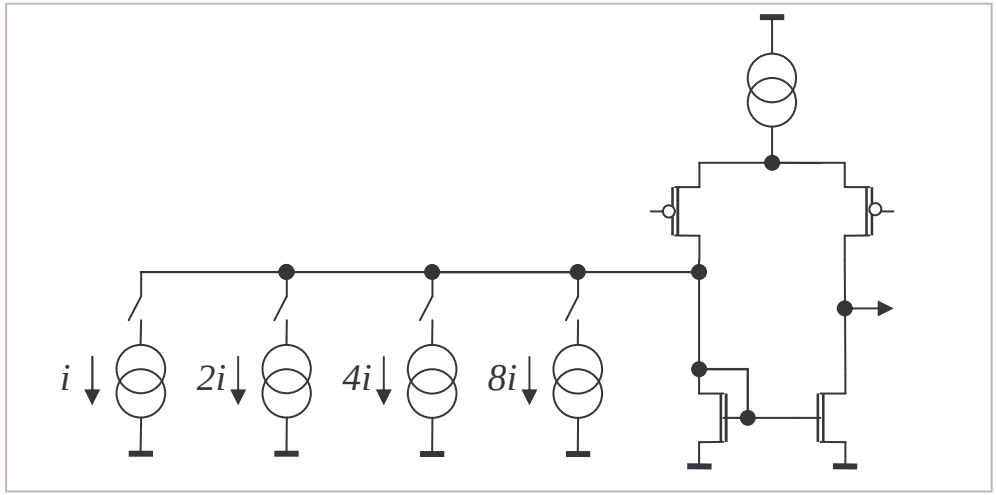
6mV mismatch ‘noise’
100ns spread in response time

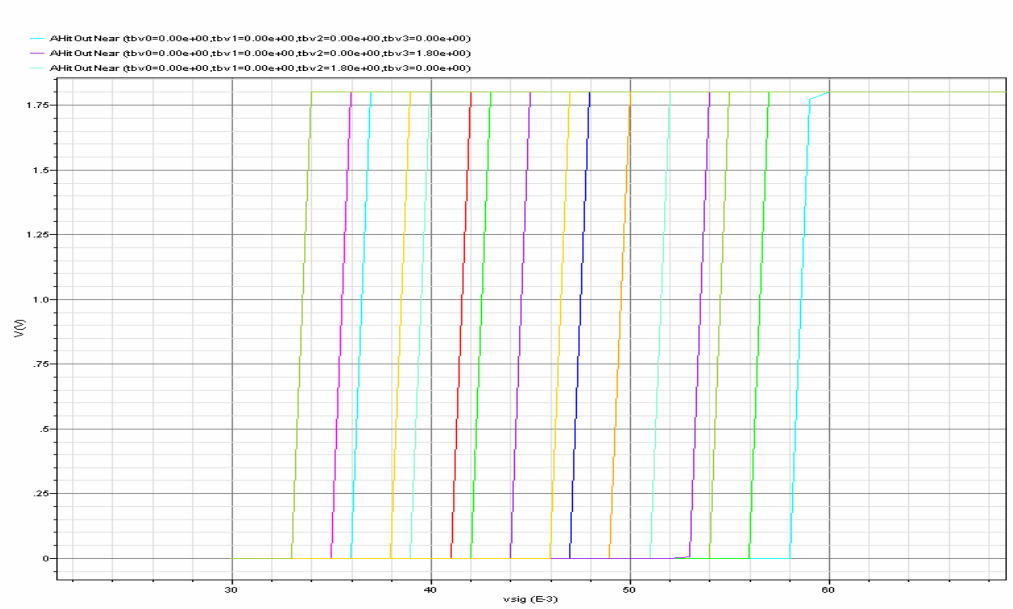




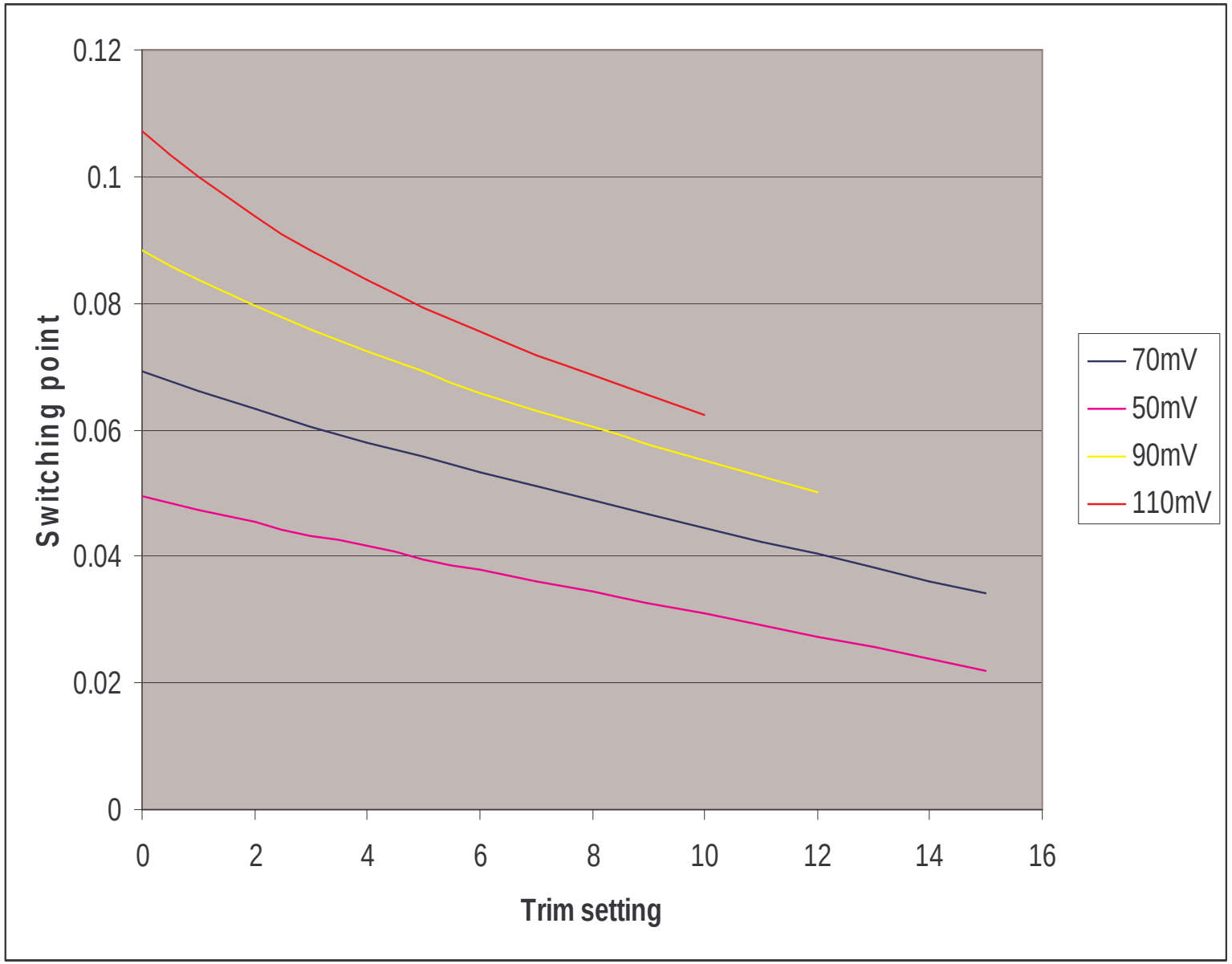


Threshold Adjustment

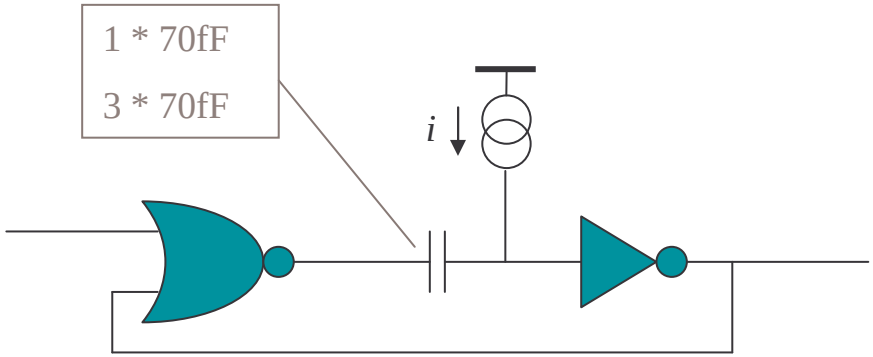


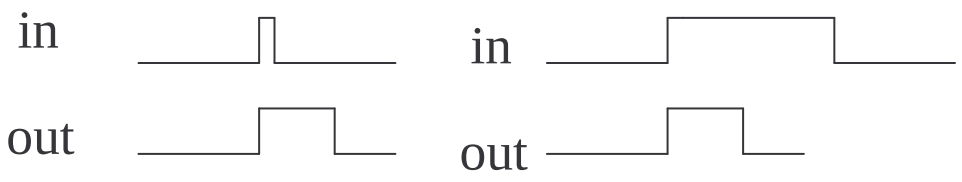


Threshold adjustment example



Monostable trigger





Bias current (i)	200ns monostable output	600ns monostable output
215nA	~250nS pulse	~750nS pulse
265nA	~200nS pulse	~600nS pulse
350nA	~150nS pulse	~450nS pulse

- Gives a well-defined length pulse
- External bias controls pulse length
- Can be used instead of edge-sensitive logic
- Can be used to sequence the self-reset of pre-sample pixels (3:1 ratio is required 450-600ns total reset time).
- Can draw a moderate current during switching (~25uA) so will be supplied with a separate power supply to avoid problems!

Next

- Full row simulations with logic
- Complete top level schematics for review