Novel Integrated CMOS Sensor Circuits

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***Abstract*—Three novel integrated CMOS active pixel sensor circuits for vertex detector applications have been designed with the goal of increased signal-to-noise ratio and speed. First, a large-area native epitaxial silicon photogate sensor was designed to increase the charge collected per hit pixel and to reduce charge diffusion to neighboring pixels. High charge to voltage conversion is maintained by subsequent charge transfer to a low capacitance readout node. Second, a per-pixel correlated double sampling kT/C reset noise reduction circuit was tested. It requires only one read, as compared to two for typical double sampling in active pixel sensors, and no off-pixel storage or subtraction is needed. The technique reduced input-referred temporal noise by a factor of 2.5 to a measured 15.6 e^-, rms. Finally, a column-level active reset technique was designed that suppresses kT/C reset noise. It reduced noise by up to a factor of 7.6, to an estimated 8.3 input-referred electrons, rms. The technique also dramatically reduces fixed pattern (pedestal) noise, by up to a factor of 21. This may reduce pixel-by-pixel pedestal differences enough to permit sparse data scan without per-pixel offset corrections.**

***Index Terms*—Active pixel sensor, active rest, correlated double sampling, kT/C noise, photogate, vertex detector.**

I. Introduction

RECENT work has demonstrated that standard CMOS active pixel sensors (APSs) [1] can be used to detect minimum ionizing particles with high spatial resolution and good signal to noise [2]–[8]. These use integrated sensors and readout circuitry (Figs. 1 and 2), generally using an epitaxial layer as a sensitive region, and APS-style readout. Diodes directly in the epitaxial region are used to collect charge from the physically continuous field-free region, allowing 100% spatial coverage. In this way, greater charge can be collected via diffusion from the thicker ($\sim$ 10-μm) field-free epi layer, as opposed to a typical CMOS diode cross section of 1 μm or less. The sensors are integrated with the readout circuitry and hence do not require wire or bump-bonding between the two. The advantages over traditional hybrid approaches are greatly reduced cost and the potential for vastly larger pixel counts and densities. However, challenges remain in terms of their signal-to-noise ratio (SNR) and readout speed and to obtain the benefits of sparse readout.

One target application is a new high-resolution vertex detector being developed for the STAR experiment at the Relativistic Heavy Ion Collider (RHIC) located at Brookhaven National Laboratory [9]. In this experiment, 100 GeV per nucleon Au beams are collided, producing thousands of particles. The purpose of the new vertex detector is to identify, within the thousands of tracks, those tracks that don't originate at the collision point. Those that originate a few tens of micrometers from the collision point come from short lived decaying particles, and isolating these tracks greatly improves the efficiency of their identification. In the case of STAR, the main particle of interest is the D meson. In this environment, with thousands of other tracks, the demands on the vertex detector are substantial. In order to get the best possible pointing accuracy, the detector will be located within 2 cm of the collision point in a region of high track density, thus requiring high pixel density. Currently the main limitation of these devices in the STAR application is

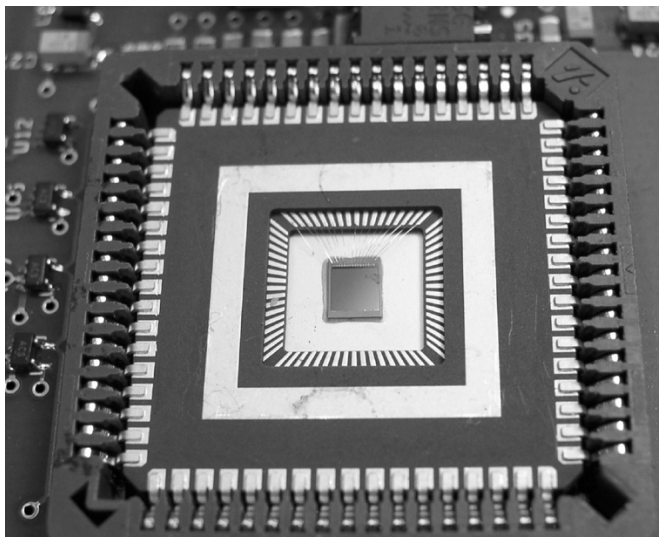

Fig. 1. Prototype CMOS sensor array for charged particle detection.

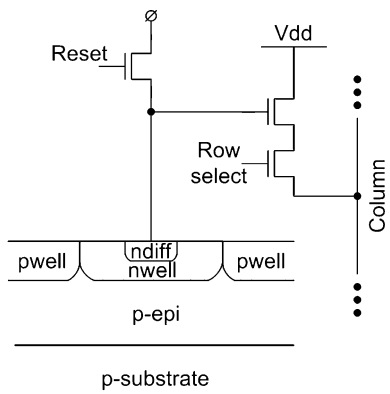

Fig. 2. Basic three-transistor active pixel sensor schematic showing a physical representation of the n-well/p-epi diode.

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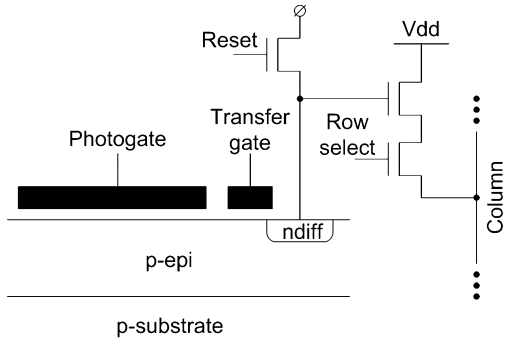

Fig. 3. Native epitaxial silicon photogate circuit. This version includes an active area only (no diffusion or field-oxide) between the photogate and the transfer gate.

read-out speed. Since in the STAR experiment the fraction of pixels that are hit is small—less than 0.5%—there is significant potential for improvement through on chip zero suppression.

In response to these challenges, this paper presents three circuits that attempt to increase SNR, reduce readout overhead, and to progress toward practical sparse readout.

II. Native Epitaxial Silicon CMOS Photogates

One problem with the use of CMOS APS is that the photodiode node must have small capacitance in order to obtain high charge to voltage conversion gain. This requires that the area of the photodiode be kept small, and hence a given diode will pick up only a fraction of the total liberated charge—a contradictory tradeoff. The remaining charge will diffuse to a region of neighboring pixels or will recombine, significantly lowering the SNR of the system.

The use of a CMOS photogate, as opposed to a photodiode, may improve this situation. A photogate resembles one bit of a CCD. An example photogate pixel schematic is shown in Fig. 3, and 4 shows a layout of a photogate pixel. The large area covering most of the pixel is the photogate (PG) transistor. The upper right-hand corner shows the transfer gate (TX) and readout circuitry. Electrons created in the epi layer can eventually diffuse to a broad field region created directly below the large area photogate, which is biased at a higher voltage. They are held there until the photogate voltage is dropped to below the transfer gate voltage, at which point they migrate to the higher voltage, lower capacitance, readout node. The readout node must be reset periodically and the photogate must be cycled regularly to keep the region directly under the photogate depleted.

In principle, the photogate can deliver higher local charge collection by virtue of its large area, which increases the probability that charge liberated by a local hit will be collected on the gate. It also maintains high charge-to-voltage conversion gain due to its subsequent charge transfer to a low-capacitance readout node. Photogates can also make CDS more convenient, since they eliminate the requirement, in APS, for complete frame storage of the first sample. Instead, two reads, one right before charge transfer, and one afterward, can take place within the readout of one row of pixels. Only one row of storage is necessary, though two reads and subtraction are still required.

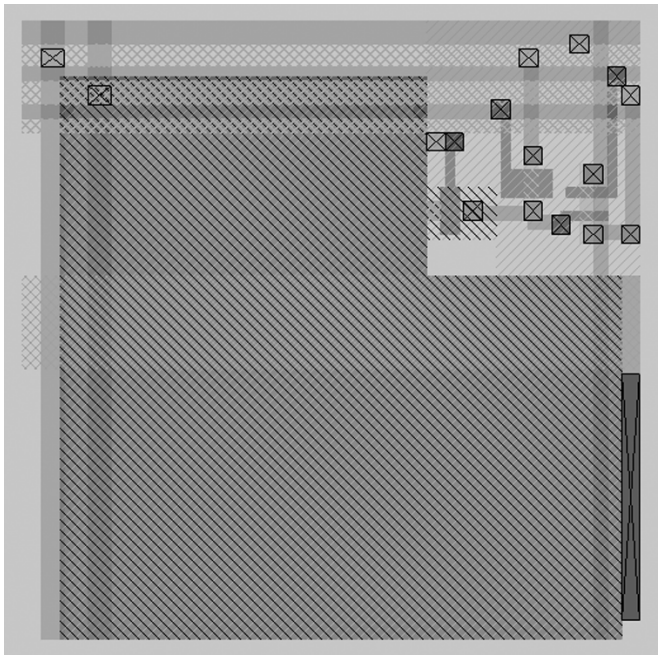

Fig. 4. Example photogate pixel layout. The large shape is the photogate, while circuitry in the upper right corner includes the transfer gate, reset, and readout transistors.

Our photogate structure differs from the standard CMOS photogate in several ways. It is a "native epitaxial silicon photogate" in that it is constructed directly in the higher resistivity epitaxial silicon instead of lying in a p-well, as would be typical in optical applications. As with the epitaxial-silicon photodiodes, this permits the photogates to collect charge from the thicker, continous, epi region[1], without the potential barrier that a p-well would present to liberated charge in the epi region. If the p-well/p-epi junction were abrupt (a simplification), then the potential difference, and hence the barrier height, between the two is

$$\Phi = \frac{kT}{q} \cdot \ln\left(\frac{N_{A,epi}}{N_{A,pwell}}\right)$$

where the N_A's are the respective doping concentrations.

In an additional difference, there is a small gap and no diffusion or field-oxide between the PG and TX gates. In CCDs, these gates physically overlap, but this is not possible in a single-polysilicon process such as the one used here. Leaving as small a gap as possible is a compromise solution that maximizes the charge transfer efficiency under the circumstances. The size of the gap between PG and TX is critical, however. Simulations (using Pisces) demonstrate that too large a gap can lead to insufficient transverse field and create a potential barrier to the transfer of electrons.

Fig. 5 shows the potential in volts and electron concentration laterally across the photogate (from left to right including the PG, TX and the readout diffusion), during transfer, given a 0.4-μm gap between PG and TX. We can see a monotonic decrease in potential energy which allows an unimpeded transfer of electrons. Extend that gap to 0.8 μm, as shown in Fig. 6, and a

[1]Optical applications generally suffice with a shallower absorption depth.

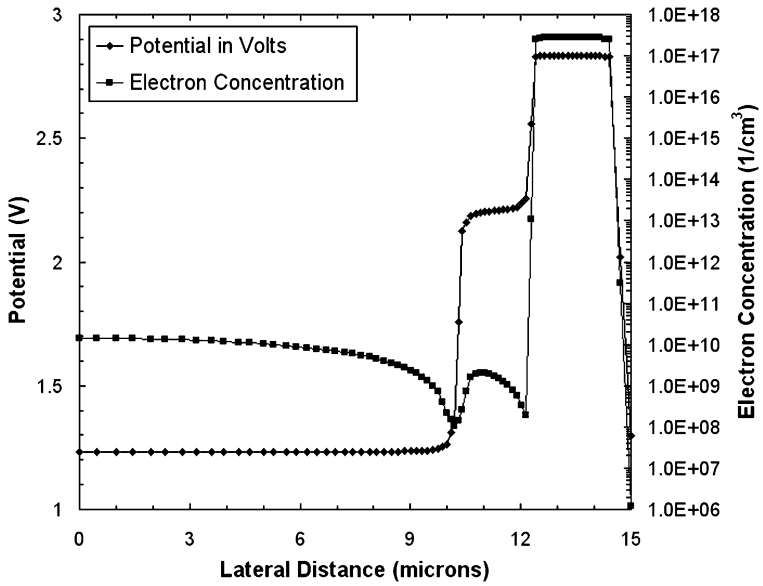

Fig. 5. Simulations of potential in volts (left scale) and electron concentration (right scale) laterally across a photogate (x axis, which is 0.02 μm below the silicon/silicon–dioxide interface), where the gap between the PG and TX gates (seen around 10 μm on the x axis) is 0.4 μm. A smooth, monotonically decreasing potential energy is seen, facilitating charge transfer.

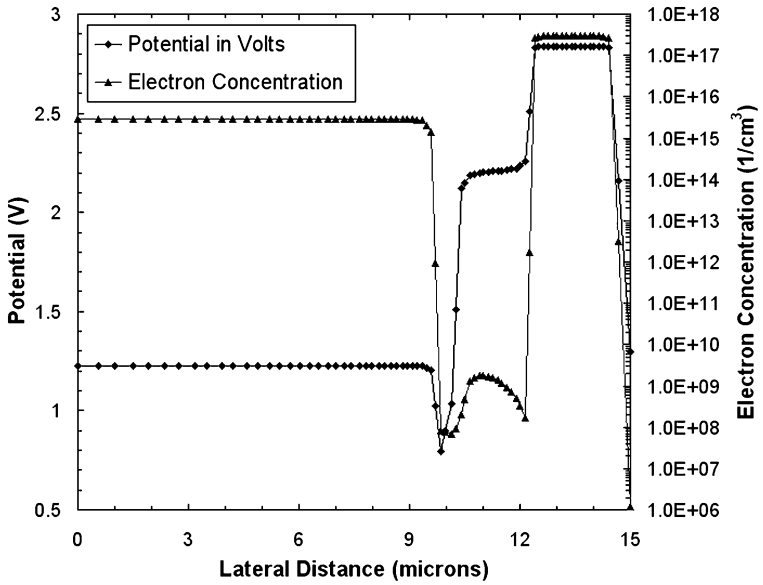

Fig. 6. Simulations of potential in volts (left scale) and electron concentration (right scale) laterally across a photogate (x axis, which is 0.02 μm below the silicon/silicon-dioxide interface), where the gap between the PG and TX gates (seen around 10 μm on the x axis) is larger, at 0.8 μm. A potential barrier is seen, impeding charge transfer.

potential barrier is seen, which would block the transfer of electrons. The distance in the actually fabricated circuit was 0.45 μm, which was the minimum distance permitted by the fabrication technology.

A variety of photogate structures, fabricated in a standard 0.25 μm digital thin-oxide (5.7 nm), 8–10-μm epitaxial-silicon process, have been tested. Sixteen different pixel designs were included in the test chip, with differences in many details, such as the boundaries of the p-wells, the inclusion of diffusion between PG and TX, the presence or absence of the TX gate, large area photodiodes with a TX gate, etc. Each pixel design was 20 $\times$20 μm, arranged in 4 $\times$ 4 subarrays of 36 by 36 pixels each, for a total of 144 $\times$ 144 pixels.

Tests of the photogate circuit have demonstrated sensitivity to ^{55}Fe X-rays. Fig. 7 shows the charge collection probability distribution of the photogate-only (no transfer gate) structure to ^{55}Fe X-rays while varying steady-state PG voltage. The grayscale indicates the number of occurrences for each ADC count and PG voltage. Some unexpected results were observed. A 5.9 keV peak was visible but did not stand out very clearly (Fig. 8), and the charge transfer times (about 10 ms for full transfer) were slow compared to simulations. We surmised that the slow transfer times blurs the ^{55}Fe measurements due to the fact that the readout is of randomly arriving hits, many of which are only partly transferred by the time the readout of a given pixel is complete.

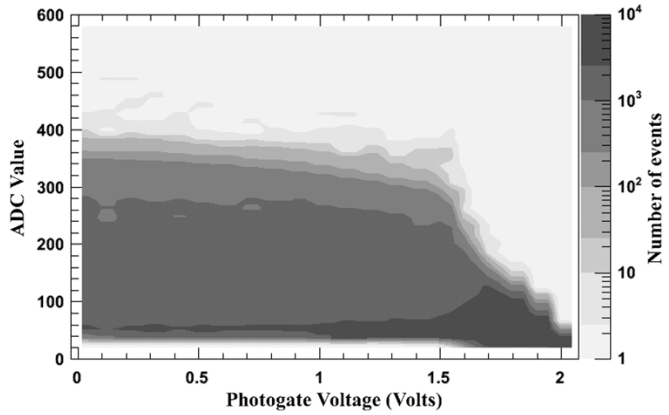

Fig. 7. A detailed DC scan, varying steady-state PG voltage, in response to ^{55}Fe X-rays. The vertical axis shows the ADC value. Horizontal axis shows PG voltage. Grayscale indicates the number of occurrences for each ADC value and PG voltage.

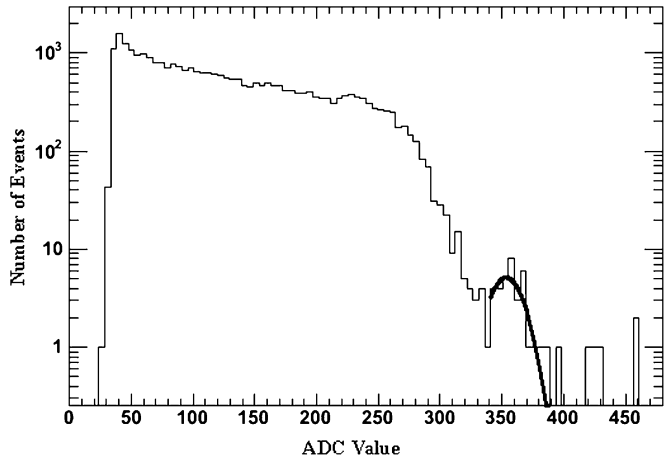

Fig. 8. Histogram of events measured at PG $= 1.55$ V. this figure represents a vertical slice from the two-dimensional histogram shown in Fig. 7. The superimposed bump is the 5.9 keV ^{55}Fe peak that is used for calibration.

An explanation of the observed slow transfer time is that a substantial fraction of the collected charge is trapped by surface states under the very large (289 μm^2) photogate area. Standard digital CMOS processes do not allow for buried channels (keeping the buried channel potential well below the surface traps) that would avoid this trapping or surface pinning (filling the surface traps) that would reduce this trapping. The collected charge density from a minimum ionizing particle may only be a few electrons per square micrometer, yet the number of traps may easily be of the same order of magnitude or greater. Trapped charge is released only slowly, and once an electron is released, it may easily be trapped again, perhaps repeatedly, instead of being promptly transferred. These observations were replicated, using the same technology, by another investigator [18], who came to the same conclusions.

An experiment was performed that provided support to this theory. The photogate circuits were exposed to brief pulses of red light of varying durations (Fig. 9). These pulses resulted in collected charge ranging from about 900 to about 4600 electrons. Higher charge levels would tend to fill a greater percentage of traps, with greater levels of remaining untrapped charge able to transfer unimpeded and hence more quickly.

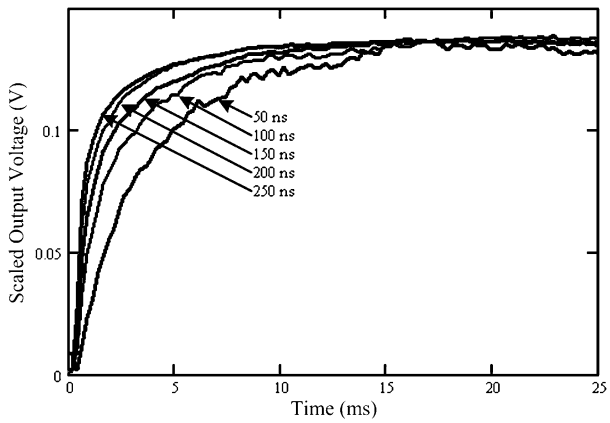

Fig. 9. Normalized rise-time plots of the photogate response to brief pulses of red light. The legend indicates the duration of the exposure. The plots are normalized to the longest exposure duration (250 ns), and the vertical scale corresponds to this light durations readout voltage. Increasing amounts of light (hence collected charge) result in faster charge transfer rise times.

Indeed, longer pulses of light resulted in faster charge transfer rise-times.

The above photogate measurements confirmed about a 16% higher charge-to-voltage conversion gain than the small photodiodes, as hoped. Of critical importance, higher average charge collection was also noted in the charge collection probability distributions, by very roughly a factor of 10. However, it is difficult to accurately quantify this until a pulsed signal source or triggered measurement is used so that complete charge collection can be guaranteed. As further confirmation, however, there was substantially reduced charge spread among neighboring pixels, with most charge collected within clusters of 4 instead of about 25 pixels. For the above reasons, signal to noise measurements or projections for minimum ionizing radiation are not yet possible.

It seems clear that this application will require the use of an enhanced process, using surface pinning or buried channels, to reduce traps, before photogate pixels can reach their full potential. The potential gain in signal to noise makes this an attractive avenue for further research.

III. Per-Pixel kT/C Noise Reduction

"Clamp and sample CDS" is a well-known technique in CCD designs and is used at the column and/or chip-level to reduce reset noise [10]. Similar capacitively-coupled "auto-zero" CDS techniques have long been used in physics applications [11]. Other techniques using multiple-sampling have also been developed, in part to address the CDS issue [12]–[14]. Here, we have fabricated and tested a per-pixel "clamp" CDS circuit for a CMOS APS sensor. Compared to external CDS or multiple sampling schemes, it holds the advantage of requiring only one read and no external subtraction, and hence is much faster.

The test circuit was fabricated in a standard 0.25-μm digital thin-oxide (5.7 nm), single polysilicon process. The pixel pitch is 20 μm. Depicted in Figs. 10 and 11, it consists of a photodiode with its parasitic capacitance C1, its reset switch T1, a source-follower T3-T4, a coupling capacitor C2, an additional reset switch T2, and readout circuitry T5-T6. The basic idea is to store the large kT/C reset noise from the T1 reset, which

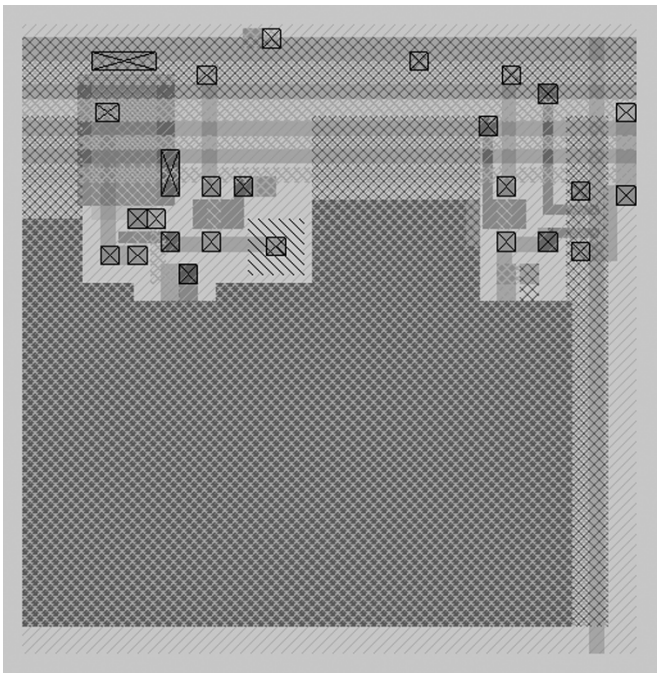

Fig. 10. Photodiode with clamp/CDS circuit. The large area is the coupling capacitor, which is formed from polysilicon and metal overlaps.

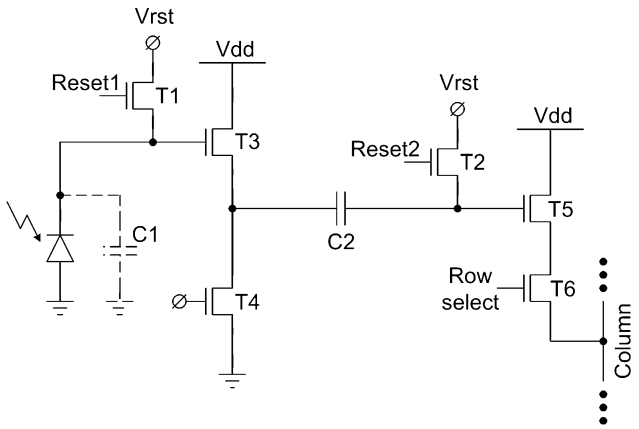

Fig. 11. Basic kT/C noise-reduction pixel schematic.

is on a low-capacitance node C1, across the much larger coupling capacitance C2. In this way, the overall kT/C reset noise is substantially determined by the larger value of C2 and hence is reduced.

Fig. 12 shows the timing operation of the per-pixel noise reduction. At the start of Δt, the T1 kT/C reset noise is stored on the small C1 photodiode node capacitance, and is also presented as an offset between the C2 capacitor terminals. At the conclusion of Δt, that offset is stored across the capacitor and hence is subtracted from the output node. Instead, the lower kT/C reset noise on the T2 transistor in combination with the larger C2 appears at the output. Normal charge integration and readout follows. It is interesting to note that by switching the order of

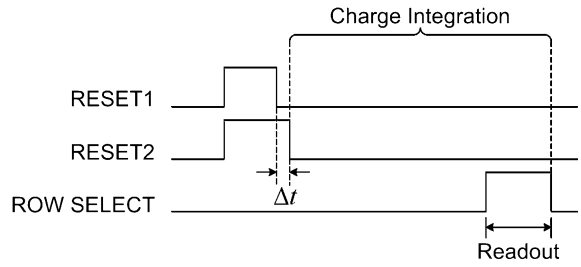

Fig. 12. Per-pixel kT/C noise reduction timing diagram.

the Reset1 and Reset2 conclusion (Fig. 12), operation with and without CDS can take place, allowing direct comparisons.

A. Noise Analysis of Per-Pixel kT/C Noise Reduction

The efficacy of the per-pixel kT/C noise reduction is based on the fact that, for small sensor-capacitance APS pixels and small signal levels, the reset kT/C noise dominates over other sources of noise. This is clear from the dramatic measured reduction (by about a factor of 4) in total noise with the use of optimal external CDS. Therefore, in this brief analysis, we will neglect minor additional contributions such as thermal noise from transistors T3 and T4.

First, we look at the case where no CDS is performed (Reset1 falls after Reset2). Let $C1$ be the capacitance of the nwell/P-epi photodiode (Fig. 11), $C2$ be the coupling capacitance, A_{SF1} the gain of the first pixel source follower, and let A_{SF2} be the gain of the second in-pixel source follower. Then the noise voltage at the output of the pixel is

$$v_{n,out} = \sqrt{\frac{kT}{C1}} \cdot A_{SF1} \cdot A_{SF2} \tag{1}$$

the input-referred noise voltage is

$$v_{n,in} = \sqrt{\frac{kT}{C1}} \tag{2}$$

which, in electrons, is

$$\frac{\sqrt{kT \cdot C1}}{q}. \tag{3}$$

Next, we look at the case where CDS is performed (Reset1 falls before Reset2). The output noise voltage is

$$v_{n,out,CDS} = \sqrt{\frac{kT}{C2}} \cdot A_{SF2} \tag{4}$$

the input-referred noise voltage is

$$v_{n,in,CDS} = \frac{1}{A_{SF1}} \sqrt{\frac{kT}{C2}} \tag{5}$$

which, in electrons, is

$$\sqrt{\frac{kT}{C2}} \cdot \frac{C1}{qA_{SF1}}. \tag{6}$$

TABLE I
PER-PIXEL NOISE REDUCTION TEST RESULTS

Measured output noise without CDS, rms:	705 μV
Input referred noise without CDS, est. rms:	39.5 e-
Measured output noise with CDS, rms:	279 μV
Input referred noise with CDS, est. rms:	15.6 e-
Measured noise reduction factor:	2.5 x
Calculated noise reduction factor:	2.8 x
Projected noise with high-density cap, rms:	202 μV
Input referred noise with high-density cap:	11.4 e-
Projected noise reduction factor:	3.5 x

Hence, the noise improvement is

$$\frac{V_n}{V_{n,CDS}} = \sqrt{\frac{C_2}{C_1}} \cdot A_{SF1}. \tag{7}$$

B. Per-Pixel kT/C Noise Reduction Circuit Measurements

The test circuit was fabricated without the benefit of a high-density capacitor structure. Instead, a stack of polysilicon and metal layers formed the capacitor. In our test circuit, C1 is about 4.3 fF and C2 is 47.0 fF. Measurements closely match the theoretically expected noise reduction, and projections were also made that take into account the higher C2 value that would be possible with a typical double-polysilicon or metal-insulator-metal capacitor.

The circuit was calibrated using an Fe-55 source and found to perform correctly. Considering that only low density capacitors were available, the measured input-referred noise of 15.6 e^-, rms, compared favorably to the best result using optimized off-chip CDS (10.3 e^-), and would nearly equal it (11.4 e^-, projected) if high-density capacitors were used. Yet this technique requires only one read and no external subtraction. It is therefore much faster and more convenient. Drawbacks include having slightly reduced gain due to the extra source follower, and of requiring additional power. The added per-pixel power is only used during reset and readout however, and can be turned on one row at a time, so this may be a fairly minor concern. The typical electrical performance results are summarized in Table I.

IV. ACTIVE RESET NOISE REDUCTION

A chip testing a variation on a relatively new method of kT/C noise reduction, "active reset" [15]–[17], was fabricated and measured. The test chip is fabricated in a 0.5-μm thin-oxide (14.5 nm) digital CMOS process, including a 10–12-μm epitaxial region, and contains several sectors of pixels, each with different photodiodes and/or other circuit variations. These variations allowed noise comparisons with different photodiode and feedback capacitances, including tests with explicitly added additional feedback capacitance. The technique appears particularly well suited to applications where high sensitivity and low noise are required.

Column-level active reset requires one additional transistor per pixel, bringing the total to 4 in an otherwise-traditional APS, and a per-column op-amp (Fig. 13). The added transistor per pixel controls the gate of the reset transistor M1.

The two most important feedback mechanisms of active reset are the amplification of feedback capacitance, and hence the increase in the effective capacitance on the photodiode during reset due to the Miller effect (reducing kT/C reset noise), and the control of the resetting current via negative feedback (Fig. 14). The first feedback loop is via the gate-to-source capacitance of the photodiode reset transistor M1. This capacitance is amplified by a factor of $(A + 1)$, where A is the open-loop gain of the column-level op-amp. The second feedback is via the transconductance of the reset transistor M1. Noise on the photodiode node will be reduced by the opposing, amplified, modulation of the drain current in the reset transistor. The channel noise of M1 is greatly reduced by the two feedback mechanisms, and it is exactly the channel noise of M1 that causes the reset kT/C noise in a normal "hard" reset.

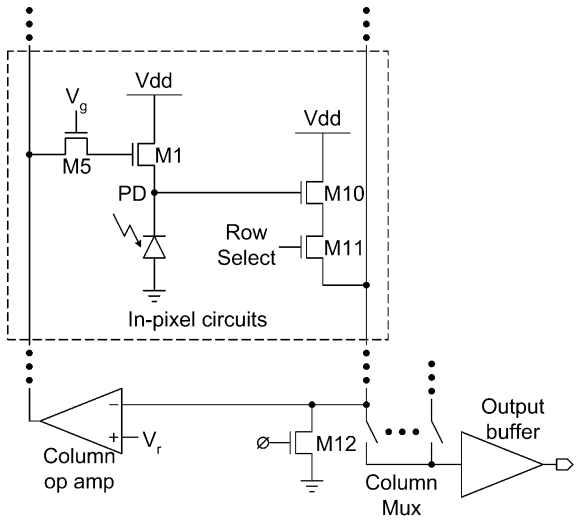

Fig. 13. Basic active reset schematic diagram. A single pixel is shown, along with the per-column op-amp and chip-wide output multiplexing.

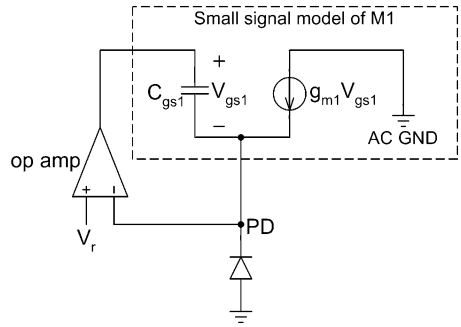

Fig. 14. Simplified active reset model. The capacitance that is amplified is the parasitic gate to source capacitance of the reset transistor M1 plus any explicitly-added capacitance. The transconductance of the reset transistor is also modulated by the feedback.

Active reset requires, in our low-power implementation, about 10 μs per row for a 1-V maximum signal range as may be typical in optical applications. For minimum-ionizing radiation, less than a 100-mV reset swing is required, and reset times would drop to 1 μs per row. This is slower than a standard reset, but active reset can be pipelined with readout and digitization without additional time overhead.

During reset, M5 (Fig. 13) is turned on (V_g is high) at moment t_1 (Fig. 15) to activate the feedback loop of the active reset, and the reference voltage V_r at the noninverting input of the column op-amp is raised from a low level (e.g., ground) at a rate of about 100 mV/μs. During this period, the column readout line and the

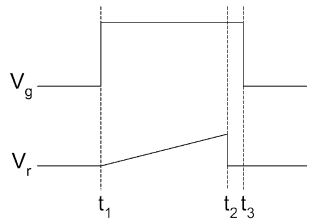

Fig. 15. Timing diagram for the active reset scheme.

voltage on photodiode node follows V_r closely. At moment t_2, V_r is lowered, the op-amp enters an extremely nonlinear region as its output and gain falls to zero, while voltage at the PD node keeps its level just prior to moment t_2. After a brief delay to allow all signals to settle, M5 is turned off at moment t_3 to conclude the reset.

In addition to reducing kT/C reset noise, the column level active reset technique can reduce fixed pattern (pedestal) noise (FPN), particularly FPN within each column where differing op-amp offsets are not an issue, by stabilizing the different pixel outputs against a reference voltage.

A. Active Reset Noise Analysis

Active reset can greatly reduce the kT/C noise of the reset switch; the dominant source of noise in small photodiode APS. Since column-level active reset is relatively new, we present a summary noise analysis of this technique, with more detail presented in [17]. Here, we analyze of noise at the two important points in time, t_2 and t_3, as seen in Fig. 15.

(1) At moment t_2, just before the reference voltage V_r drops, the noise at the PD node is mainly from the thermal noise of the column op-amp and the drain current noise of M1:

$$\begin{aligned}\overline{V_n^2}\Big|_{t_2} &\approx \overline{V_{n,opamp}^2}\Big|_{t_2} + \overline{V_{n,M1}^2}\Big|_{t_2} \\ &= \int_{-\infty}^{\infty} S_{v_{n,opamp}}(f)\cdot\left|\frac{v_{pd}}{v_{rn}}(f)\right|^2 df \\ &\quad + \int_{-\infty}^{\infty} S_{I_{n,M1}}(f)\cdot\left|\frac{v_{pd}}{i_{dn,M1}}(f)\right|^2 df. \end{aligned} \tag{8}$$

The first term to the right of the equal sign is the noise contribution from the op-amp, and the second term is the noise contribution from M1. The noise voltage at the PD node is v_{pd}, v_{rn} is the equivalent noise voltage referred to the noninverting node of the column op-amp, and $i_{dn,M1}$ is the noise in the drain current of M1.

If we assume that the column op-amp has a large open-loop gain $A = G_m \cdot R_O \gg 1$, then the two transfer functions v_{pd}/v_{rn} and v_{pd}/i_{dn} are approximately

$$\frac{v_{pd}}{v_{rn}} \approx 1 \tag{9}$$

and

$$\frac{v_{pd}}{i_{dn}} \approx \frac{1}{j\omega C_{pd} + (A+1)[j\omega C_f + g_{m_1}]} \tag{10}$$

where C_{pd} is the photodiode capacitance, C_f is the feedback capacitance, and g_{m1} is the transconductance of M1. The approximately unity ratio between v_{pd} and v_{rn} is intuitively correct because they are the two inputs of the op-amp, and v_{pd} should closely follow v_{rn} during active reset. The transfer function v_{pd}/i_{dn} is the most interesting part of this analysis, as it reveals the two important feedback mechanisms. Equation (10) can be rewritten to show the equivalent capacitance at the PD node during active reset

$$C_{eq} = C_{pd} + (A+1)\left[C_f + \frac{g_{m_1}}{j\omega}\right]. \tag{11}$$

The two terms in the square brackets correspond to the two fundamental feedback mechanisms: the first term indicates that feedback capacitance C_f is amplified by $A+1$ due to the Miller effect. The open-loop gain A is critical to enlarging C_{eq} and hence reducing the kT/C noise. The second term indicates the feedback of the photodiode voltage v_{pd} back to the V_{gs} of M1 in order to control the resetting current I_d of M1.

(2) At moment t_3, just before the loop switch M5 is turned off, the noise at the PD node mainly consists of the attenuated noise from moment t_2, and the thermal noise from M5 at moment t_3:

$$\begin{aligned}\overline{V_n^2}\Big|_{t_3} &\approx \overline{V_n^2}\Big|_{t_2}\cdot(a+be^{-p(t_3-t_2)})^2 \\ &\quad + \int_{-\infty}^{\infty} S_{v_{n,M5}}(f)\cdot\left|\frac{v_{pd}}{v_{n,M5}}(f)\right|^2 df. \end{aligned} \tag{12}$$

The first term to the right of the equal sign is the attenuated noise from moment t_2, where a is the dc attenuation factor, b and $1/p$ are the magnitude and time constant of the exponential decay of the noise voltage on the PD node. The second term is the noise contribution from M5 at moment t_3, when M5 is in the triode mode and its thermal noise dominates. There is almost no noise contribution from the column op-amp during (t_2, t_3) due to the fact that the column op-amp is at ground potential with zero gain. Details of a, b, p and the transfer function $v_{pd}/v_{n,M5}$ are of less importance and are described in [17]. The noise contributions of M10, M11, and M12 can be neglected during the column level active reset, as the total noise power from these three transistors is inversely proportional to the column-line capacitance C_{col}, which has a large value.

B. Noise Measurements of the Active Reset Circuit

Electrical tests of the active reset chip were performed using a low noise amplifier (less than 30 μV, rms). Readout noise of ~ 44 microvolts and a dynamic range of ~ 90 dB (~ 15 bits), rms, was measured on a sector of large photodiodes such as would be used in optical applications. A sector of small photodiodes, such as would be used in a tracking application, was measured to have 120 μV rms noise, as compared to 910 μV with a standard reset—a factor of 7.6 improvement.

Temporal noise was measured and compared to the calculation for different values of feedback capacitance C_f (Fig. 16). Analysis indicated that noise reduction is more sensitive to the increase of g_{m1} than the increase of C_f, as $j\omega\ C_f$ is typically smaller than g_{m1}. The relative insensitivity of noise reduction in terms of C_f is supported by measurement, as only a small improvement in temporal noise was measured when extra feedback capacitance was applied.

The array was measured with an ^{55}Fe source in order to calibrate the gain of the pixels. An estimated input-referred noise of 8.3 e^- was found. This is superior to our best result measured

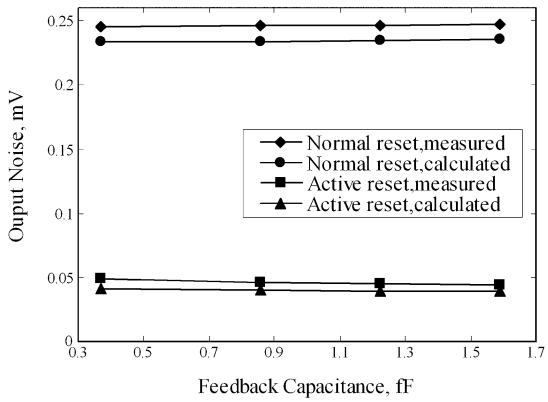

Fig. 16. Output noise voltage versus different feedback capacitance values. The photodiode capacitance is estimated as 84 fF, and the feedback capacitance is 0.367 fF before extra feedback capacitance is added deliberately.

TABLE II
ACTIVE RESET TEST RESULTS

Output noise without active reset, rms:	910 μV
Input noise w/o active reset, rms (est.):	63 e-
Output noise with active reset, rms:	120 μV
Input noise with active reset, rms (est.):	8.3 e-
Improvement in noise due to active reset:	7.6 x
Fixed pattern noise w/o active reset, rms:	15 mV
FPN within columns with active reset, rms:	0.7 mV
Improvement in FPN within columns:	21 x
FPN within rows with active reset, rms:	3.8 mV
Improvement in FPN within rows:	3.9 x

thus far from standard pixels, with optimized CDS, of 10.3 e^-. Recalling that the active reset chip was a 0.5-μm design instead of the previous 0.25-μm designs, direct comparisons are somewhat risky.

Column-level active reset will substantially reduce pixel-level FPN, much as CDS does. It does so by stabilizing the column output levels against the op-amp reference voltage during reset. Hence, all FPN associated with each pixel and the column-level source follower is divided by the gain of the op-amp A, which is high enough to reduce FPN to nearly zero. On the other hand, each column op-amp has a certain input offset FPN that is an additional source of FPN. In practice, we found the pixel-level FPN to be reduced by a factor of 21, from 15 to about 0.7 mV, rms. Column-level FPN (mostly due to the op-amp offsets) were also reduced, at about 3.7 times lower, to about 3.8 mV. The measurement results for the small photodiode pixels are summarized in Table II.

Active reset looks very promising for several reasons. It significantly reduces both temporal and fixed pattern noise, yet it does not affect the gain of the system as the previous per-pixel CDS circuit does. It obtains similar or better noise reduction when compared to conventional CDS. In particular, traditional CDS actually increases the impact of noise sources that are not correlated between samples, while active reset does not. Although active reset is slower, it can be pipelined with readout, and unlike CDS it requires only one read and no subtraction.

The FPN reduction becomes particularly interesting if sparse data readout is considered. In normal APS readout, FPN can be higher than the signal levels seen in vertex applications, and hence pixel-by-pixel pedestal subtraction may be required, posing a substantial burden. With active reset, the dramatic reduction in FPN noise within each column may negate that need, and only per column offset cancellation may be necessary—a far easier proposition.

V. SUMMARY AND CONCLUSION

Three new CMOS active pixel circuits for vertex tracking applications have been designed and tested. First, native epitaxial silicon photogate variations were investigated for their potential to increase local charge collection while preserving high charge to voltage gain. Although functional, we concluded that an advanced process, including buried channels or surface pinning to reduce the problem of surface-state traps, would be required before they can reach their full potential. Next, a fast per-pixel kT/C noise reduction circuit was tested and found to yield results competitive with traditional CDS, with 15.6 e^- rms input-referred noise measured, providing a factor of 2.5 improvement, and 11.4 e^- noise projected with the use of high-density capacitors. Finally, a column-level active reset noise reduction circuit was tested and found to reduce temporal noise by a factor of 7.6 and fixed-pattern (pedestal) noise by up to 21 times, to only 0.7 mV. With the technique, input referred noise was estimated to drop to 8.3 e^-, rms, which is superior to our best measurement of 10.3 e^- using optimized off-chip CDS.

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