Tera-Pixel APS for CALICE

Progress

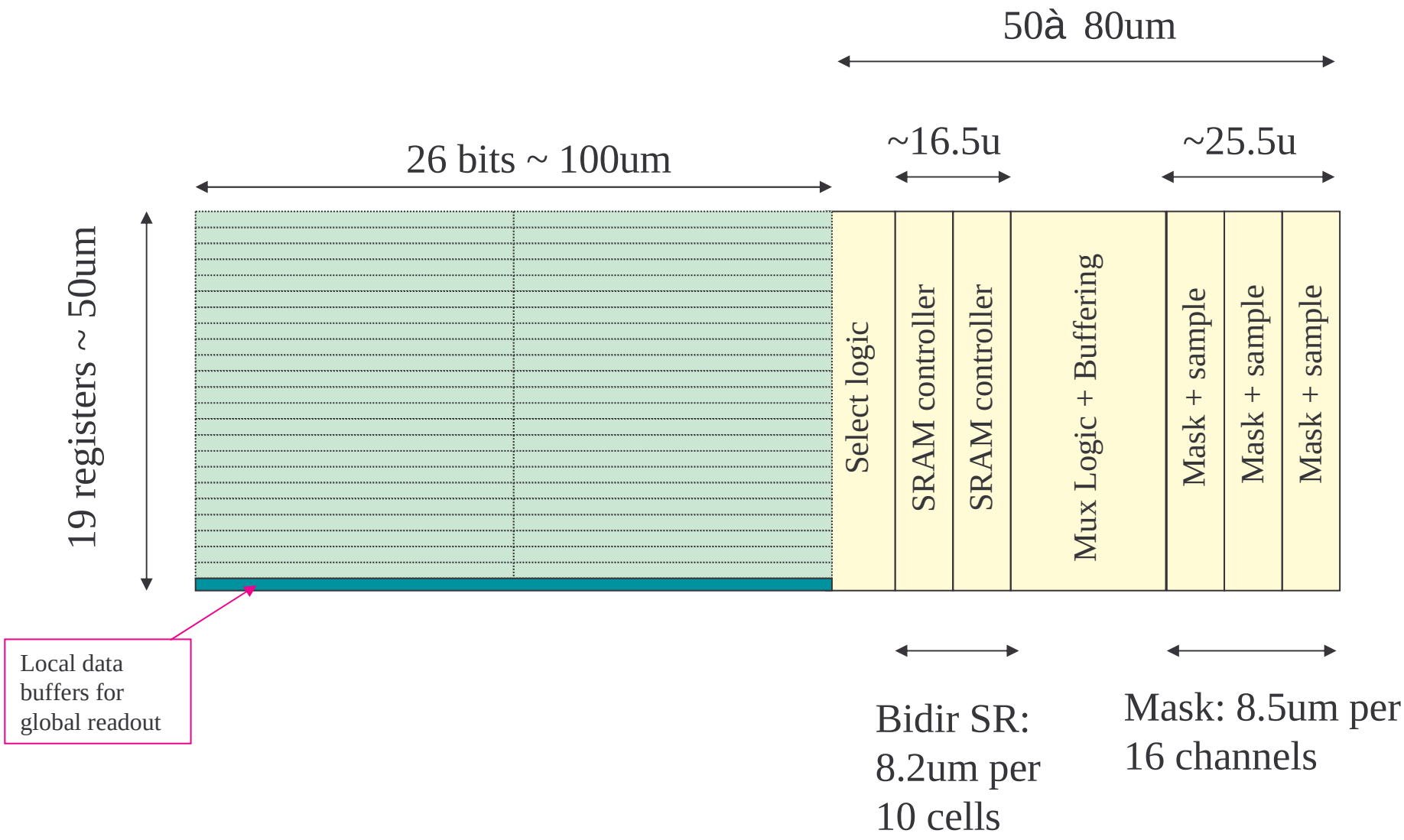
19th January 2007

Recent Activity

- IDR
- Foundry
  - Deep P implant
  - Submission date changed!

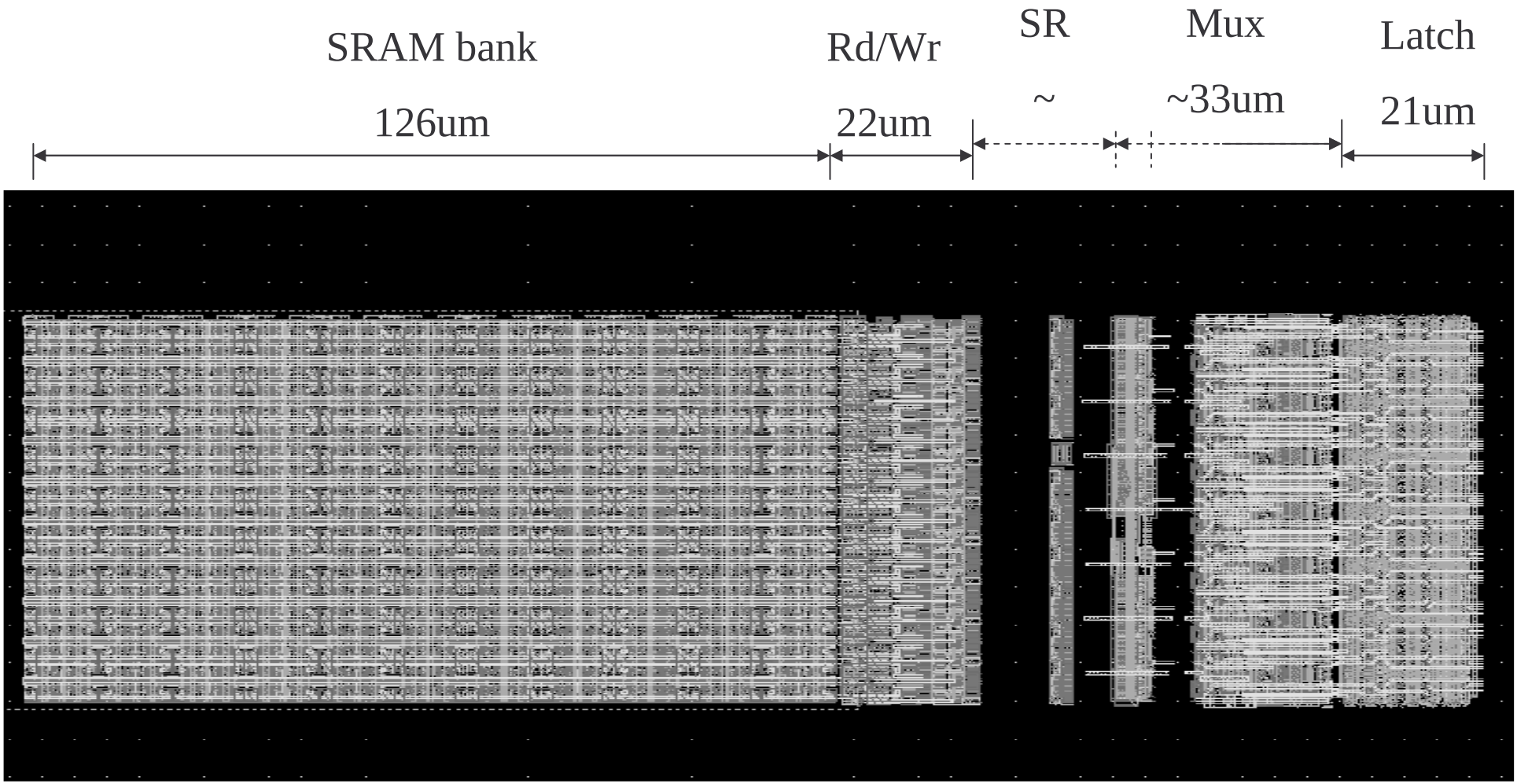
- Logic layouts well underway
  - Slightly larger than initial predictions
- Pixel layouts in early stages
  - Example
- Capacitor technology change

Area Estimates (from 6th Sept 06)

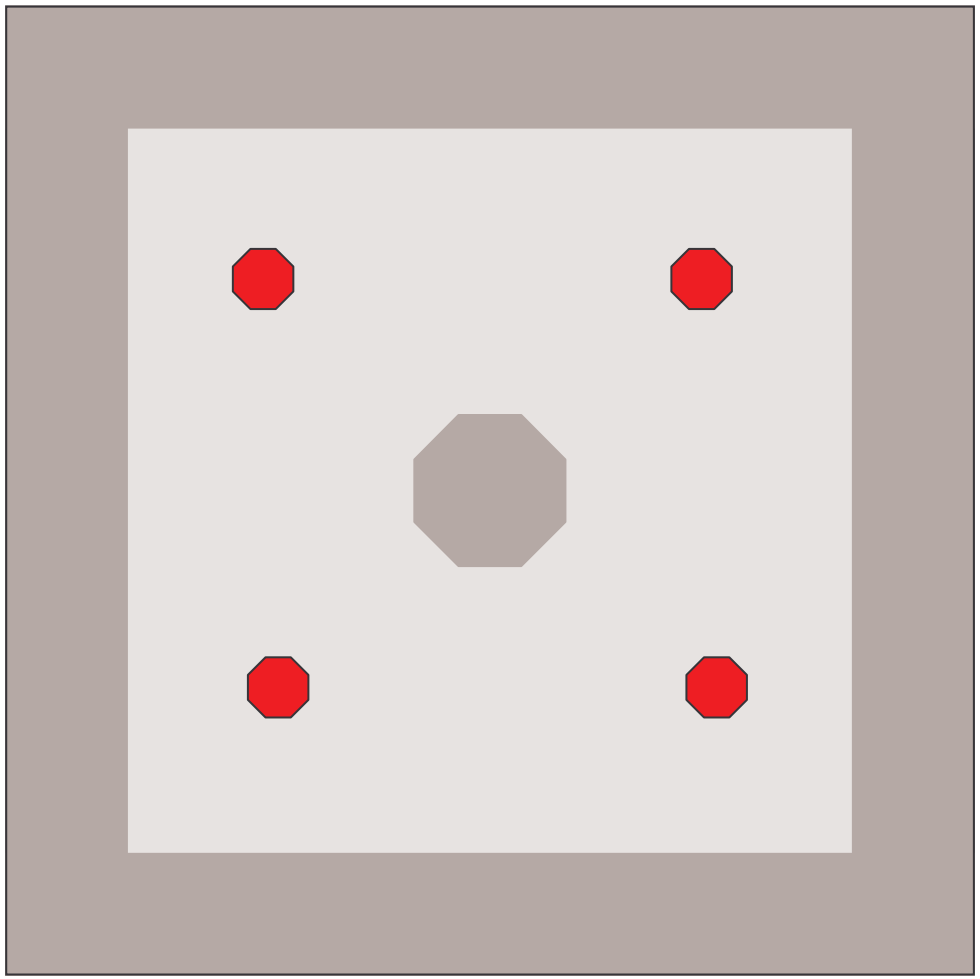


Logic layouts: Actual sizes

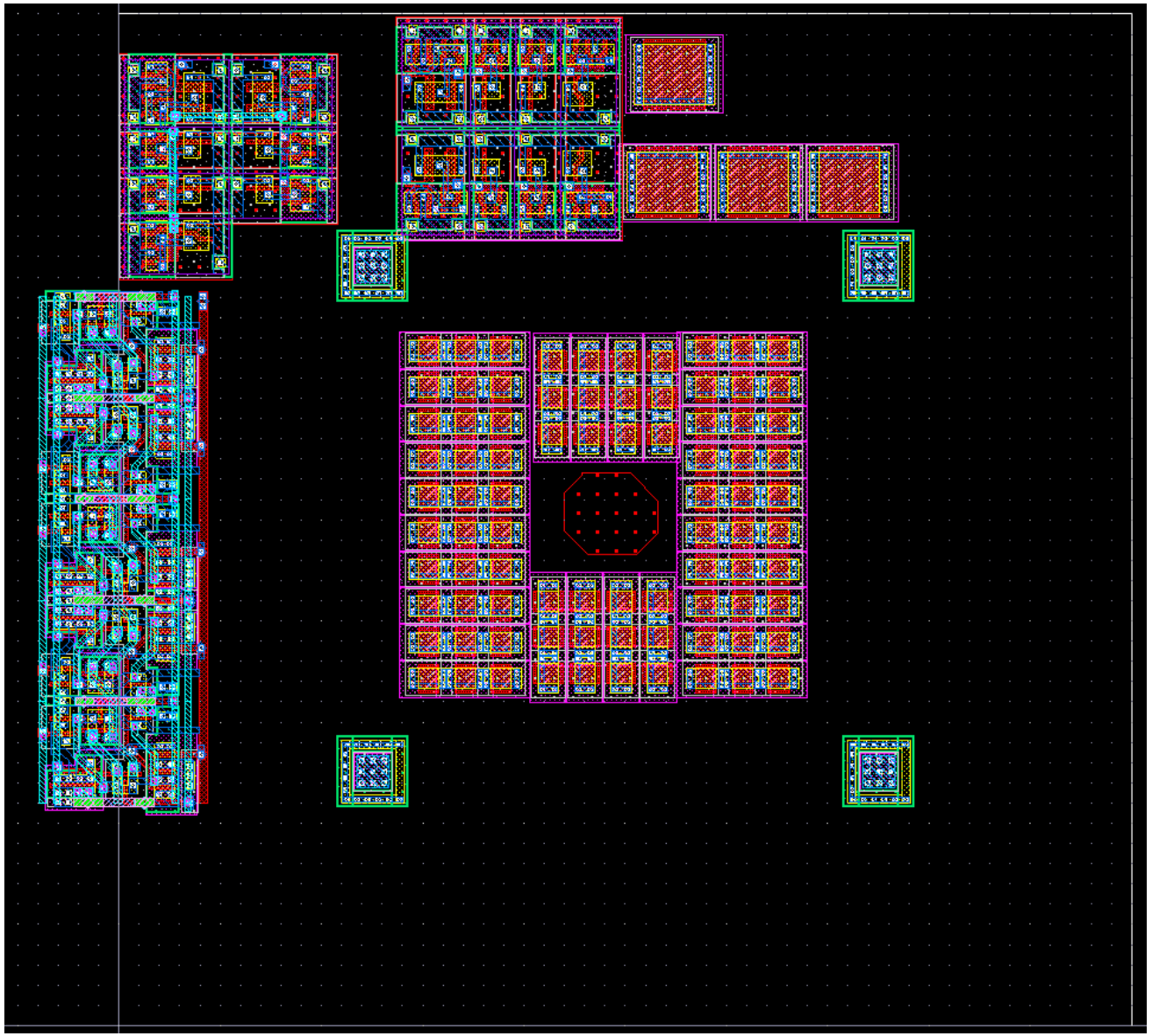
(50 micron row pitch)



Likely Pixel Arrangement



Pixel Layout



Capacitor Technology