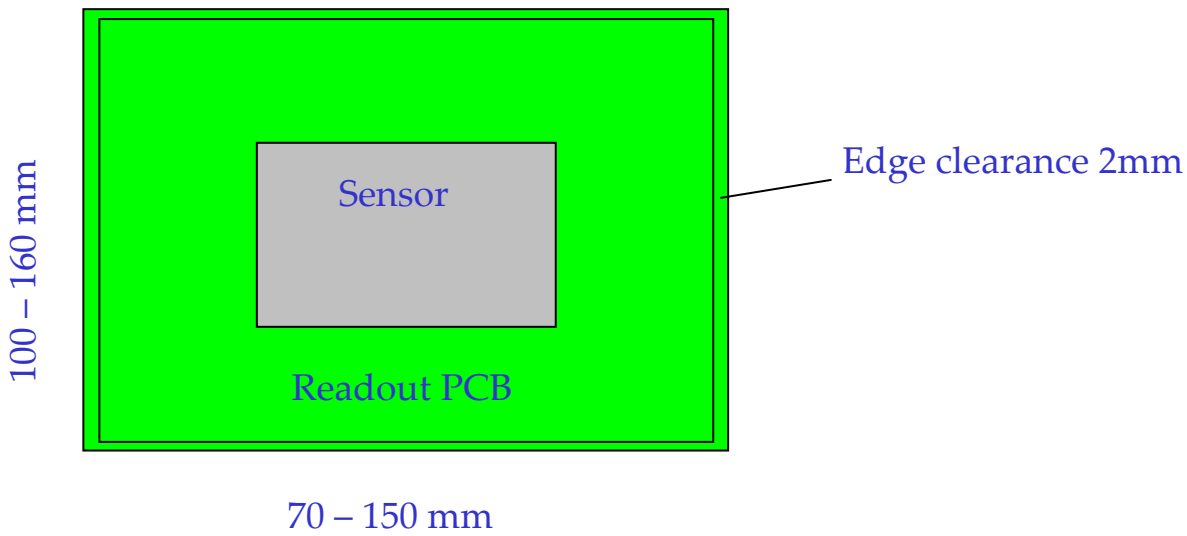
Activities so far

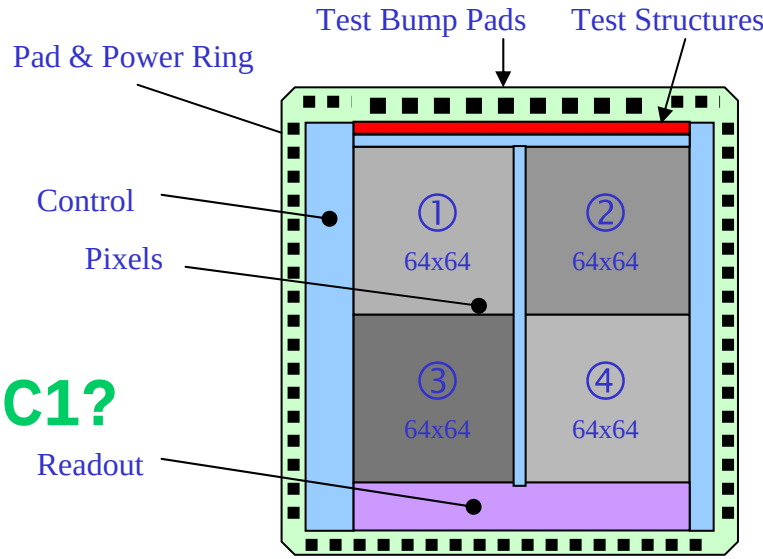
- Meeting at Imperial, Paul and Matt
- A part of work on preparation for testing of the ASIC1 reallocated from Matt to me:
  - Readout PCB
  - (tbc) a part of firmware for the control board

Readout PCB

- There are mechanical constraints, seemed not too harsh at first glance



Readout PCB



- **Still not known:**
  - most important: pin out of ASIC1?
  - how many I/O?
  - how many variable voltage references; what precision?

For the above, an input from RAL is awaited

- clock, control & readout connector(s)? (to be settled down through contact with Imperial)

Readout PCB

- Preliminary working assumptions:
  - 40 input + 40 output MAX
  - 20 analog voltage references MAX, precision not really known, working out multiple possibilities while waiting
  - linear power supplies, in order to avoid noise off switching power supplies
- Now it does not seem that relaxed regarding mechanical constraints, quite a lot of external components might be needed
- Not a problem packing them within given constraints – personally would prefer more space for relaxed physical separation of LVDS, analog and digital sections of the board

Control Board firmware

- There is a plan that a daughter board holding 1Mx18 bit SRAM for buffering of readout data is attached to the control board
- The SRAM interface firmware block is not written yet, not 100% sure whether Matt or I will write it (not really on agenda at the moment)