ASIC1 test PCB status

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Present

- The board has been first submitted on Wed 4 July to the manufacturer #1
- Manufacturer #1 replied they could not make the board as is (the PCB build with blind vias is tricky)
- When asked what could be done on our side in order to do the business ASAP, they said it was not possible in a short term
- We approached manufacturer #2 with the same question, and they proposed a new build, which was submitted on Friday 6 July

Present

- Original build was 8-layer build with multiple blind vias (1-7, 1-5, 2-8, …)
- When informed it was hard to manufacture, I promptly modified the design to employ only 1-7 blind vias
- Even then, manufacturer #1 said it could not be settled in a short time, whereas manufacturer #2 proposed that they (for some reason) introduce additional layer between original layers 6 and 7; the new layer would be just a dummy structure, needed for technology reasons.
- The introduction of new layer caused a change to widths of and gaps between tracks on the board, but hey…
- The manufacturer warned the boards might bow a bit, but this is not an issue for us

Present

- The board is electrically still a 8-layer board, but physically it is a 9-layer board

Present

- Maximalist requests for the board accomplished (reference to PCB review)
  - four tantalum capacitors per power net
  - M3 mounting holes
  - three LA connectors

Future

- The first three boards finished on the last Friday, 13 Jul
- Shipped to the IC the same day
- The first three boards ready for initial tests (assembled):
  - Optimistic: Wednesday 18 Jul (if assembled at IC)
  - Pessimistic: Tuesday 24 Jul (if assembled commercially)
- Initial tests to be done at RAL, by Jamie and me
- Matt should have DAQ software ready soon

The board outline