Science & Technology Facilities Council

Rutherford Appleton Laboratory
Particle Physics Department

A MAPS-based readout for Tera-Pixel electromagnetic calorimeter at the ILC

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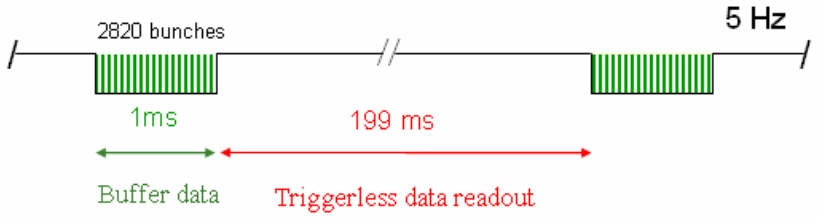
Outline

- ILC CALICE
- CALICE MAPS Concept, R&D activity
- Conclusions

ILC operation

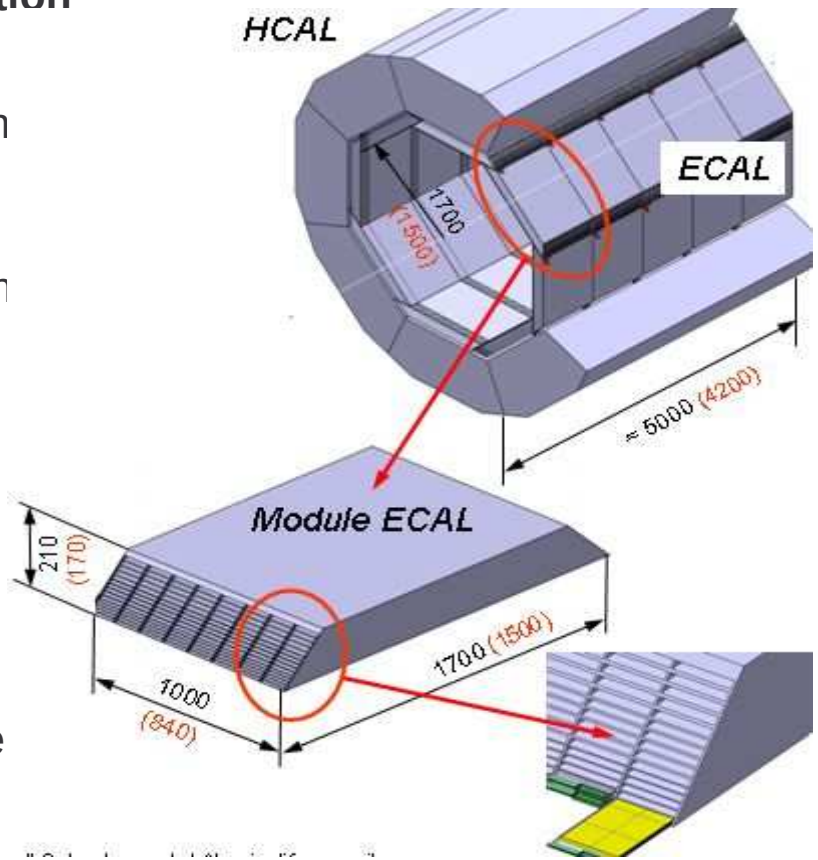
TESLA 500GeV



- Exact ICL beam timing parameters not yet defined
  - Assume close to previous (“TESLA”) design
  - Beams collide rapidly within a quick burst (“train”)
  - Long dead time between trains
- Assume worst case timing as follows
  - Beam collision rate within train = 6.7 MHz, i.e. 150ns between collisions
  - Number of collisions within train = 14000, i.e. train is 2ms long
  - Train rate = 10Hz, i.e. 100ms between trains; 2% duty cycle
- Rate of signals
  - ILC is not like LHC; rate of physics processes is small
  - Most collisions give nothing, but when reaction does happen, many adjacent channels will be hit
  - Expected rate not very well known; needs detailed simulation modeling
  - Assume average ~10–6 hits/pixel/crossing, which is ~0.005 hits/pixel/train

CALICE description

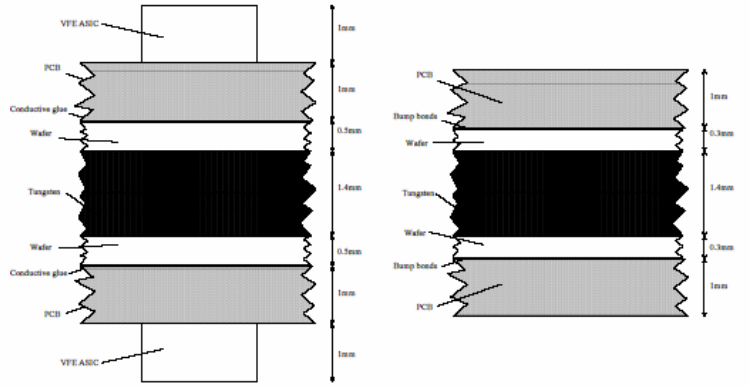
- CALICE has a baseline ECAL design
  - Sampling calorimeter, alternating thick conversion layers (tungsten) and thin measurement layers (silicon)
  - Around 2m radius, 4m long, 30 layers tungsten an silicon, ≈2000m2 Si
- Mechanical structure
  - Half of tungsten sheets embedded in carbon fibre structure
  - Other half of tungsten sandwiched between two PCBs each holding one layer of silicon detector wafers
  - Whole sandwich inserted into slots in carbon fibre structure

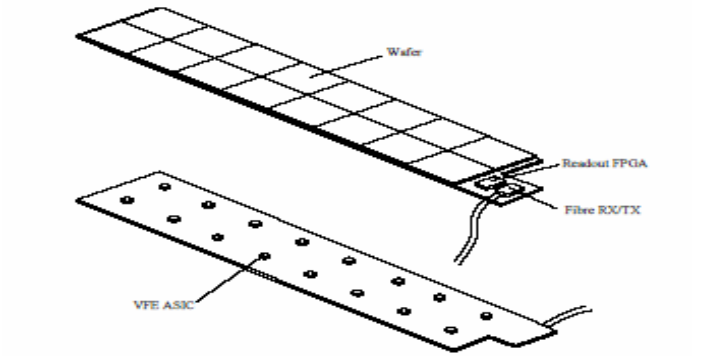


CALICE description

Baseline ECAL design

- Silicon sensor detectors in baseline are diode pads, pad size between 1.0×1.0 and 0.5×0.5 cm2, glued to large PCB
- Pad readout is analogue signal; digitized by Very Front End (VFE) ASIC mounted o the other PCB side
- Si wafers ≈ 10x10cm2
- Si layers on PCB ≈ 1.5m long 30cm wide
- Average dissipated power 1-5 μW/mm2
- Total number of pads around 20-80M





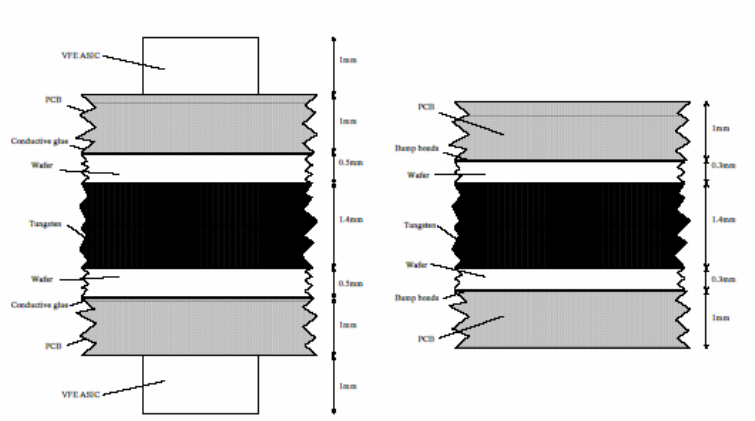
CALICE MAPS design

MAPS ECAL design

Baseline design with diode pads largely unaffected by use of MAPS

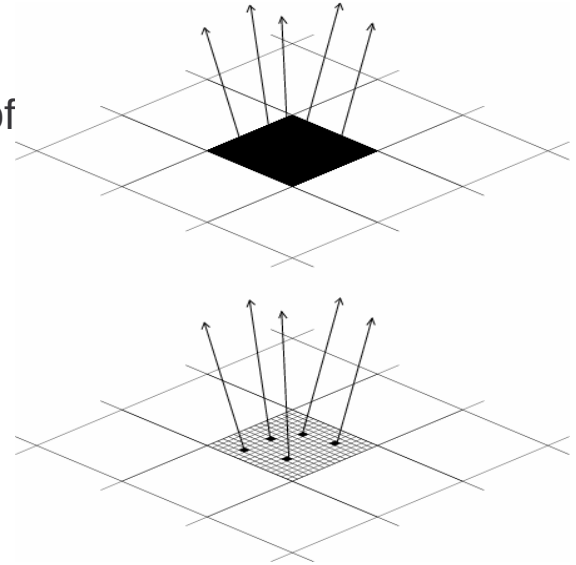
Potential benefits include:

- Reduced PCB section for MAPS ⇒ Decrease in Moliere radius ⇒ Increased resolution
- Increased surface for thermal dissipation
- Less sensitivity to SEU because of spread out logic
- Cost saving (CMOS standard process vs. high resistivity Si for producing 2*10^7 cm2 and/or overall more compact detector system)
- Simplified assembly (single sides PCB, no need for grounding substrate)



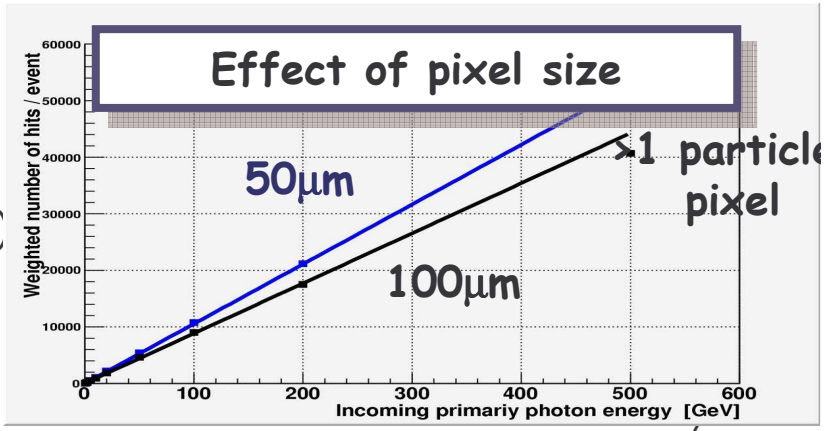
Baseline design with VFE (left) and MAPS without VFE (right)

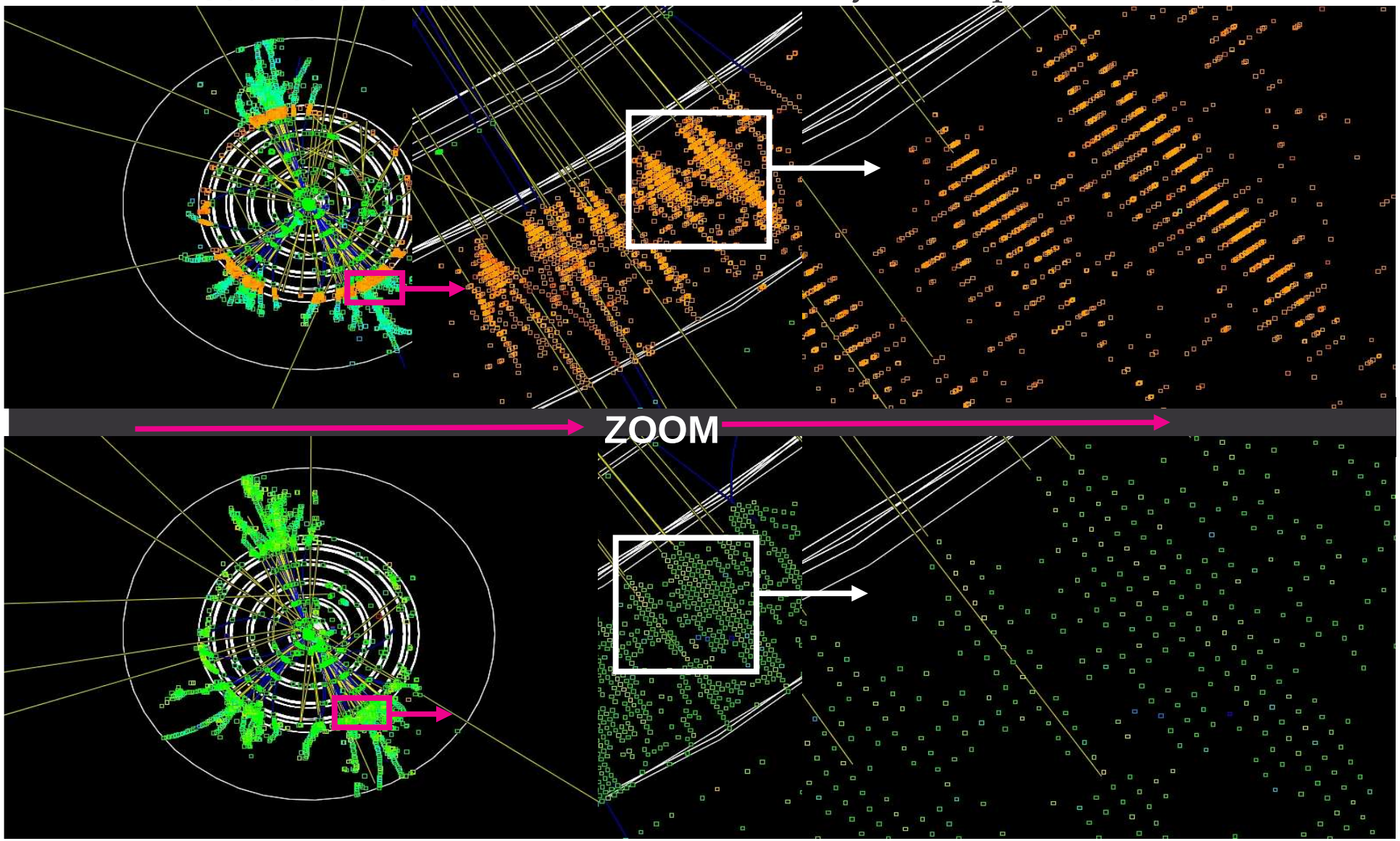
CALICE MAPS design



- Divide wafer into small pixels so as to have small probability of more than one particle going through each pixel
- Binary readout, 1bit ADC
- Improved jet resolution or reduced number of layers (thus cost) for the same resolution

- Around 100 particles/mm2 pixel size of maximum 100 X 100u2
- Current design with 50 x 50um2 pixel
- Total number of pixel for ECAL around 8 x 1011 pixels ➡ **Terapixel** system
- Record collision number each time hit exceeding threshold (timestamp stored in memory on sensor)
- Information read out in between trains




ZOOM

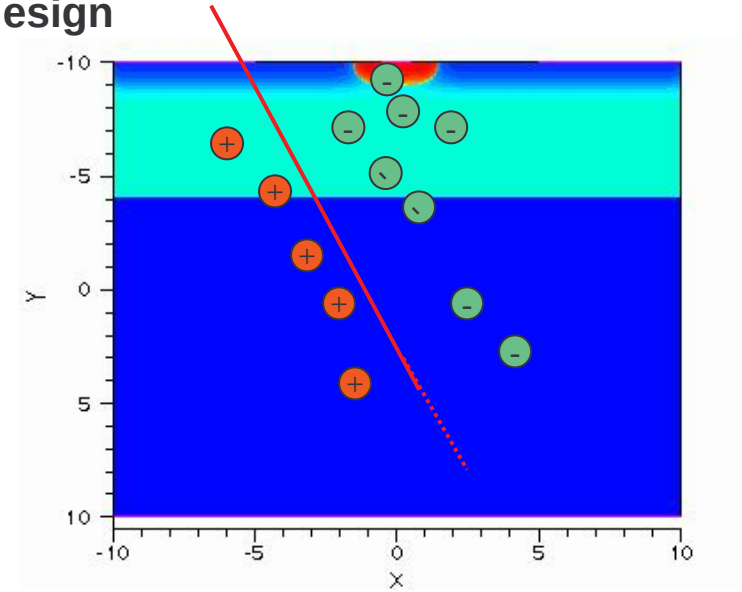
CALICE MAPS design

- First prototype designed in CIS 0.18 μm process submitted early 2007
- Different pixel architectures included in the first prototype
- Target is to reduce noise to the level of physics background (S/N>15)
- Faulty pixels masking and variable threshold to reduce false hits and crosstalk
- Optimization of pixel layout and topology essential
- Minimization of power consumption essential

CALICE MAPS design

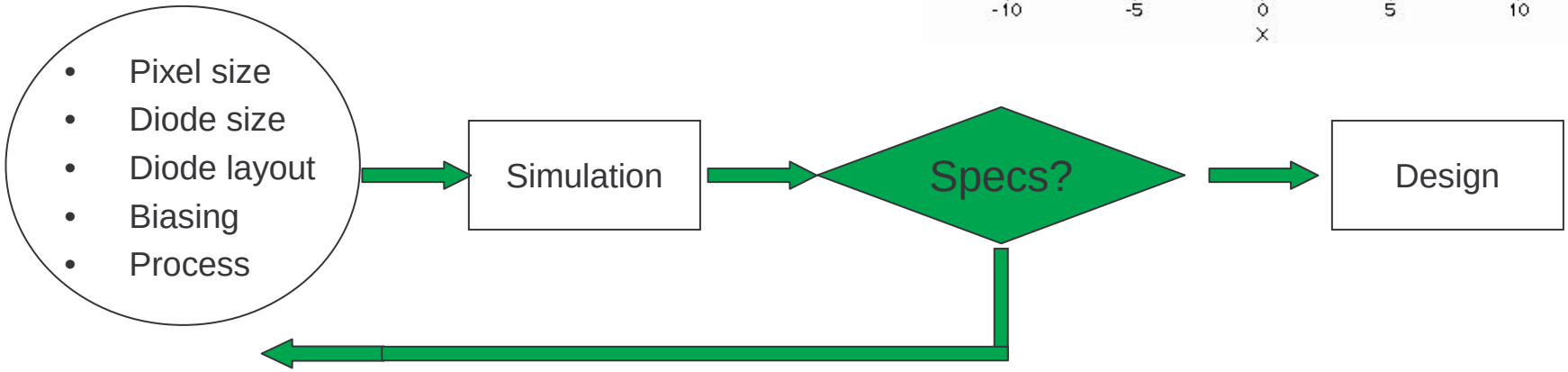
- Pixel layout optimization:

Ø Maximization of signal
Ø Minimization of charge sharing (crosstalk)
Ø Collection time

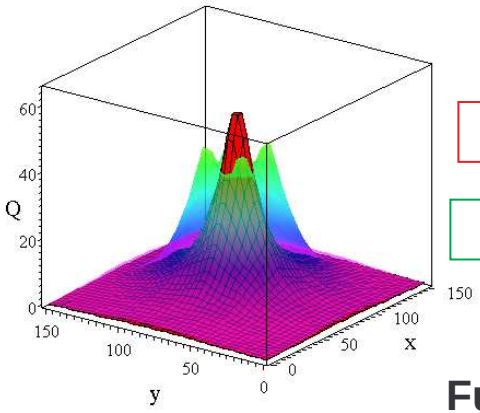


Large phase space:

- Pixel size
- Diode size
- Diode layout
- Biasing
- Process

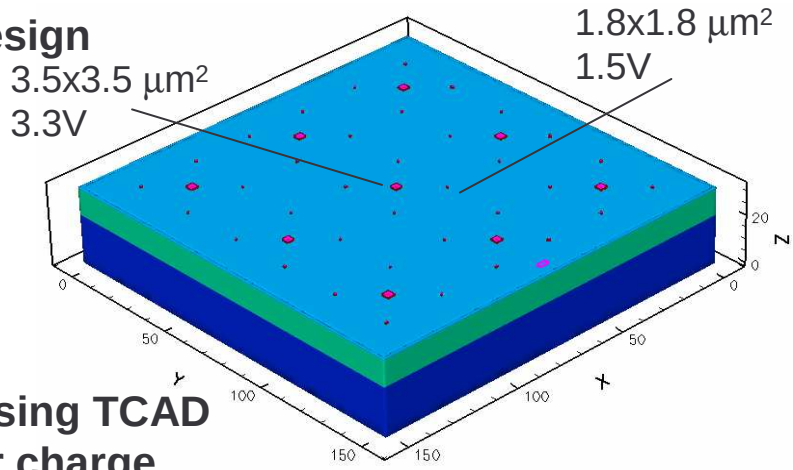


CALICE MAPS design



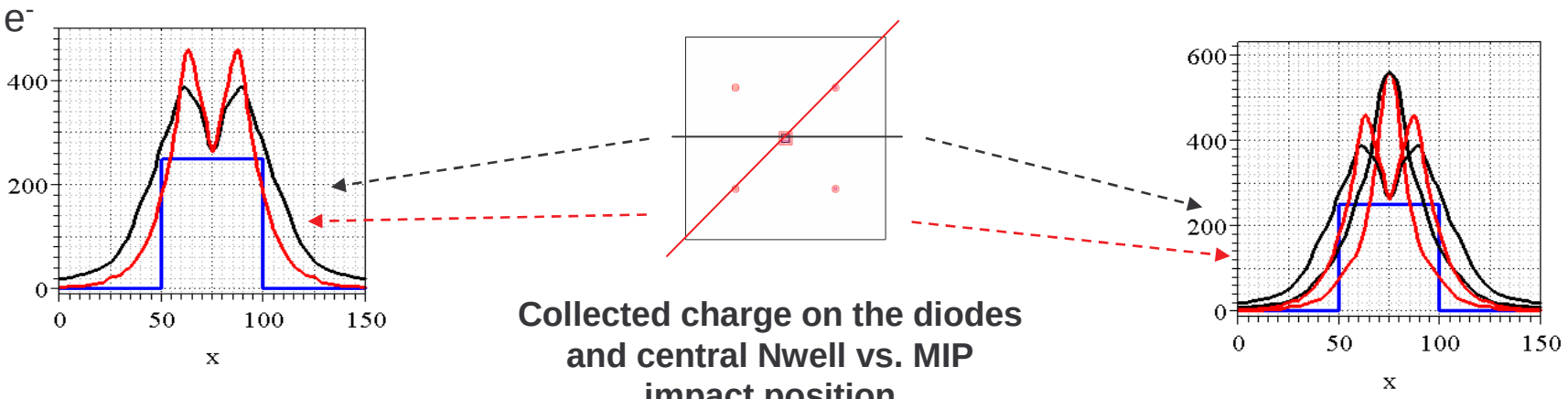
Q lost in NWell

Q collected by diodes



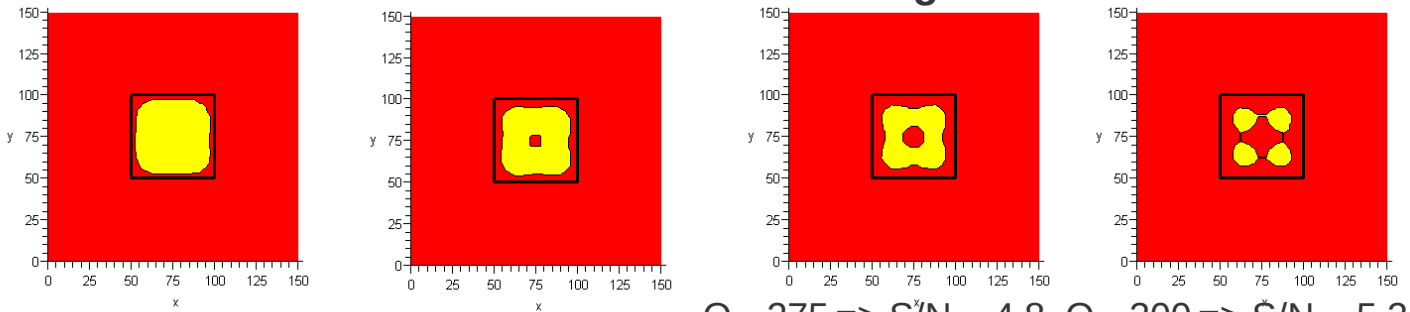
Full 3D device simulation using TCAD Sentaurus (Synopsys) for charge collection study

MAPS - central NW houses electronics-



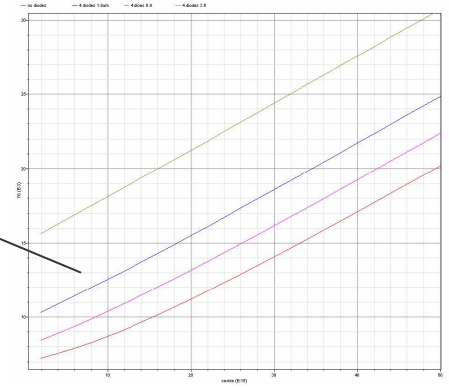
Collected charge on the diodes and central Nwell vs. MIP impact position

CALICE MAPS design

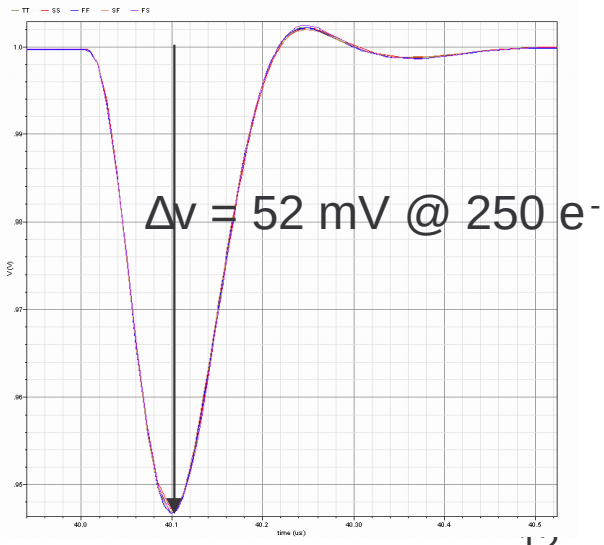


Q_{thr} 225 => S/N ~ 4 Q_{thr} 250 => S/N ~ 4.4 Q_{thr} 275 => S/N ~ 4.8 Q_{thr} 300 => S/N ~ 5.2

- Crosstalk is reduced by increasing threshold
- This at the expense of S/N
- Reduce the charge lost in N-Well housing the readout electronic



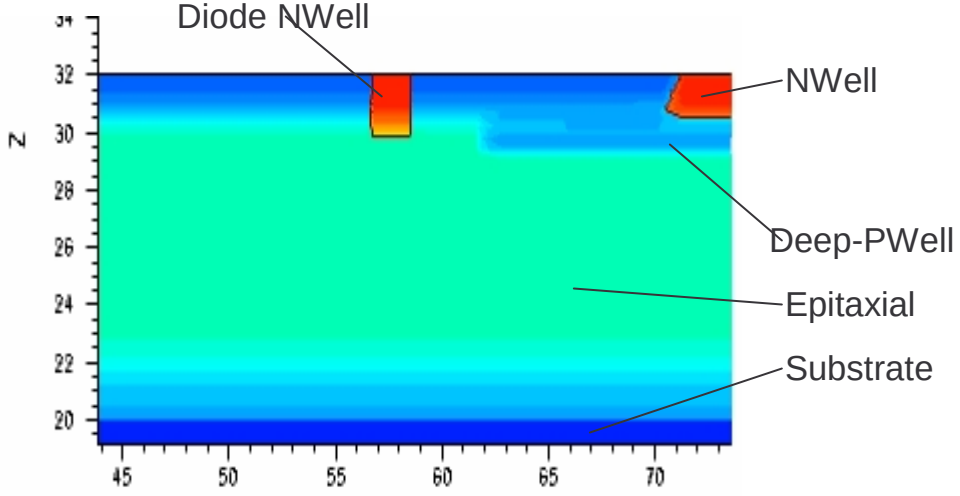
- Δv = 52 mV @ 250 e^-
- Noise =12 mV (8 fF)
- S/N = 4.33 (Sg = Ng)
- e^-_{in} ~ 57 e^-

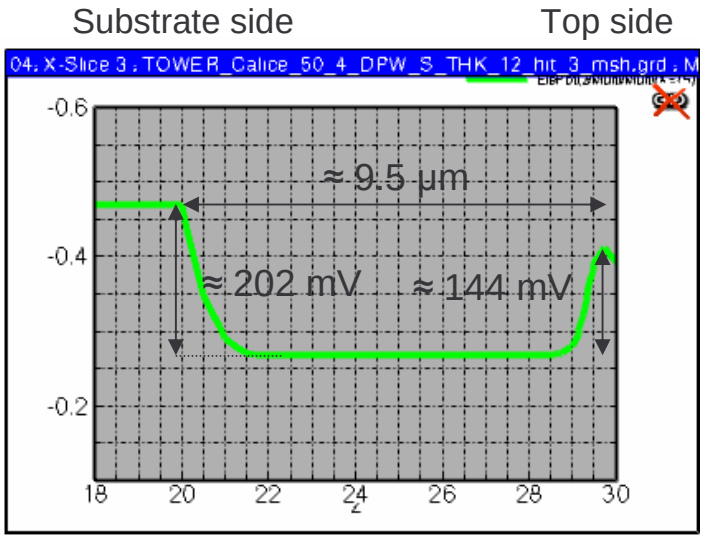


CALICE MAPS design

Optimization MAPS process

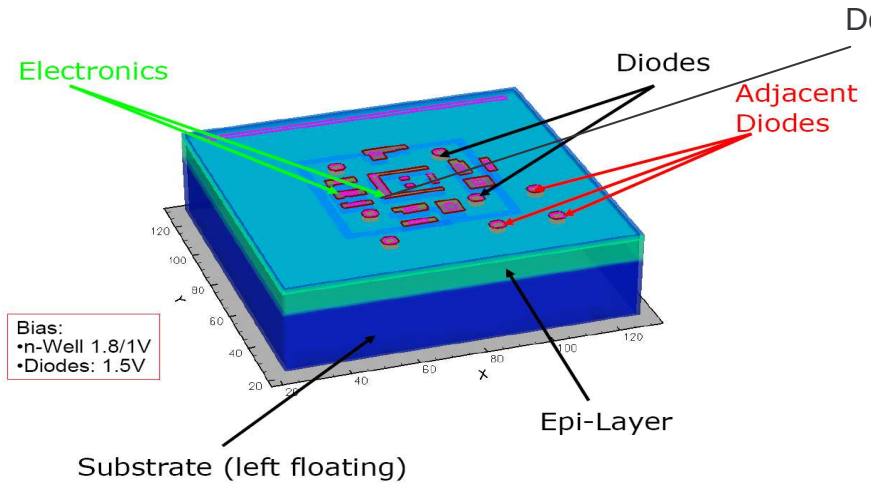
- Using Pwell implant to shield N-well housing readout electronic
- Improvement in charge collection
- Optimization of the diode location and size is necessary

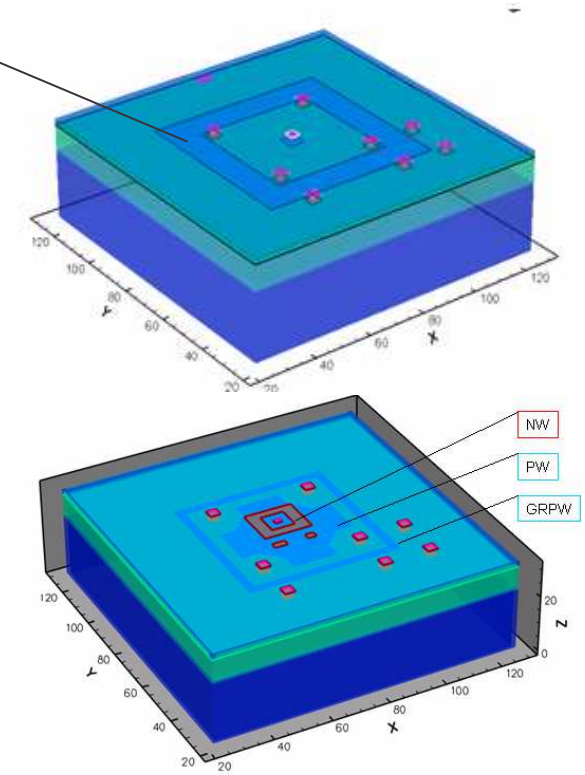




Electric potential in epitaxial layer12µm

CALICE MAPS design - pixel simulation -

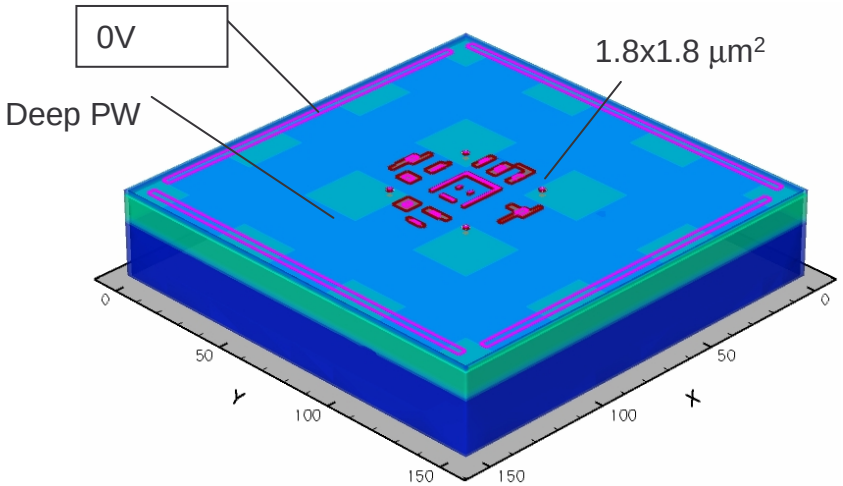


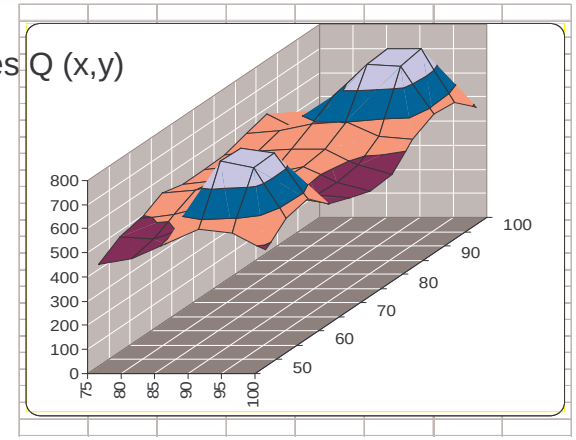


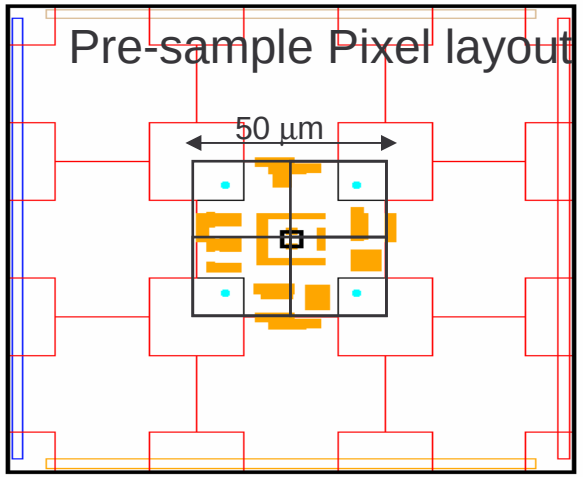
- Several Deep P W layouts studied
- Optimization of collecting diodes **size and location** given the electronic design constraints

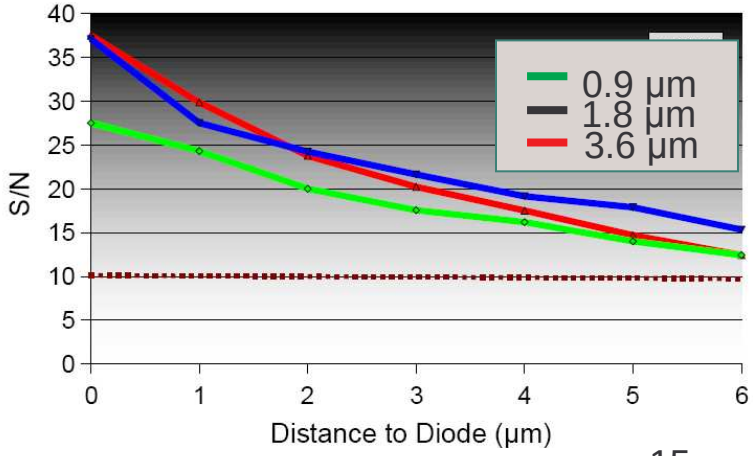
Cell size: 50 x 50 μm^2

CALICE MAPS design - pixel simulation -







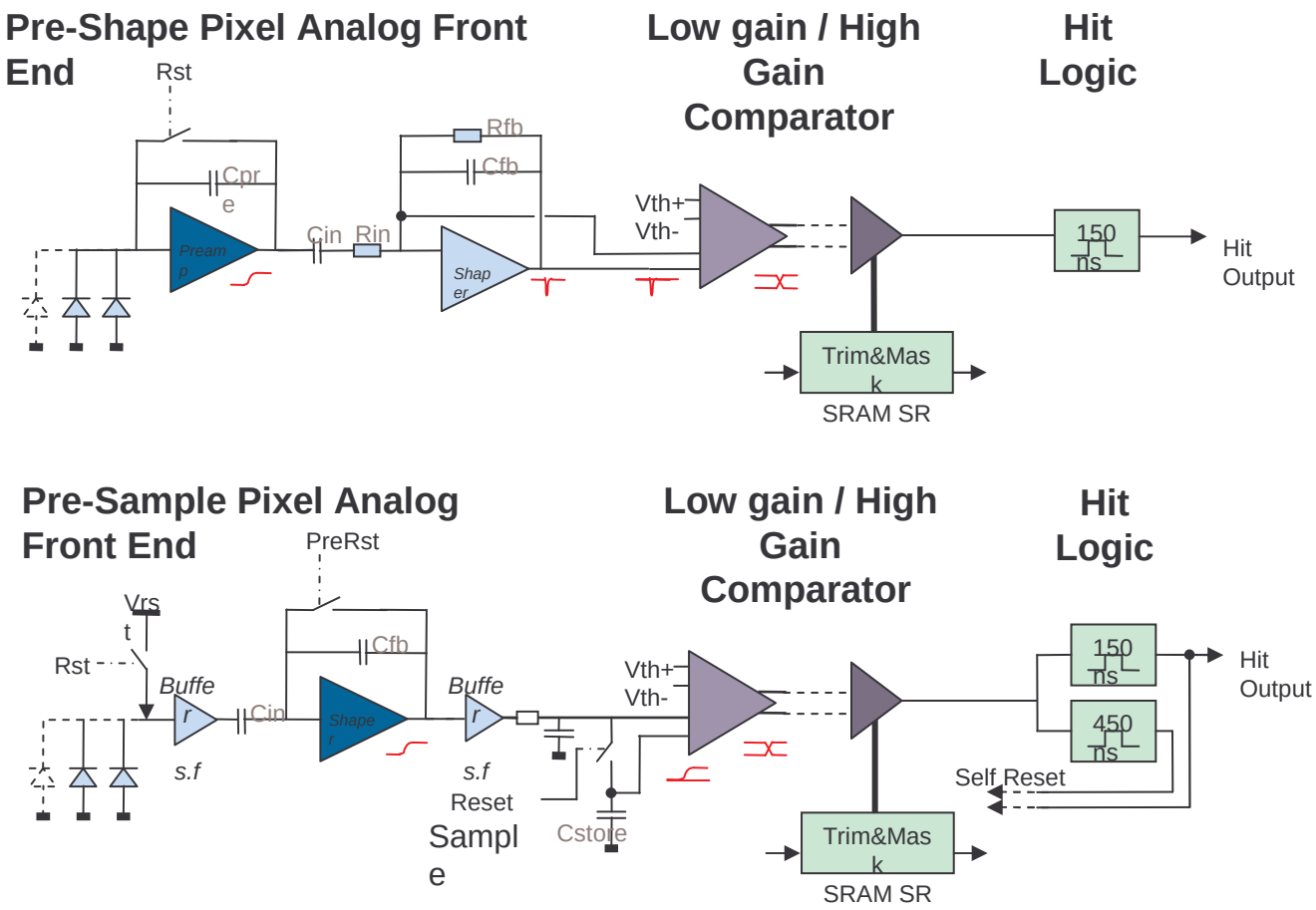


Pre-Shape:
Pixel reset before start of bunch train
Stand by in readout
Hit event generates one time hit-flag to the logic
CR-RC shaper decays according to input amplitude then is ready to accept next event

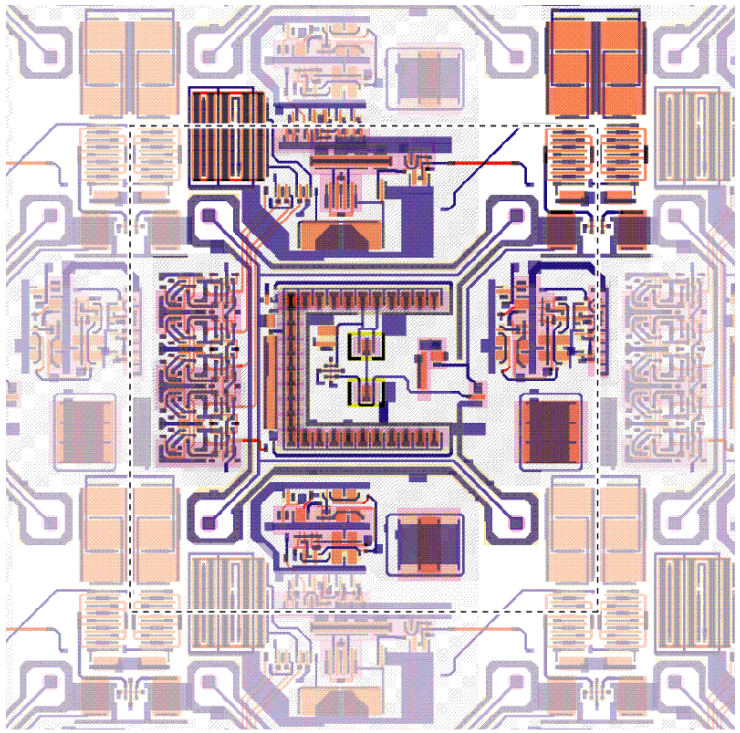
Pre-Sample:
Pixel reset before start of bunch train and automatically after local hit during bunch train
Stand by in readout
CA output sampled after Reset and then real-time difference input to comp

Expected similar noise characteristics from both designs

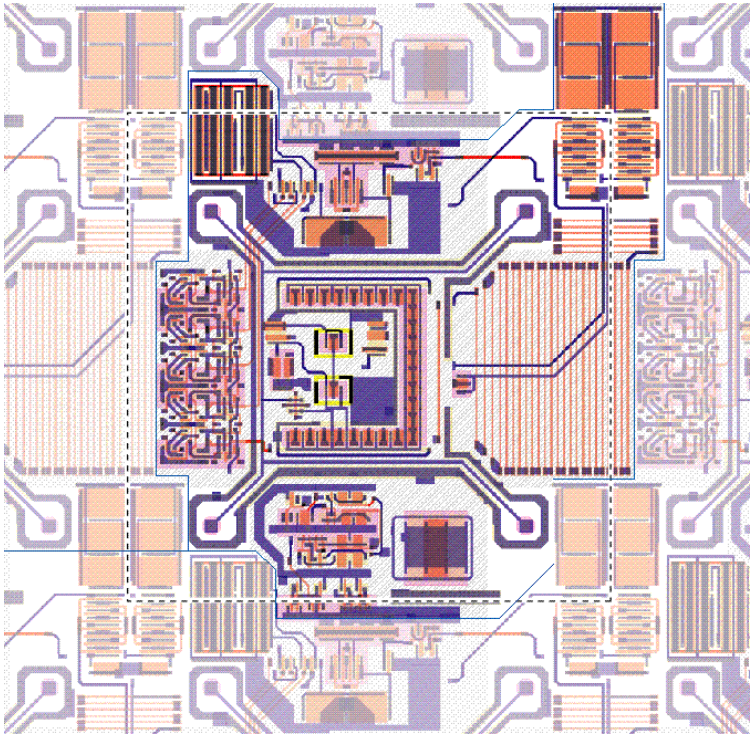
CALICE MAPS design - readout



CALICE MAPS design - pixel layout -

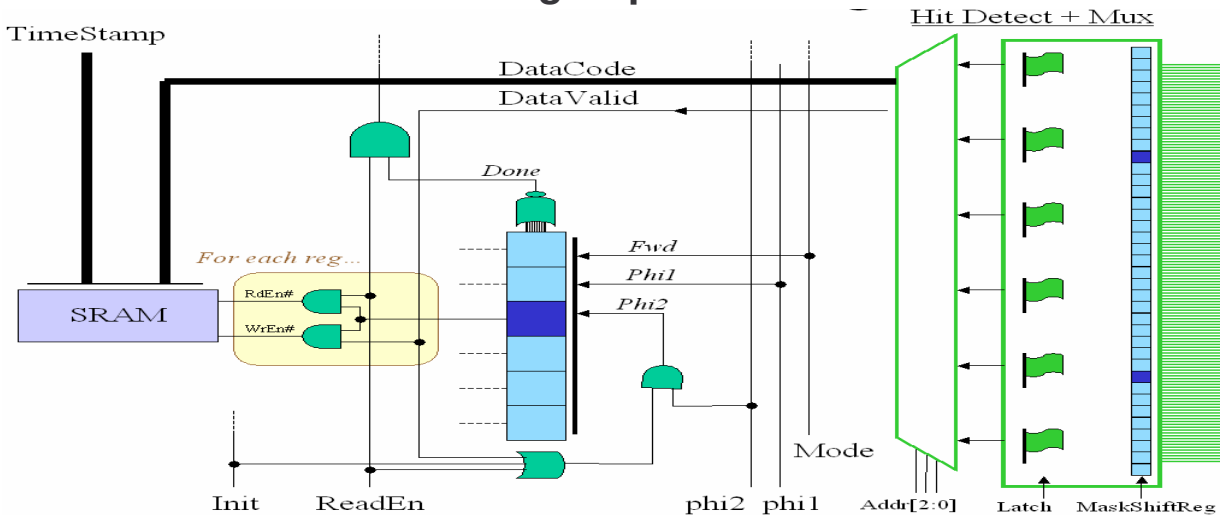


Pre-sample layout



Pre-shape layout

CALICE MAPS design - pixel architecture -



- Each digital block serves 42 pixels from one row
- Row split into 7 groups of 6 pixels
- Following a hit, for each row the logic stores in SRAM time stamp(13 bits), pattern number (3 bits), pattern (6 bits)
- 22 bits/hit + 9 bits row encoding = 31bits/hit
- Register for masking out noisy pixels

CALICE MAPS design - pixel architecture -

- 1*1 cm² in total
- 2 capacitor arrangements
- 2 architectures

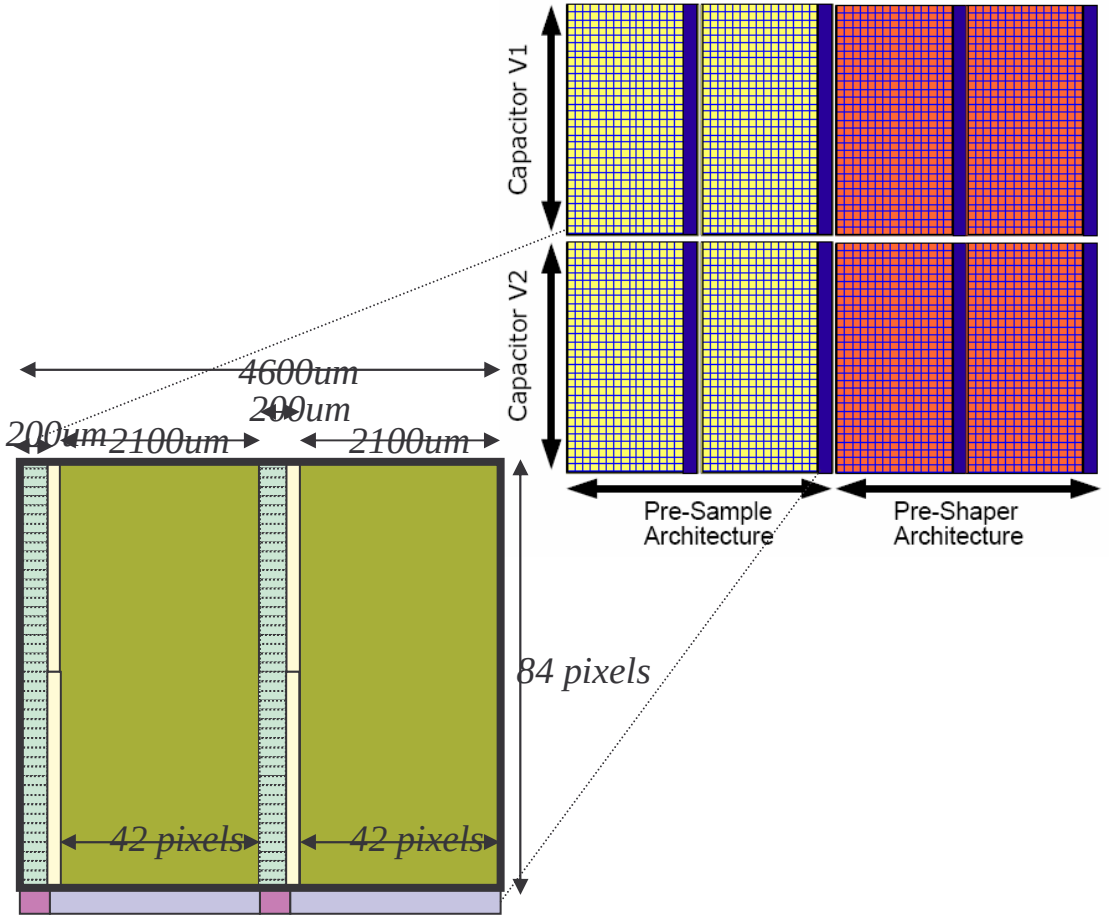
6 million transistors, 28224 pixels

- Estimated power:

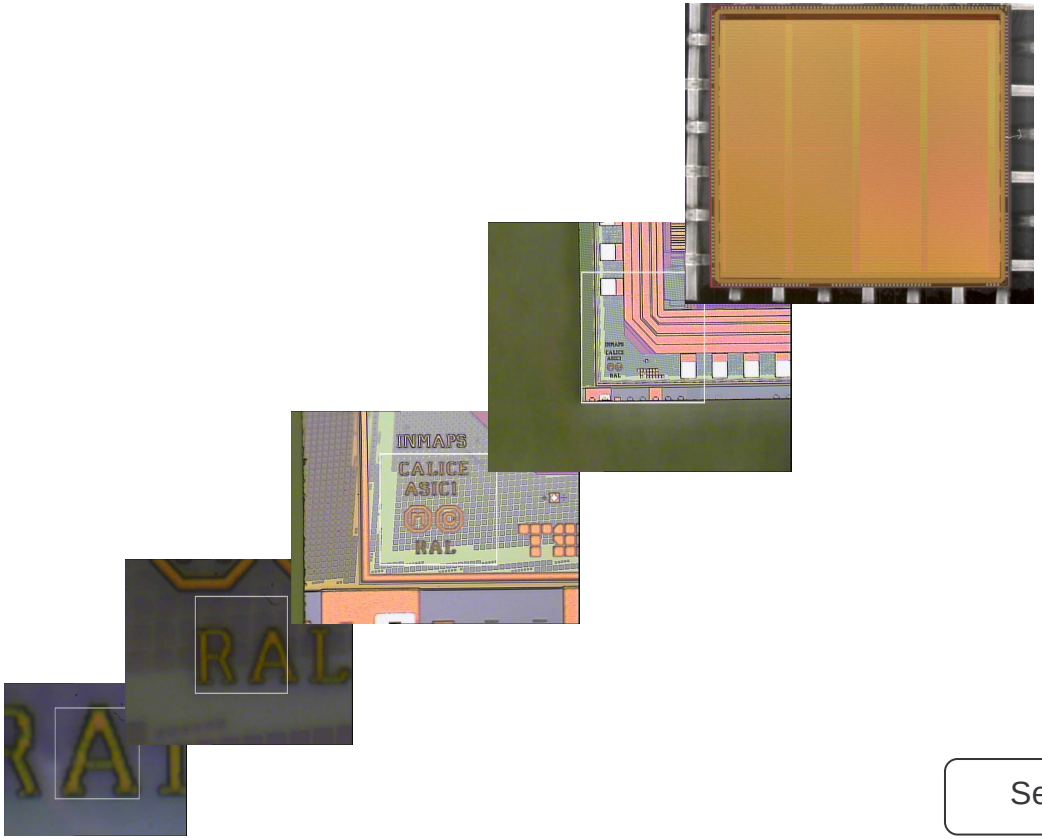
≈10 μW/pixel continuous

≈40μW/mm² including 1% duty factor

- Dead area ≈200 μm every 2 mm
- Each sensor could be flip-chip bonded to a PCB

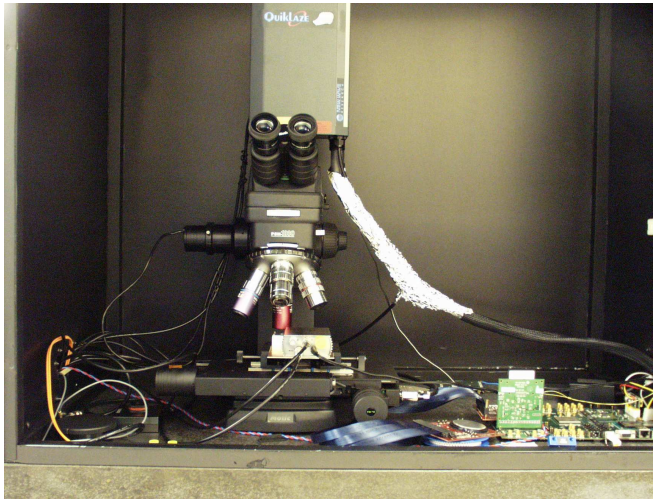


CALICE MAPS design – pixel architecture



Sensor microphotograph

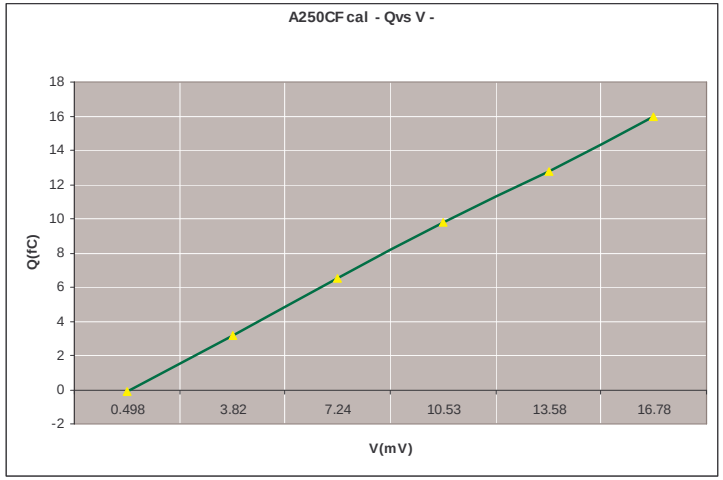
CALICE MAPS - RAL test setup -



Laser MIP

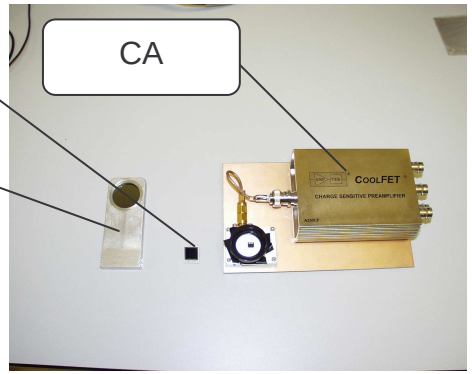
- Three wavelength laser:
  λ=1064, 532,355 nm,
  focusing < 2 μm,
  pulse 4ns, 50 Hz repetition,
- Labview Control software
- MIP Calibration: Si reference detector coupled to low noise CA + differentiator (no shaper) A250CF peltier cooled
- Amplifier Gain measured ~ 7mV/MIP
- Amount of stray light and EMP reduced within the laser test setup

CALICE MAPS - RAL test setup -



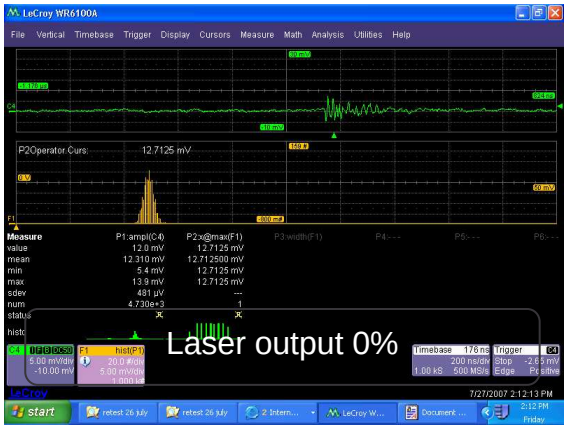
Reference sensor

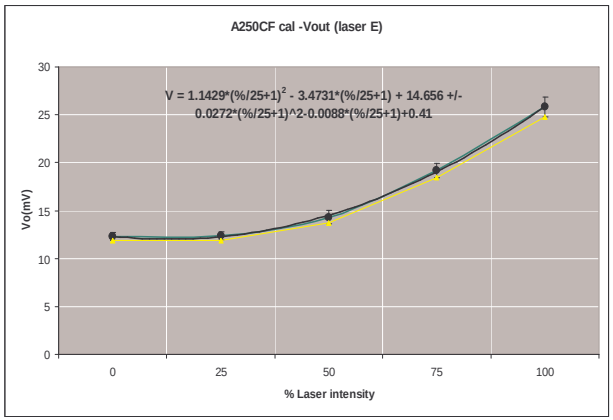
ND filter



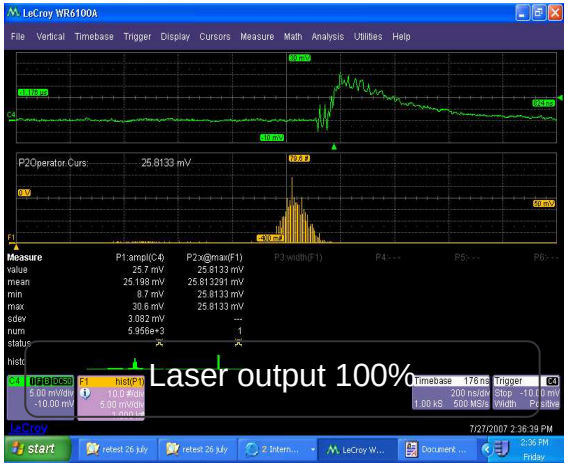
A250CF calibration using injected charge through capacitor and pulse generator

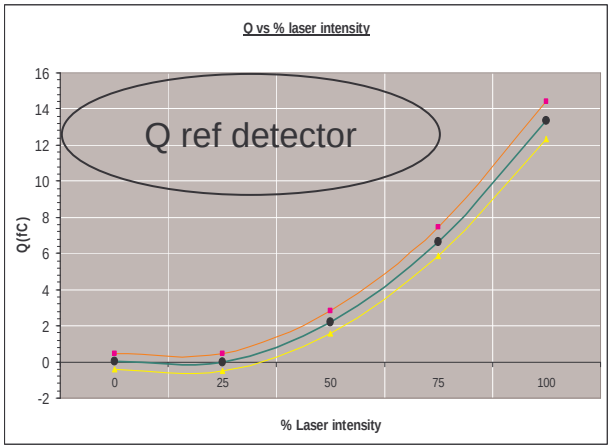
CALICE MAPS - RAL test setup -

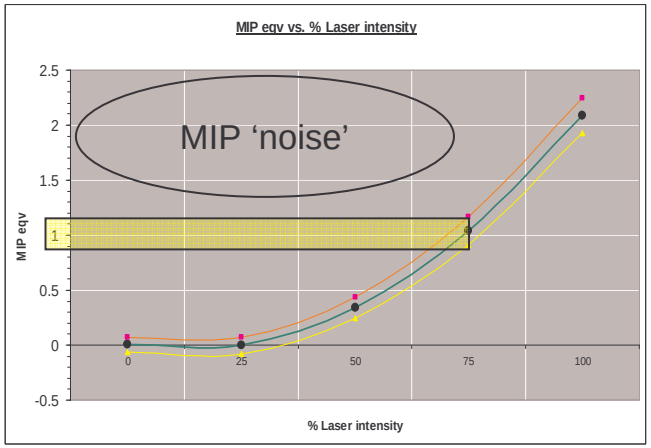




- A250CF output vs. Laser intensity
- Q injected vs. Laser intensity
- MIP-equivalent vs. Laser intensity
- Sub-MIP resolution AND accuracy capability (λ = 1064nm, spot size = 2μm)



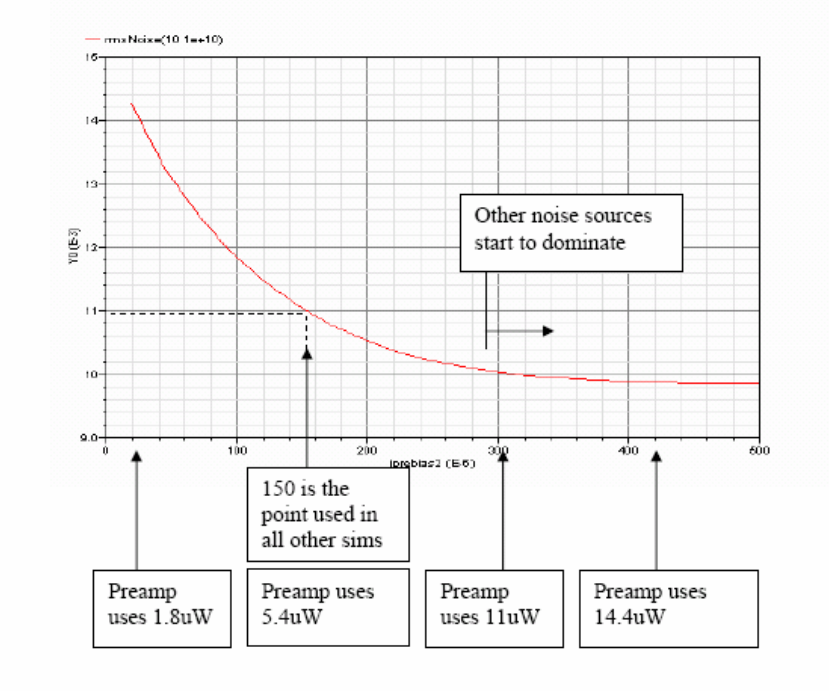




Conclusions

- MAPS-based ECAL can potentially offer a number of advantages in terms of performances and overall cost
- Novel INMAPS process for MAPS might have significant advantages in terms of charge collection efficiency
- Pixel design and readout electronics optimized for charge collection and S/N
- First design aims at demonstrating feasibility of the approach and to achieve significantly high S/N
- Power dissipation still high and needs to be addressed
- Test setup ready
- Chip testing underway now

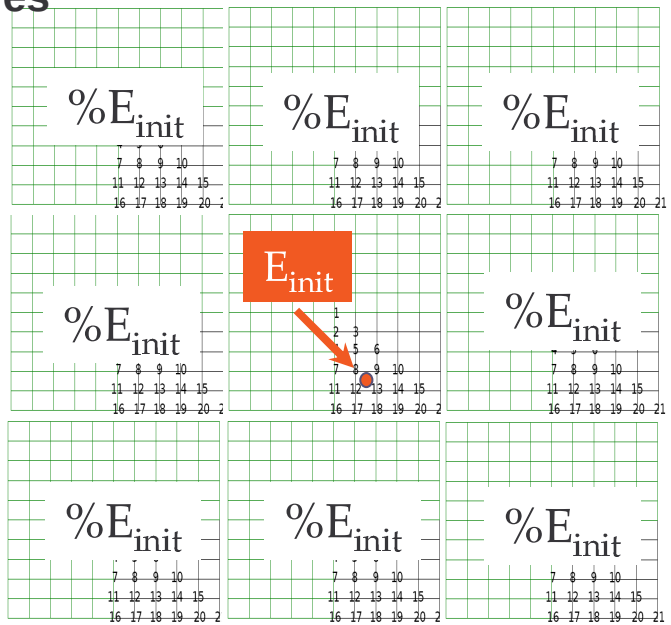
CALICE MAPS backup slides



CALICE MAPS backup slides

Geant4 E_{init} in 5x5 μm² cells

Apply charge spread
$E_{after\ charge\ spread}$



Register the position and the number of hits above threshold

+ noise only hits :
proba 10^{-6} Ł ~ 10^6 hits in the whole detector
BUT in
a 1.5*1.5 cm² tower : ~3 hits.

Importance of the charge spread :

$$\sum E_{neighbours} \sim (50\% - 80\%) \times E_{init}$$

Add noise to signal hits
with σ = 100 eV
(1 e- ~ 3 eV Ł 30 e- noise)

Sum energy in
50x50 μm² cells
E_{sum}

CALICE MAPS backup slides

- Stave structure
- Lack of hybrids/ASIC allow less complex/thinner PCB
- Thinner sensors (down to 100 μm)
- Bump-bond MAPS