



# A CMOS Monolithic Active Pixel Sensor with Analog Signal Processing and 100% Fill Factor

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# Introduction

SiW ECAL for ILC

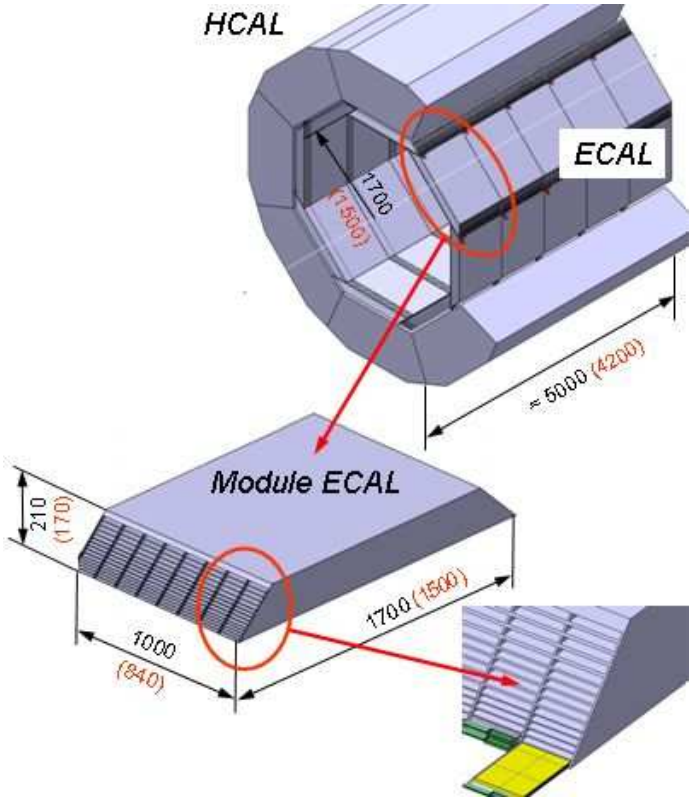
- 30 layers silicon & tungsten
- Prove Monolithic Active Pixel Sensor (MAPS) as a viable solution for the silicon!

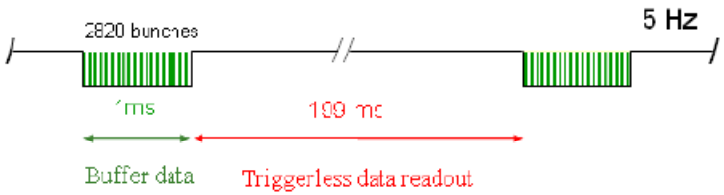
Pixel Specification

- MIP signal (~450e-)
- Noise rate $10^{-6}$
- Binary readout from 50micron pixels

Machine operation

- 150ns max bunch crossing rate
- 199ms between bunch trains for readout



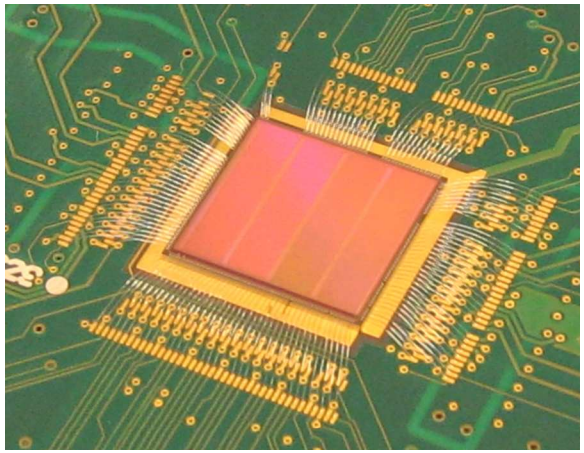



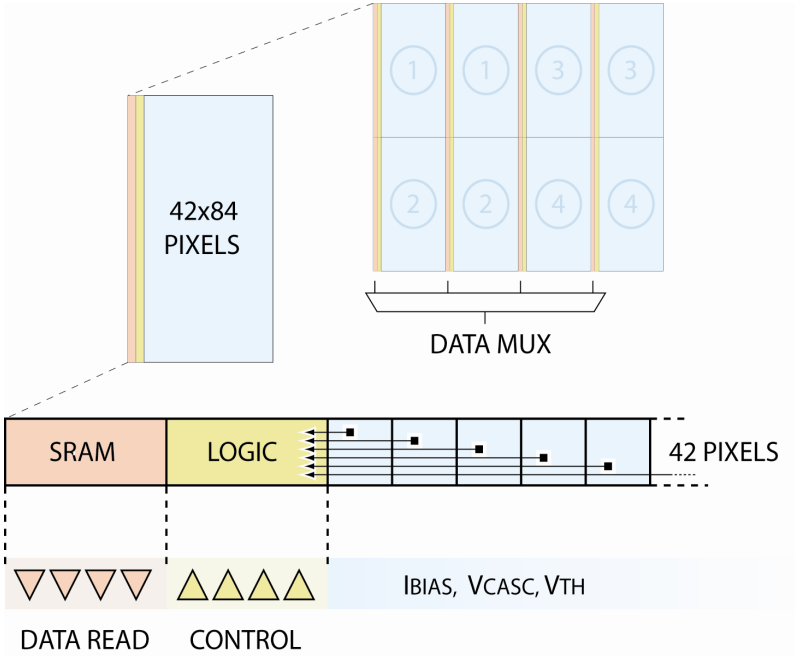
# Test Chip Overview

- 8.2 million transistors
- 28224 pixels; 50 microns; 4 variants
- Sensitive area 79.4mm2
  - *of which 11.1% "dead" (logic)*

- Four columns of logic + SRAM
  - Logic columns serve 42 pixels
  - Record hit locations & timestamps
  - Local SRAM

- Data readout
  - Slow (<5Mhz)
  - Current sense amplifiers
  - Column multiplex
  - 30 bit parallel data output

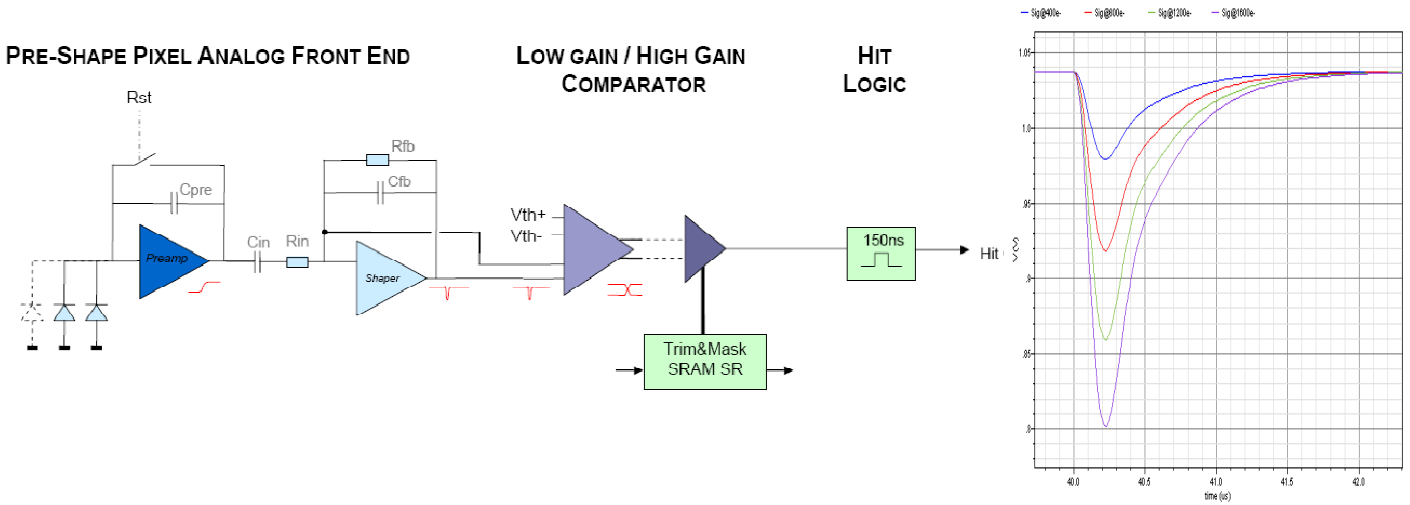




# Pixel Architectures

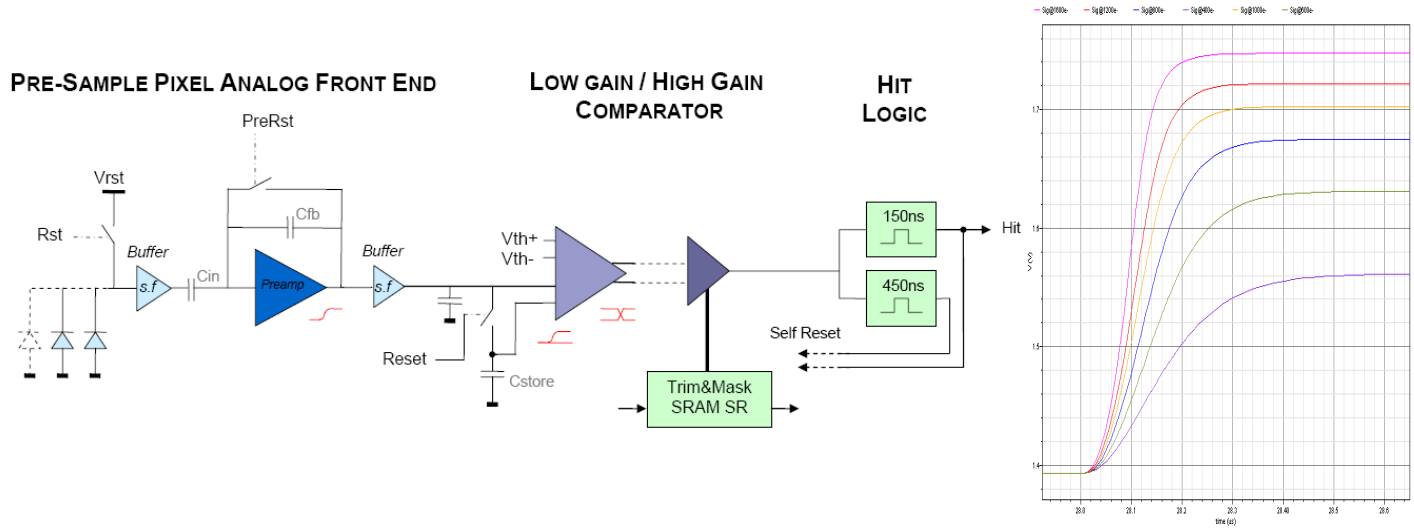
## preShape

- Gain 94uV/e
- Noise 23e-
- Power 8.9uW
- 150ns “hit” pulse wired to row logic
- Shaped pulses return to baseline




## preSample

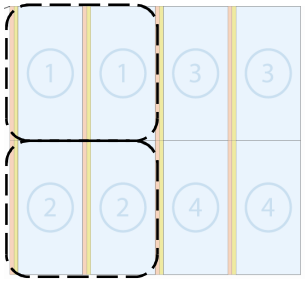
- Gain 440uV/e
- Noise 22e-
- Power 9.7uW
- 150ns “hit” pulse wired to row logic
- Per-pixel self-reset logic



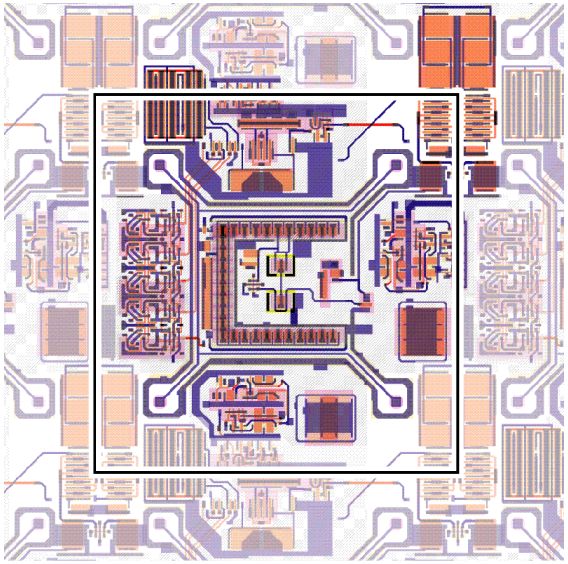
# Pixel Layouts

## preShape Pixel

- 4 diodes
- 160 transistors
- 27 unit capacitors

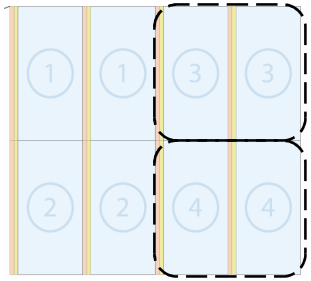



- Configuration SRAM
  - Mask
  - Comparator trim (4 bits)
- 2 variants (①,②): subtle changes to capacitors

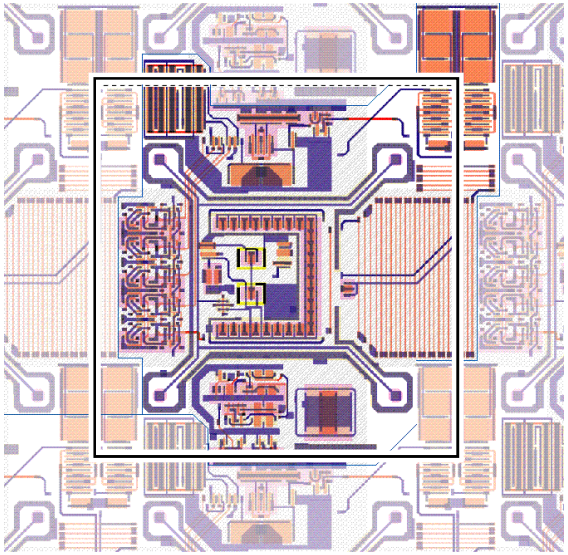


## preSample Pixel

- 4 diodes
- 189 transistors
- 34 unit capacitors
- 1 resistor (4Mohm)




- Configuration SRAM
  - Mask
  - Comparator trim (4 bits)
- 2 variants (③,④): subtle changes to capacitors

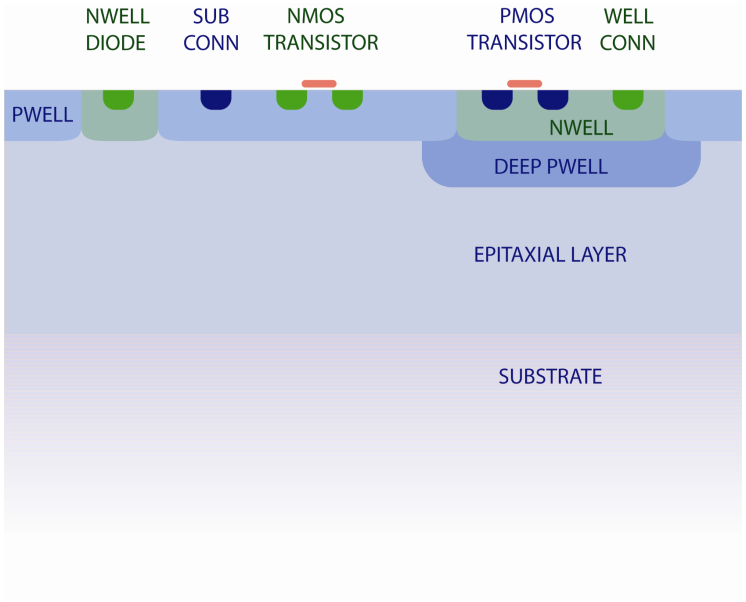


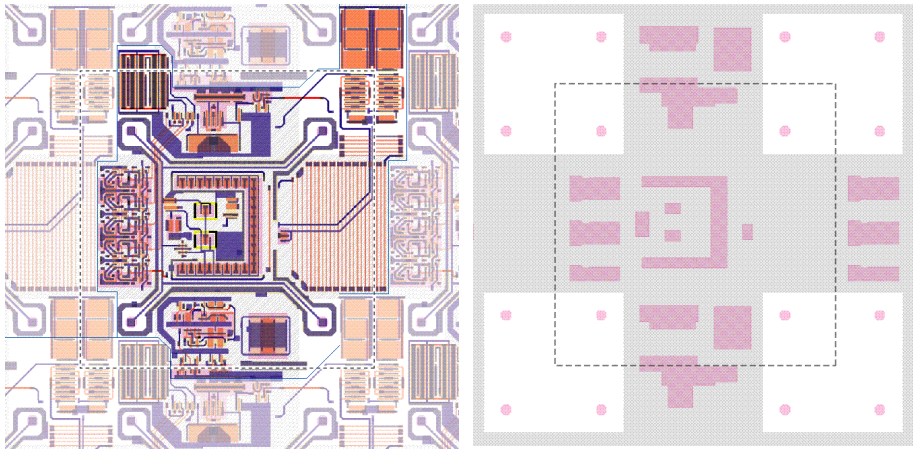
# INMAPS Process

- Standard 0.18 micron CMOS
- 6 metal layers used
- Analog & Digital VDD @ 1.8v
- 12 micron epitaxial layer

- Additional module: Deep P-Well
  - Developed by foundry for this project
  - Added beneath all active circuits in the pixel
  - Should reflect charge, preventing unwanted loss in charge collection efficiency

- Test chip processing variants
  - Sample parts were manufactured with/without deep p-well for comparison



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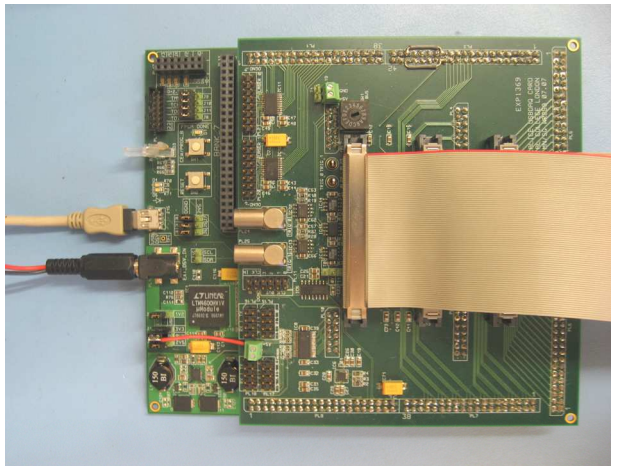
# Prototype Testing

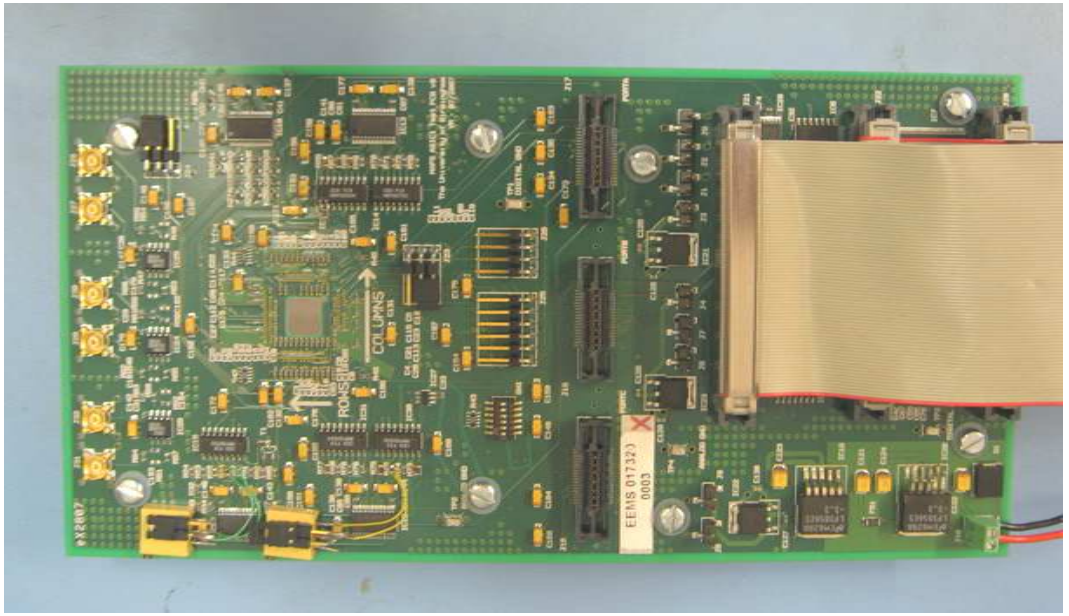
FPGA Based DAQ

- Xilinx
- USB2
- Master/Slave modes
- Laser/PMT interfaces



Cable Link

- 3x80 Flat ribbon
- LVDS 50Mhz (max)



Sensor card

- Rear mounted sensor
- Voltage & current DACs
- Logic Analyzer Ports
- LVDS I/O
- Power regulators

# Preliminary Tests: Proof of Life

Pixel Configuration

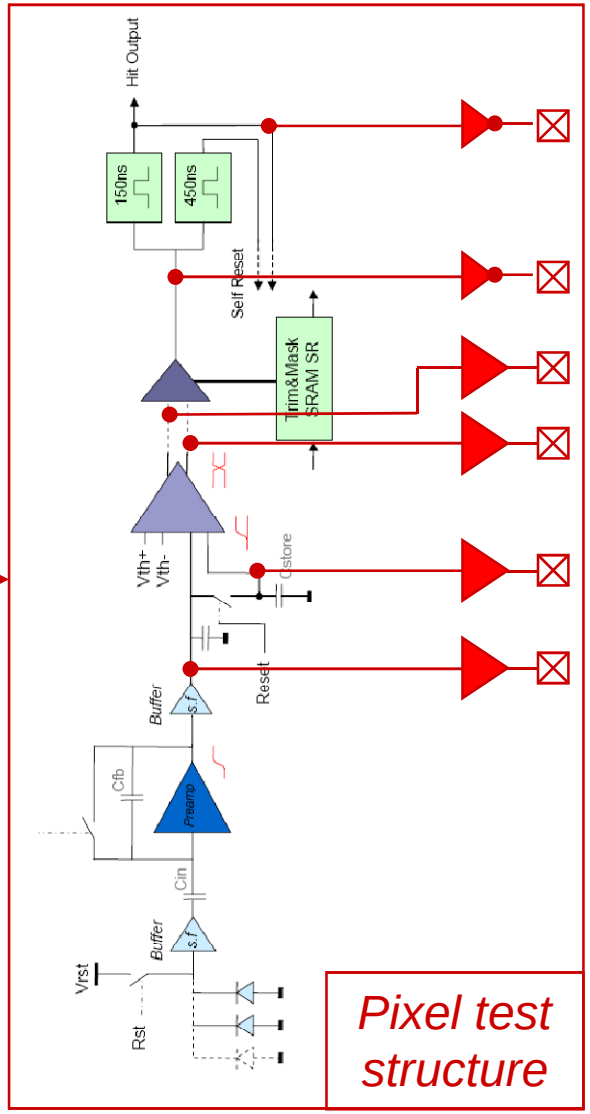
- Write & read back random config data with no errors

Digital Logic

- Operate all four columns in “override” mode which fills SRAMs with false hits
- Row, timestamp, mux and hit pattern data look correct for “override” mode (on Logic analyzer)

PreSample test pixels

- Monostables generate pulses
- Comparator switches; TRIM settings adjust threshold
- Pixel signal output shows saturation due to ambient light
- Voltage step on Vrst shows output pulse, which can be reset

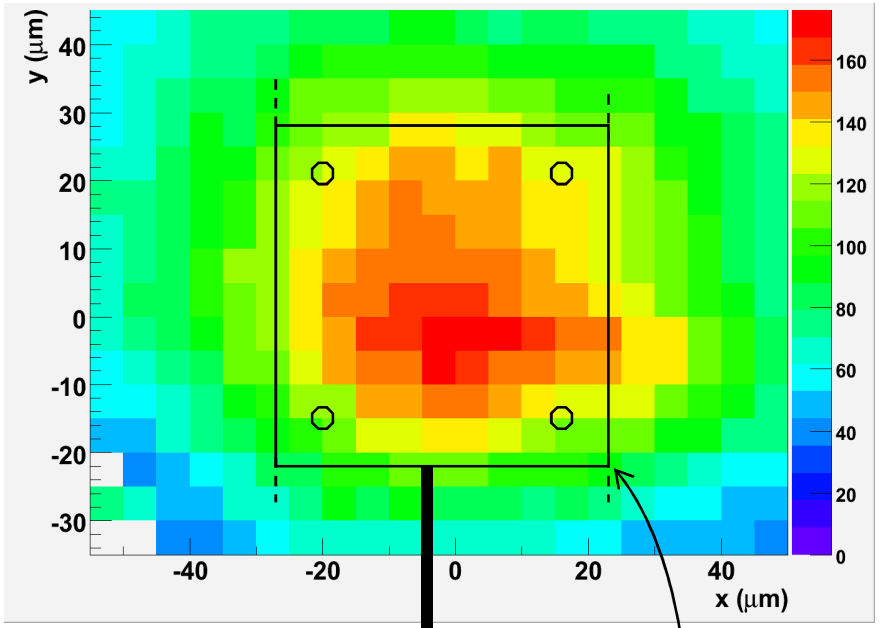


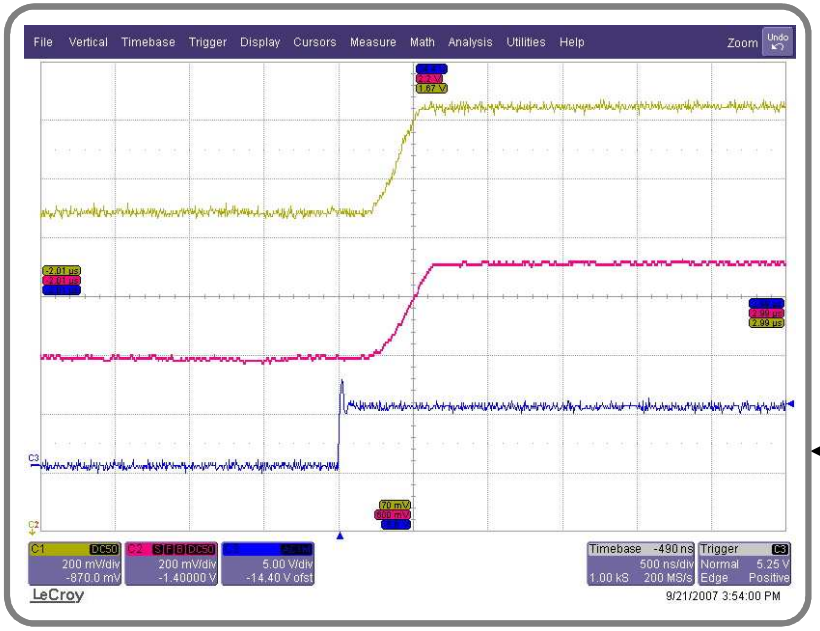
# Preliminary Tests: Laser Scan

## Focussed Laser

- 4ns pulse at 1064nm wavelength
- Focussed to 4x4 micron on rear of sensor
- Exact signal unknown
- Step by 5um in x and y
- Record & plot signal step size for each position

*12um epi + DPW*




*Test pixel outline overlaid for scale: exact position unknown!*

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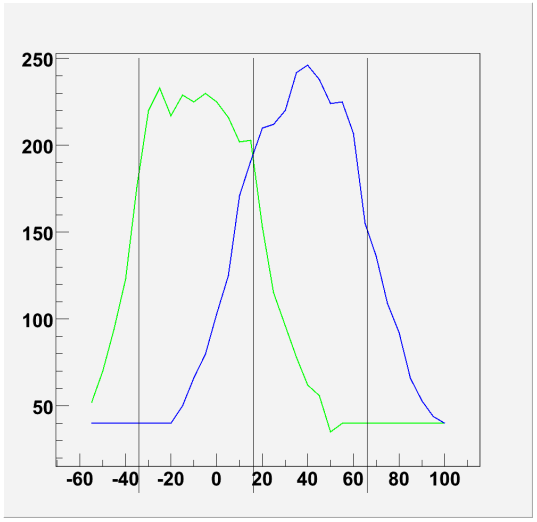
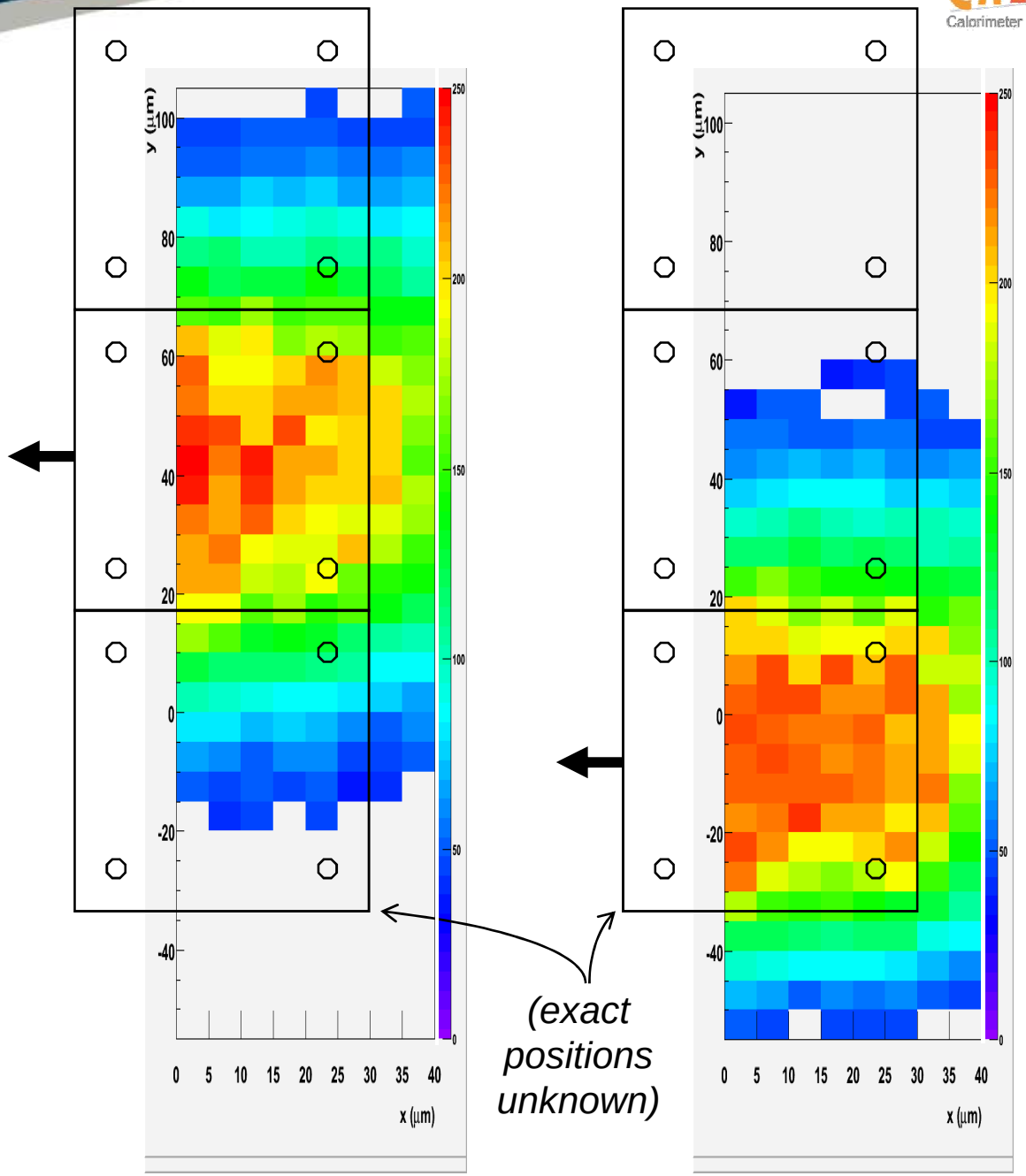
# Laser Scan

- Two neighbour test pixels
- Laser focussed to 5x5 micron
- Step by 5um in x and y
- No other diodes around these test pixels



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# Summary & Future

- Preliminary results
  - Proof of life from novel new MAPS test sensor
  - Charge collection observed
  - Proof of principle; deep P-well

- Immediate Future
  - PCBs in manufacture
  - Quantitive evaluation of sensor performance
    - Fe55 source
    - Laser scan
    - Cosmics (stack of 4 sensors)
    - Beam test

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# Second Sensor

- Larger format
  - Reticule size ~ 25x25mm
  - Minimised dead area
  - Minimised number of I/O pads, suitable for bump bonding
  - Will be tiled to create 15x15cm square array for beam test
- Pixel design
  - Selected from one of the variants based on test results
  - Optimisation?
  - Pixel pitch à 100 microns?
- System on chip
  - Integrated timecode & sequencing
  - Serial data output
  - Minimised number of control signals required
- Design submission: mid 2008


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# Is Finish

# Row Control Logic & Memory

- Hit signals from 42 pixels are sampled by external clock
  - (150ns/bunch crossing rate)
- To optimise use of local memory
  - Rows are divided into 7 parts
  - Each is interrogated in turn
  - The sub-pattern of hits is stored if any are present
- 19 SRAM registers
  - Timestamp
  - Mux address
  - Hit distribution
- Memory manager
  - Ensures each register is written once
  - Can raise a global overflow flag
  - Activates only the valid registers during readout