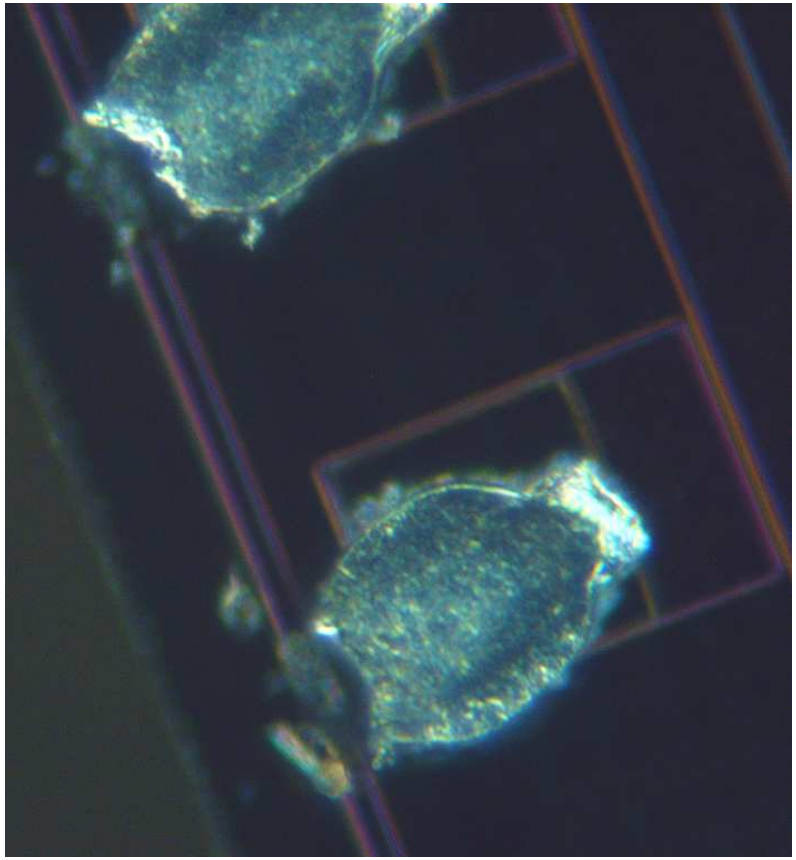
ASIC1

progress

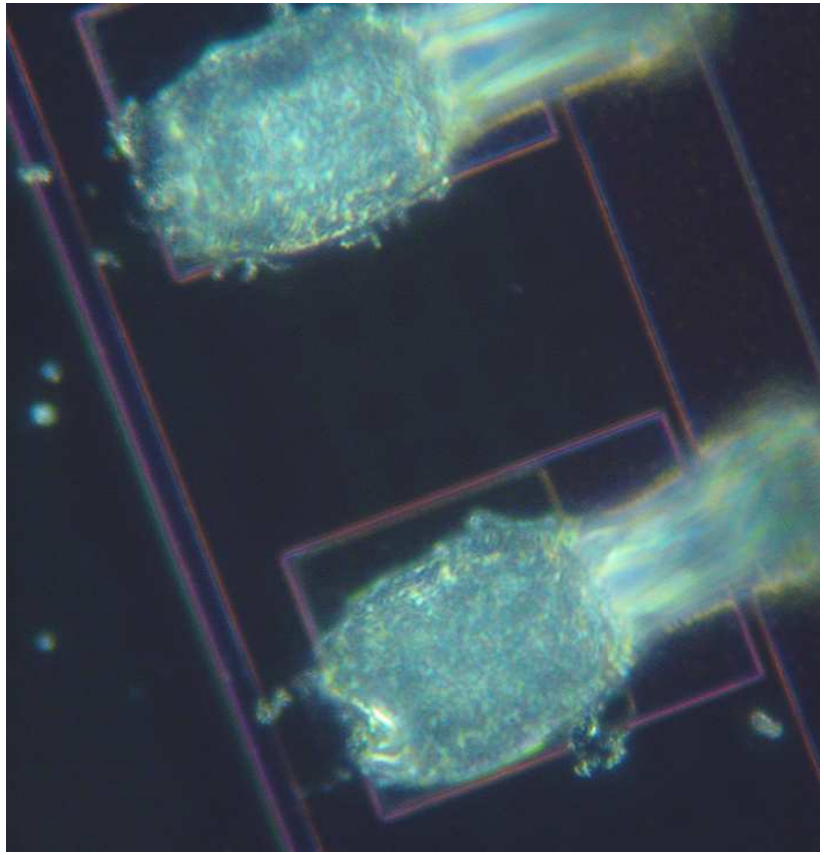
Jamie Crooks, Feb 08

Bonding Problems: Resolved

Shorts to seal ring discovered under bonds



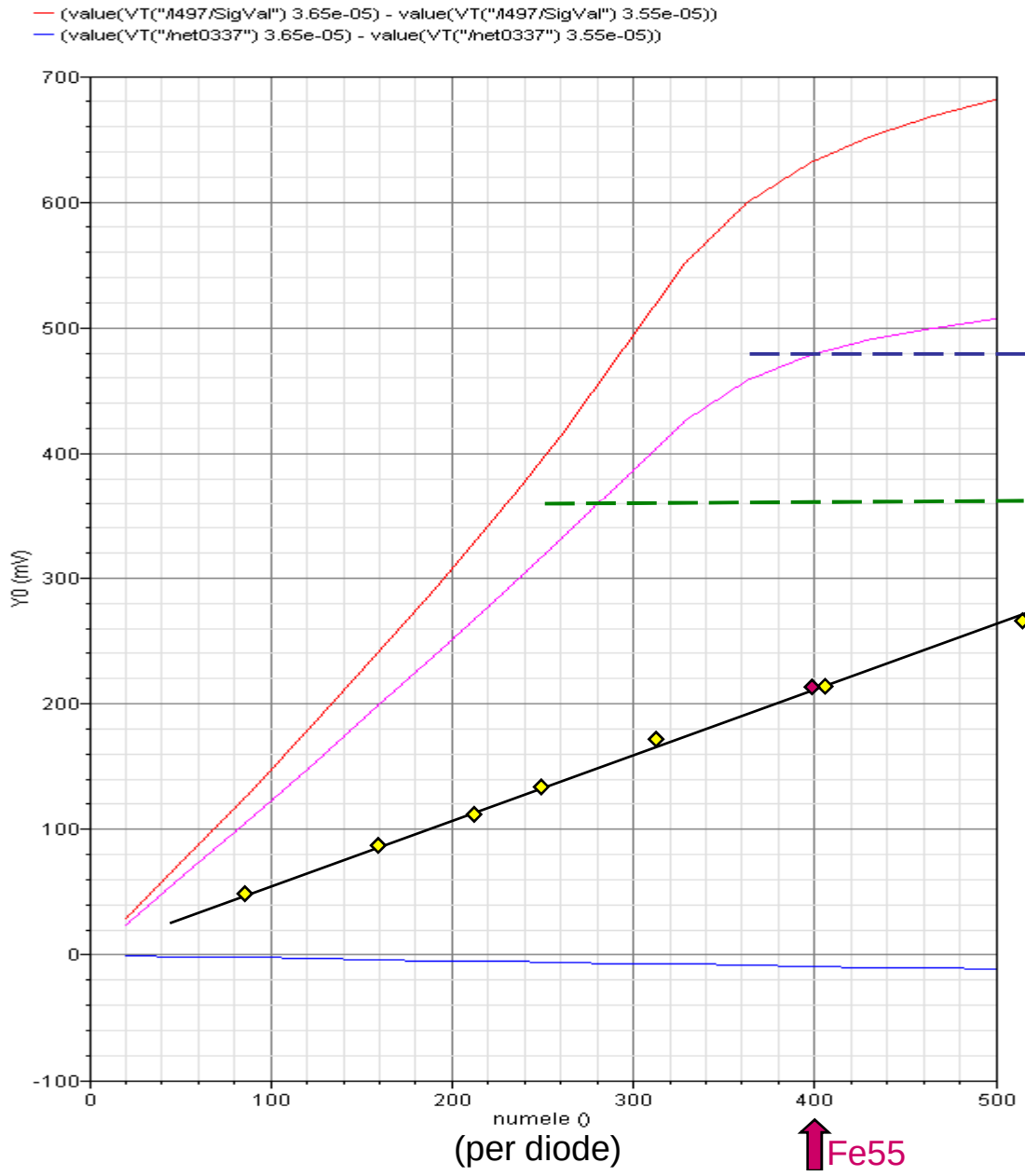
Smaller bonding wedge + revised program



Bonding Status

Bonded	#	Status	Wafer/Split	Location	Notes
22/1	1		12 +DPW	RAL TD (optics lab)	Threshold scan ok (some bumps, not completely normal)
18/1	9		12 +DPW	RAL TD (optics lab)	reworked with new bond program: shorts on pix/aco/dco power nets
29/1	11		12 8 +DPW	IC	reworked with new bond program: threshold scan ok
29/1	15		12 8 +DPW	RAL TD (optics lab)	reworked with new bond program: (shapers bad; samplers good)
1/2	16		5 2 +DPW	RAL TD (optics lab)	reworked with new bond program: threshold scan ok
22/1	17		12 8 +DPW	RAL TD (optics lab)	reworked with new bond program: threshold scan ok
22/1	19		1 12 0 +DPW	RAL TD (optics lab)	reworked with new bond program: threshold scan fails (no RE signals?)

PreSample Test Pixel



Pixel node (ideal simulation)

(14fF parasitic on diode node)

Test Pad (ideal simulation)

Test Pad Sat. Limit (measured)

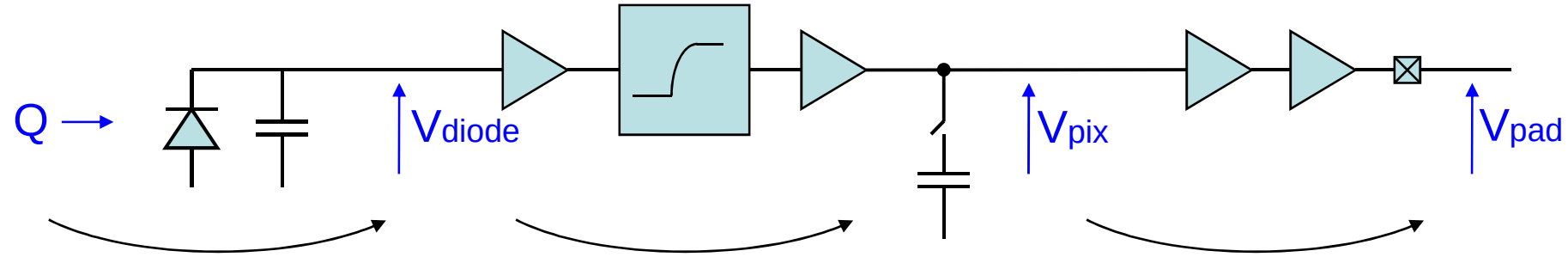
PCB Sat. Limit (measured)

Test Pad (measured)

(diode voltage step is applied through Vrst, signal step at pad is measured & plotted such that it corresponds to the diode node voltage step in the simulation)

Diode node (ideal simulation)

System overview: preSample test pixels



= 5.7 uV/e- (sim)

(Can be estimated from)

Gain ~0.8 from simulations

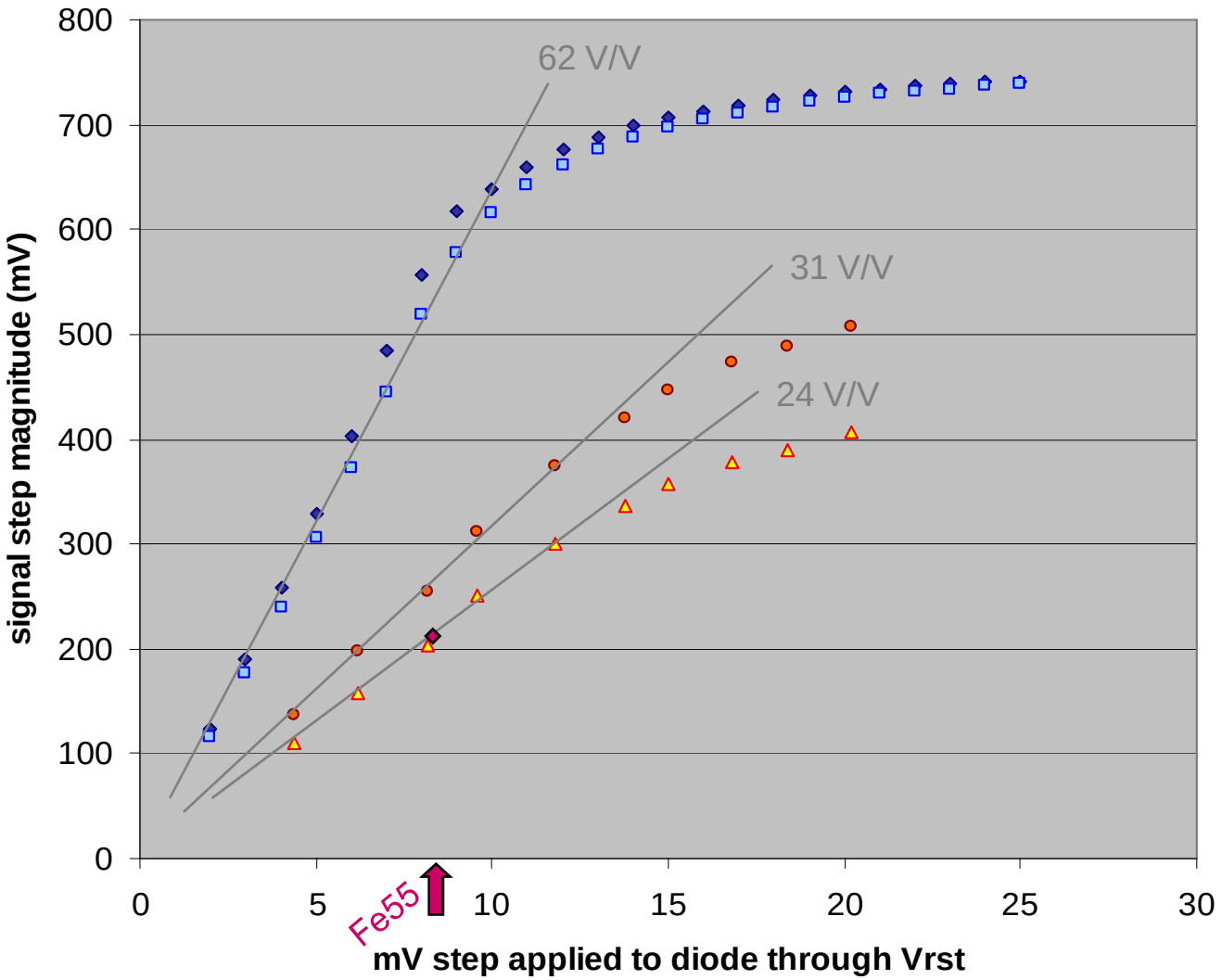
Can be measured by applying Vstep to Vrst holding pixels in reset

Can be simulated by placing a voltage pulse on the diode node

Fe55 measurement should give calibration of this gain

Can be simulated using ideal or parasitic extracted pixel models and injecting charge

Voltage gain

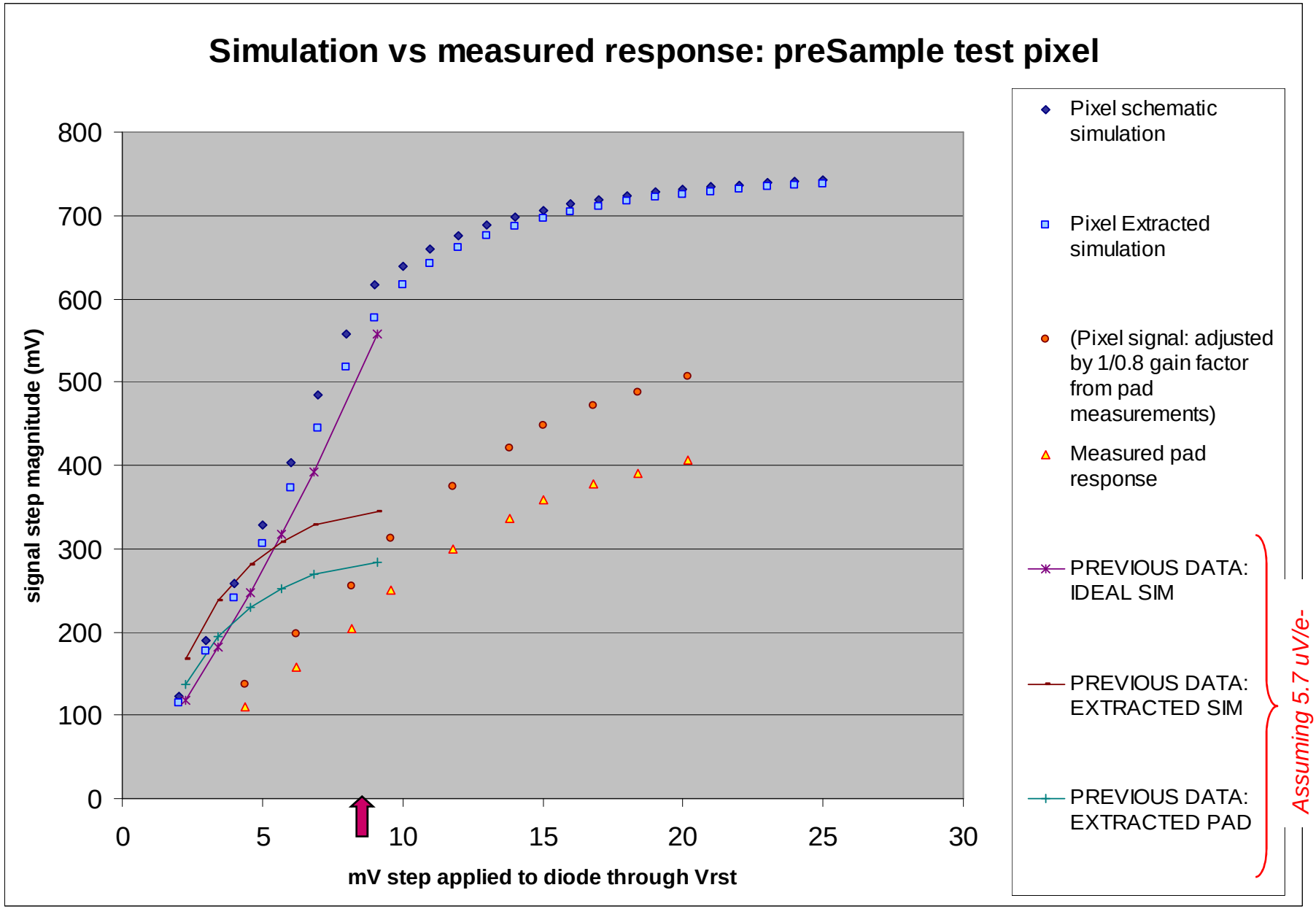


Simulations place an ideal voltage step on the diode node therefore independent of Cdiode

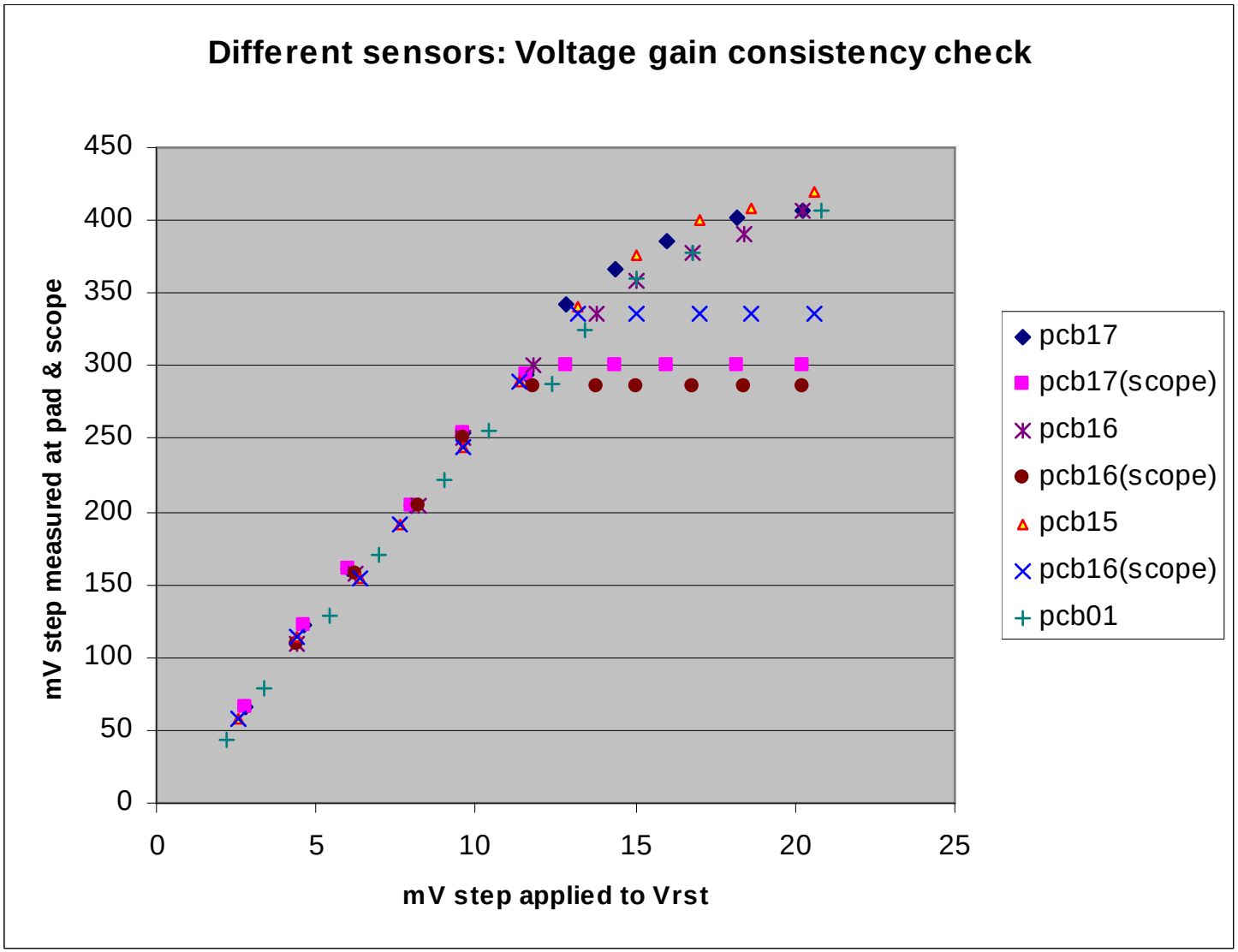
- Pixel schematic simulation
- Pixel Extracted simulation
- (Pixel signal: adjusted by 1/0.8 gain factor from pad measurements)
- Measured pad response

Measurements apply a voltage step on the diode node through the VRST transistor, therefore independent of Cdiode

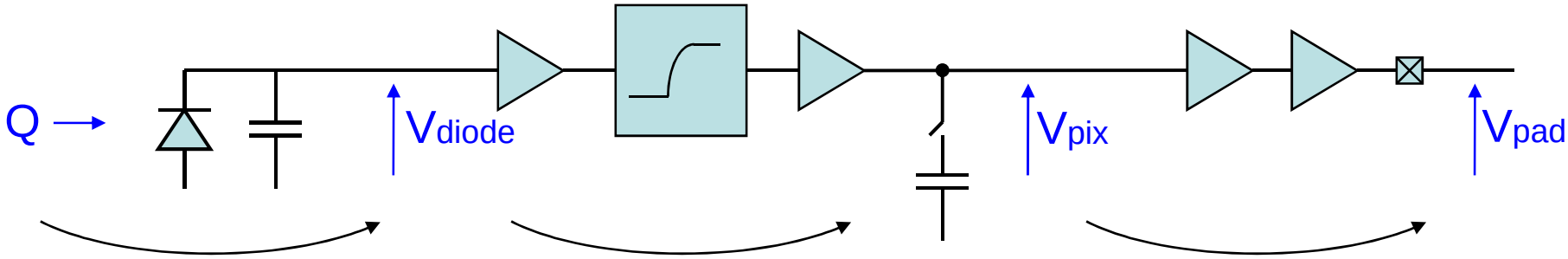
Compare with previous data



Measured voltage gain on 4 sensors



System overview: preSample test pixels



From Fe55 measurements = 130uV/e-

Est. from Fe55 meas. = 161uV/e-

= 31 V/V (est. from meas)

= 0.8 V/V (sim)

= 5.7 uV/e- (sim)

= 24 V/V (measured)

(136uV/e-)

These figures combined have been generally quoted before during design phase, in uV/e-

Any measurements taken with the test pixels will include the two buffer stages with gain<1

Noise

- Assumptions
  - We are in the linear region of test pixel
  - Parasitic capacitance estimate of diode node is ~correct
- System gain
  - from diode to pad

$$\frac{207\text{mV}}{1600\text{e-}} = 130\text{uV/e-}$$

- Noise
  - measured by Marcel at pad

$$= 3.5\text{mV}$$

  - referred back to diode using gain

$$\frac{3.5\text{mV}}{130\text{uV/e}} = 27\ \text{e-}$$

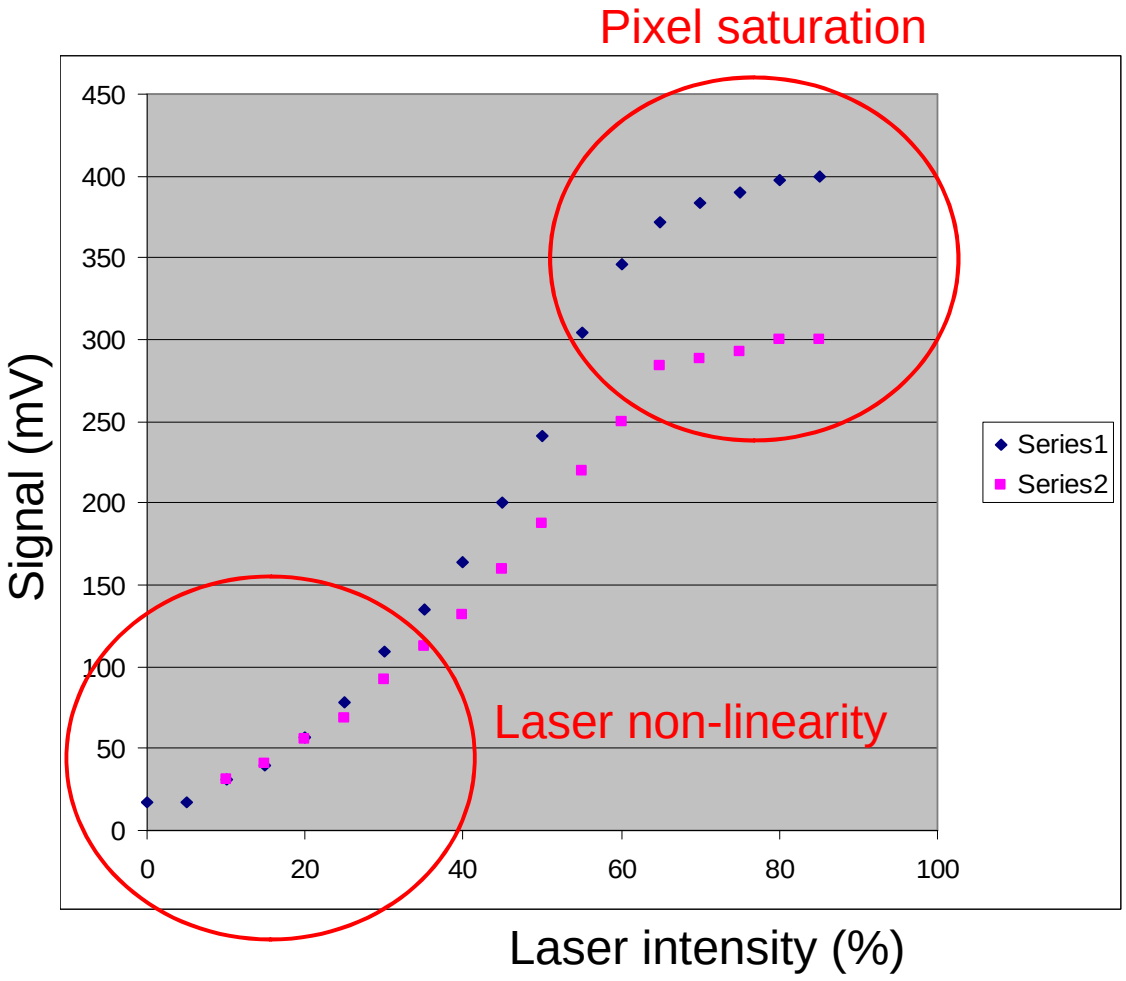
  - Will be sampled in-pixel during normal operation

$$27 * \sqrt{2} = 38\ \text{e-}$$

- SNR
  - Typical signal
  - Worst case signal in corner

$$\frac{250\text{e-}}{} = 6.5$$

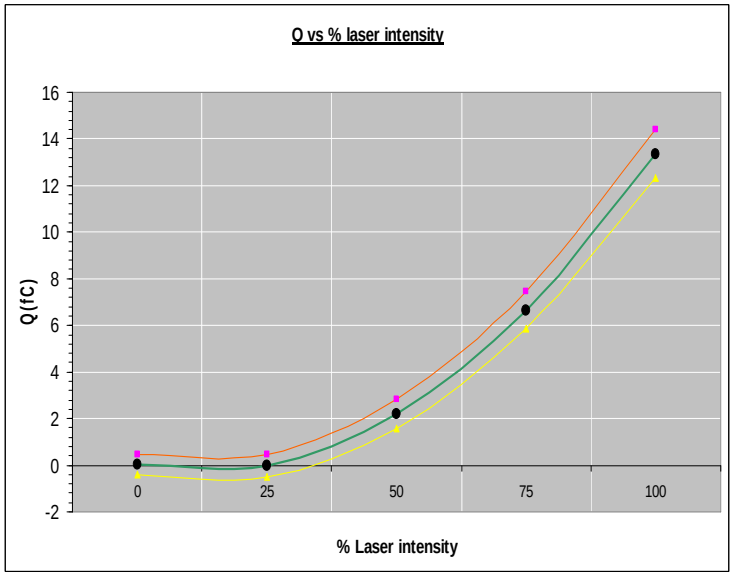
Linearity Measurements



Series1 Sensor 1: 12um epi +DPW;
(PCB modified for AC coupling)

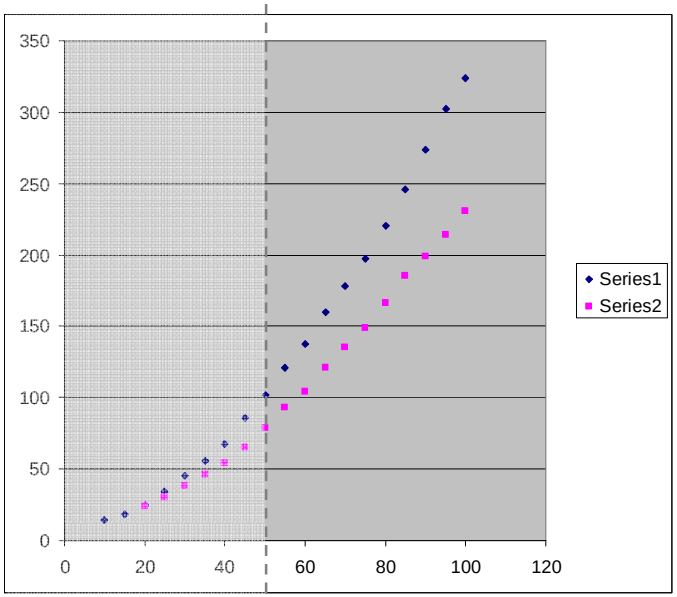
Series2 Sensor 16: 5um epi +DPW
(standard PCB design)

Giulio's laser calibration Aug 07

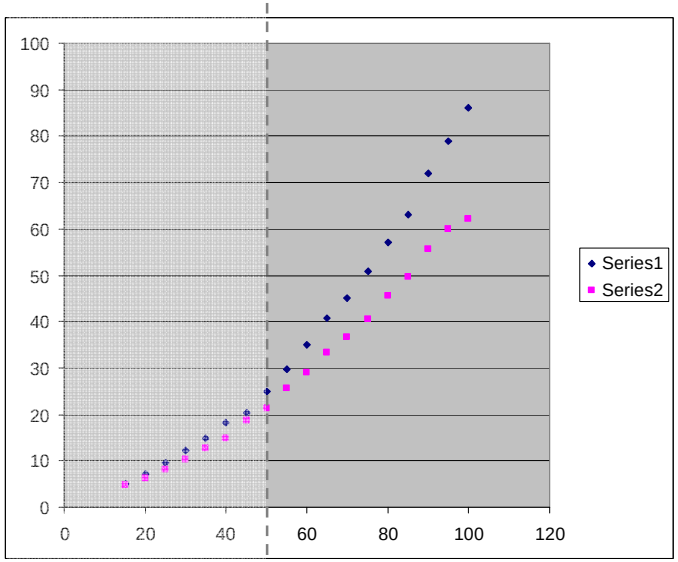


Linearity Sweeps

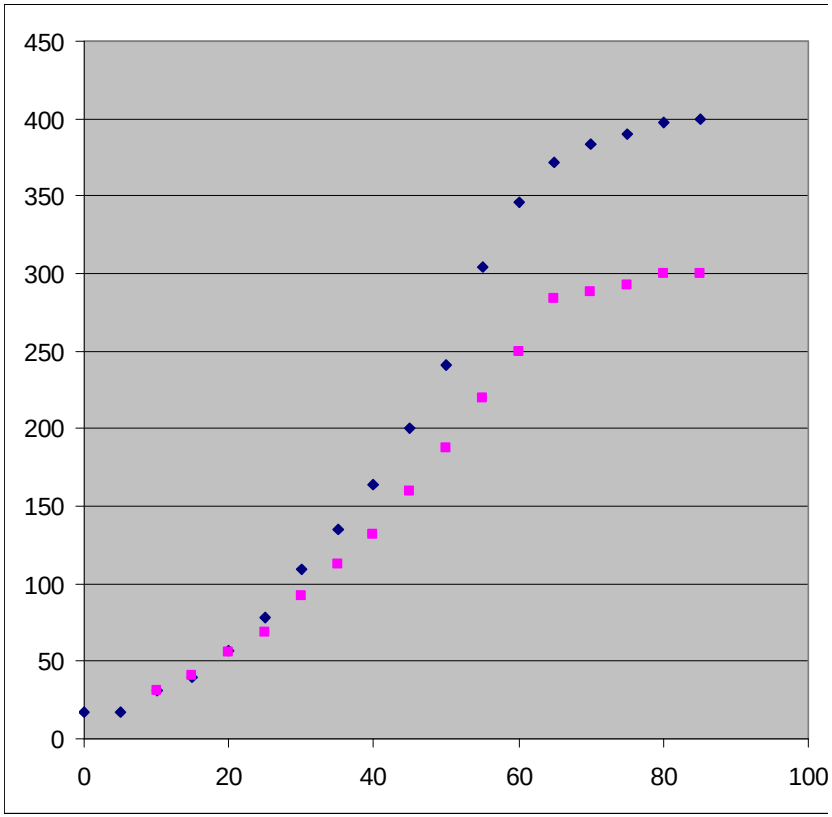
11x11 shutter



6x6 shutter



Non-linear region of laser



16x16 shutter

(Data from Jamie B)

- samplers with source
- samplers without source
- shapers with source
- shapers without source

- histogram of the number of hits at each timestamp integrated over a very large number of bunch trains (~360k), for thresholds down to 160.