Simulation results for Deep P Well Calice pixel – first submission -

Introduction

This document presents simulations results for the CMOS MAPS 0.18µm featuring DEEP P-well (INMAPS) for the CALICE ECAL detector. Results for the no INMAPS CMOS structure are also presented.

DC Simulation results

The layout and corresponding 3D models of the simulated structures are shown below:

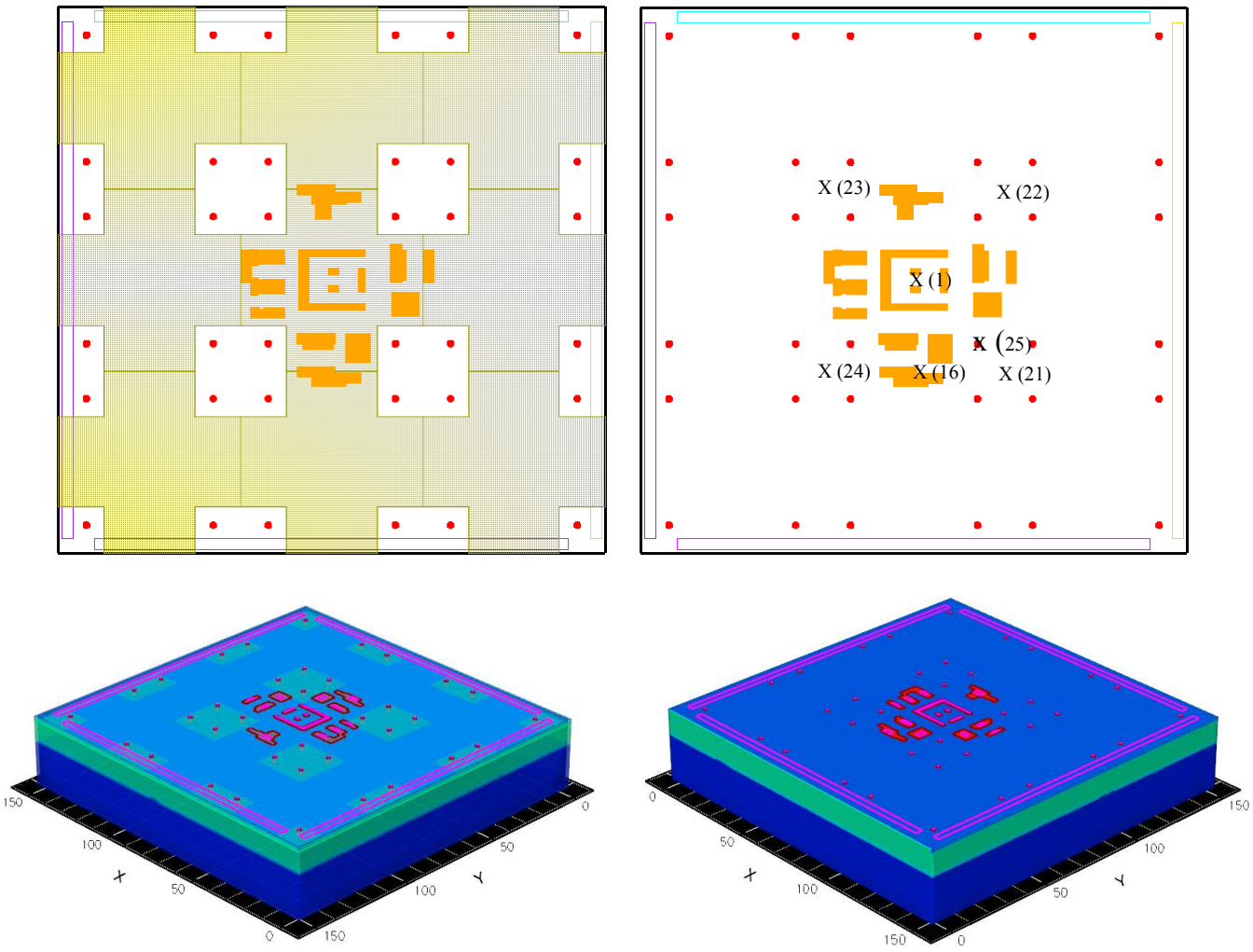


Figure1,2: Layout and 3D structure of the CALICE MAPS pixel. INMAPS process on the left, NO-INMAPS on the right. Hit locations(X) with their number are show superimposed onto pixel.

The simulated structures consist of an array of 3x3 pixels. The central pixel includes the NWells housing the readout electronics. The remaining pixels include only the diodes and not the NWells to speed up the simulation time. The 21 simulated hit points are shown superimposed onto figure 2.
Both structures are biased with voltages:
Diodes: 1.0V
Nwells: 1.8V

The leakage currents for each diodes of the central pixel for both structures are reported in the table below:

	D1	D2	D3	D4
NO INMAPS I_{lk} (fA)	0.97	0.98	0.97	0.98
INMAPS I_{lk} (fA)	1.12	1.12	1.13	1.14

The INMAPS structure shows a slightly higher leakage current compared to the NO INMAPS. This is expected, as a result of the highly doped (i.e. more conducting) Deep Pwell region near the collecting diodes in the INMAPS. In both cases the amount of shot noise added, at least for realistic integration time, is negligible.

The depletion width region under the collecting diodes for both structures can be determined from the extension of free-carriers region. From figure 3 it is deduced to be around 1.8 μm.

In the INMAPS the presence of Deep PWell around the NWells creates a potential barrier of around 140mV that helps confine the electrons inside the epitaxial region (figure 4). Along with the potential barrier created by the doping difference between substrate and epitaxial region, of around 200mV, the liberated charge following MIP ionization moves in a equipotential well of around 8um width.

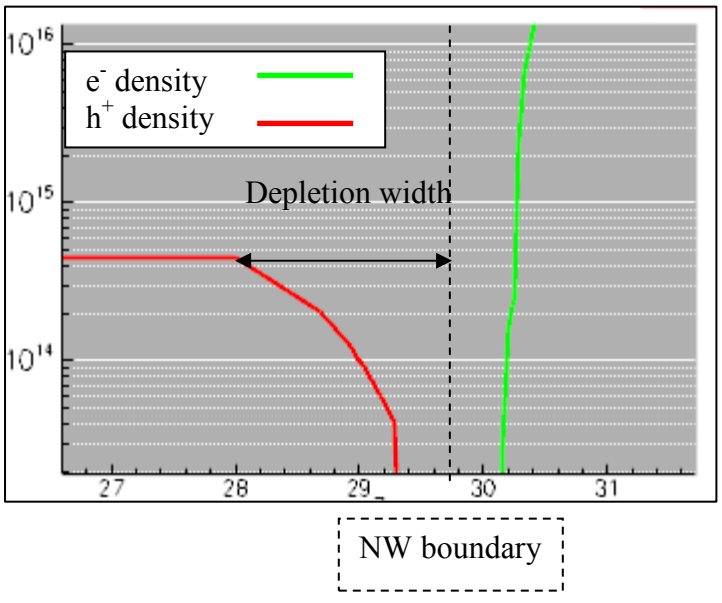


Figure 3. Depletion region under collecting diodes for Deep Pwell structure (sample along Z direction from D1 [X = 57.5, Y =57.5]).

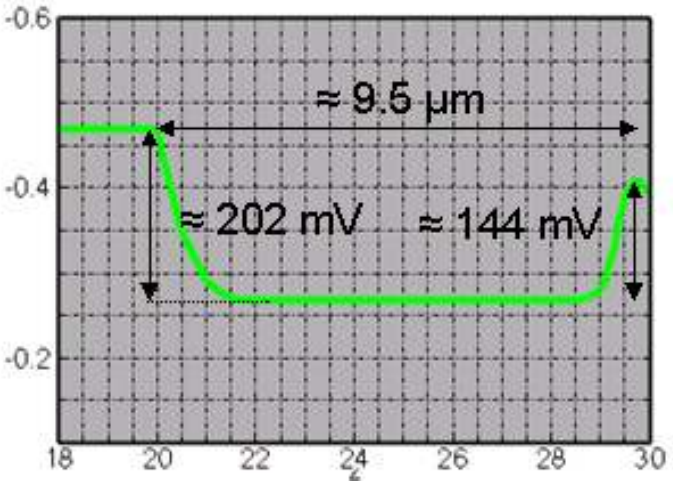


Figure 4. Potential barrier in the epitaxial region as a result of the Deep Pwell (sample along Z from [75,75]).

AC Simulation results INMAPS

The hits results from the 21 simulated points are transformed over the full array of 3x3 pixels to obtain a surface representation Q(x,y),{ x[0,150, y[0,150]} of the collected charge. The interpolation function is obtained by applying an SVD algorithm [1].

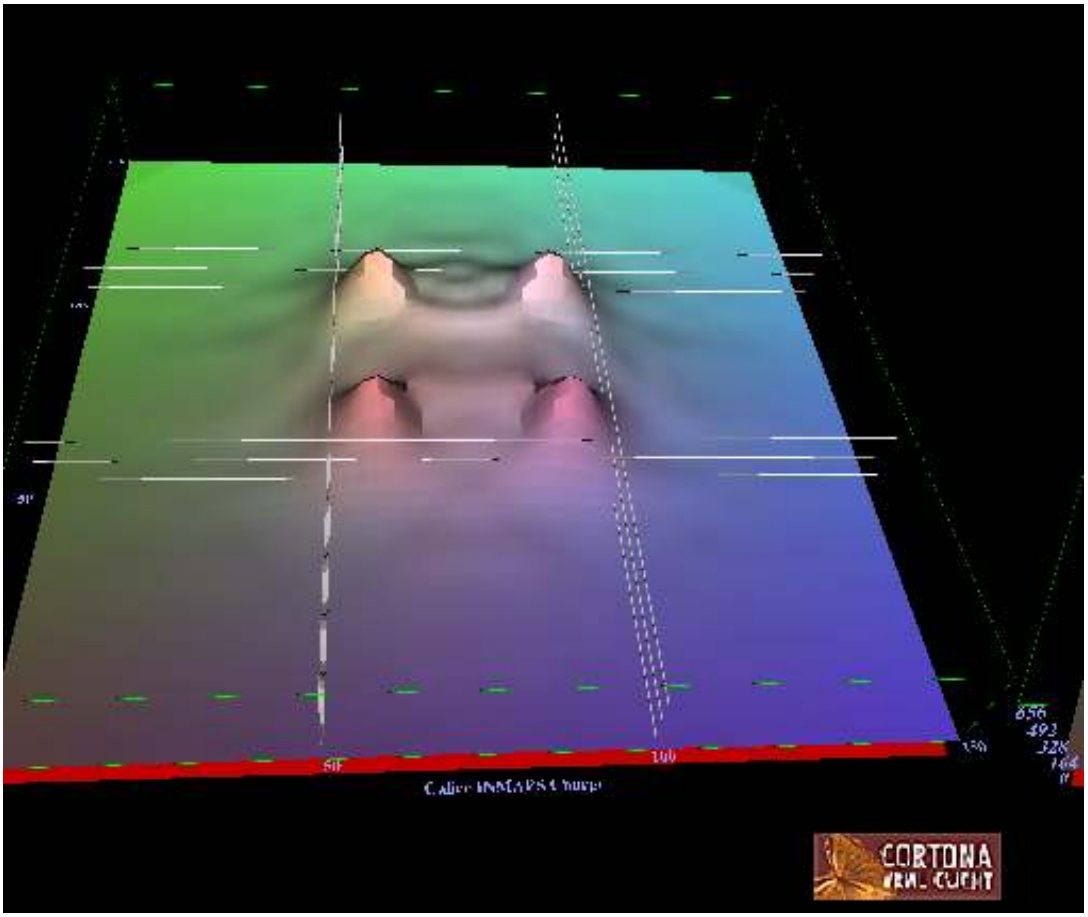


Figure 5. Charge collected (e^-) by INMAPS pixel vs. MIP orthogonal hit.

The average, maximum, minimum and standard deviation value of pixel's collected charge (in e^-) deduced from the 21 simulated hits points are reported in the table below:

Pixel collection	Charge (e^-)
<Q>	401
Q_{max}	656
Q_{min}[1]	261
Q_{stdev}	95

[1] minimum obtained from Hit 21, figure 2

N.B. For a lower symmetry pixel (i.e. with NWells asymmetrically placed in the pixel) it is expected that the full pixel's results deduced from the 21 hit points above may be inaccurate. This is particularly important when it comes to infer the minimum of the collected charge, as this dictates the lowest S/N achievable. Therefore, additional 'lowest charge' hit points (22, 23, 24 in figure 2) have been simulated and compared with the results from hit 21. Also the result for a straight hit on diode D2 (hit 25) is reported in the table below.

Hit	Q (e^-)	Hit 21 Q (e^-)	De	%De $(H_{xx}-H_{21})/H_{xx}$
22	267	261	6	2.2
23	266	261	5	1.8
24	263	261	2	0.7
25	788	261	527	66.8

The presence of the Deep PWell helps reduce the asymmetry of the pixel to a few percent. For worst case condition, the lowest charge hit (21) has been taken into account to build the surface of figure 5.

Assuming a nominal input referred noise of $25e^-_{rms}$ it follows that a minimum S/N ≥ 10 can be obtained over the whole pixel's surface, with an average S/N ≥ 16. The maximum S/N value for these set of simulations is obtained in case of hit 25, approximately S/N ≈ 31, the minimum for hit 21, S/N ≈ 10.4.

The contourplots of figure 6 show the area of the pixel interested for different values of charge threshold. Sample of Q(x,y) along direction (x,y) and (x,75) is shown in figure 7, against a plot of pixel's boundary.

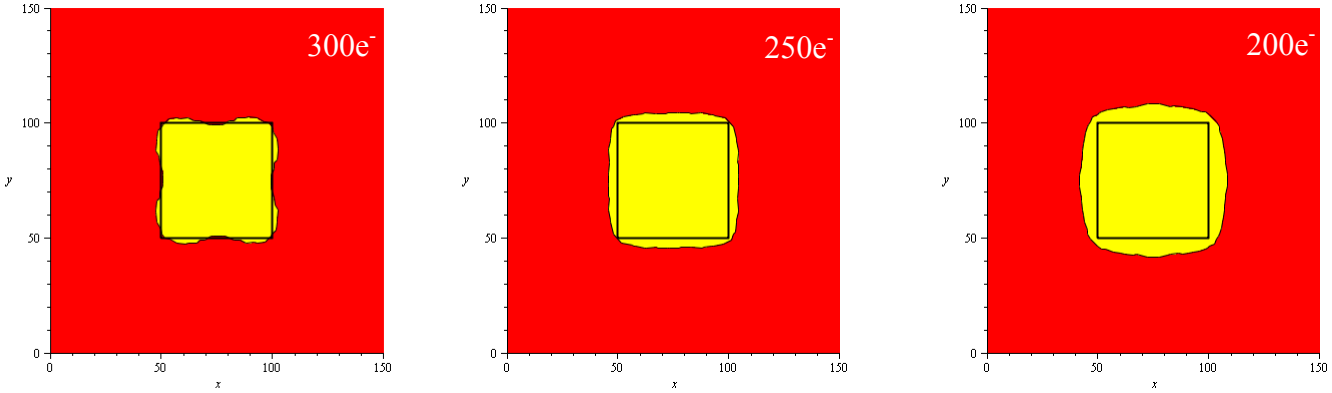


Figure 6. Contourplots for different Charge(e^-) thresholds

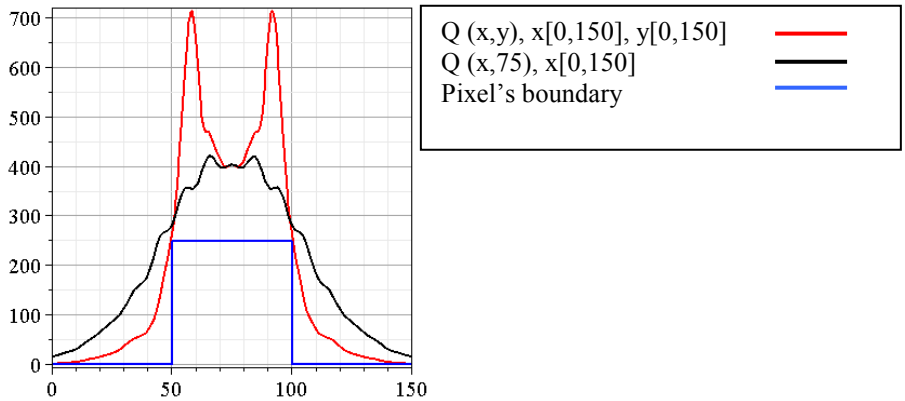


Figure 7. Sample of Q(x,y)

Using the same mapping approach used for charge collected, the charge collection time surface QT(x,y) is obtained:

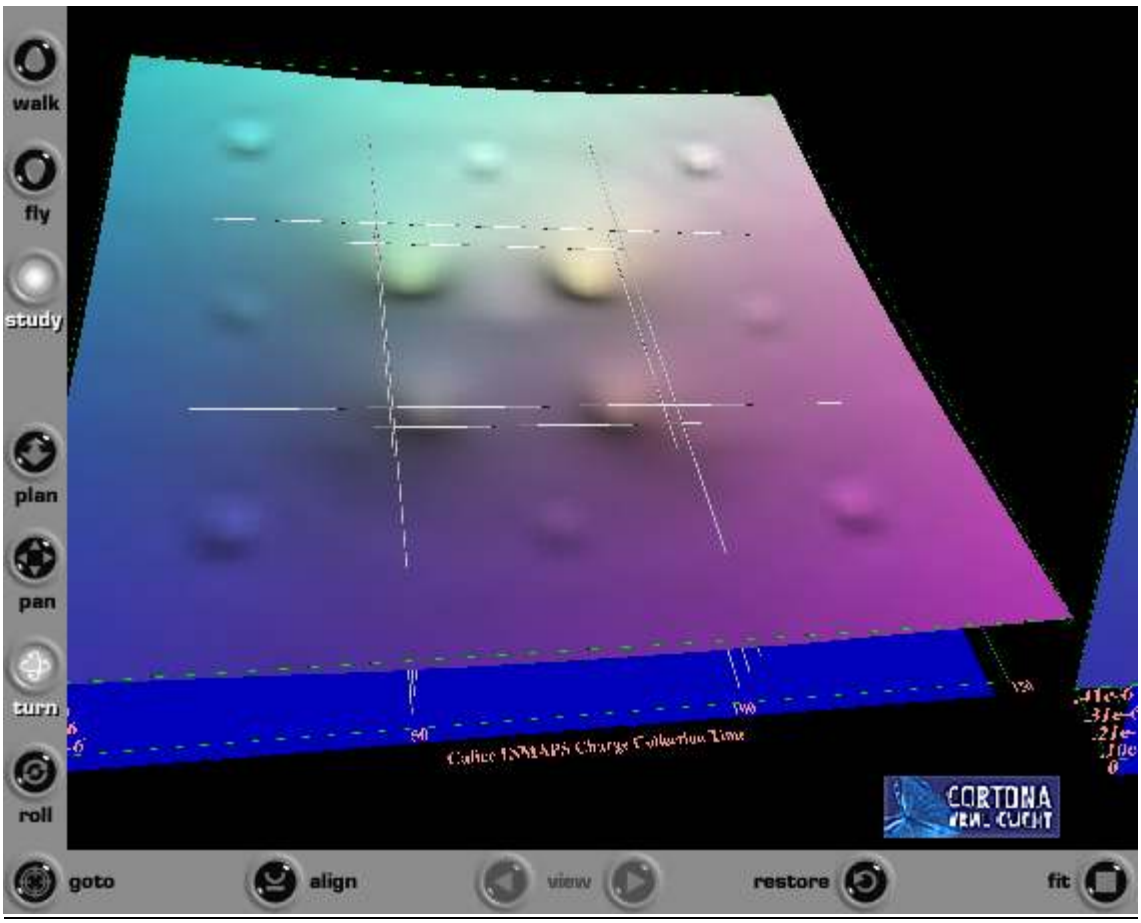


Figure 8. Charge collection time (s) by INMAPS pixel vs. MIP orthogonal hit.

The collection time is defined as the time it takes for the charge to reach 90% of its end of simulation time value (600ns in all cases).
The average, maximum, minimum and standard deviation value of pixel's time of charge collection deduced from the simulated hits points of figure 2 are reported in the table below:

PixelTime	Collection time (ns)
$<T_c>$	178.1
T_{cmax}	209.2
T_{cmin}	110.9
T_{cstedv}	0.28

AC simulation results NO INMAPS

The results for charge collected and charge collection time for the NO INMAPS process are reported below.

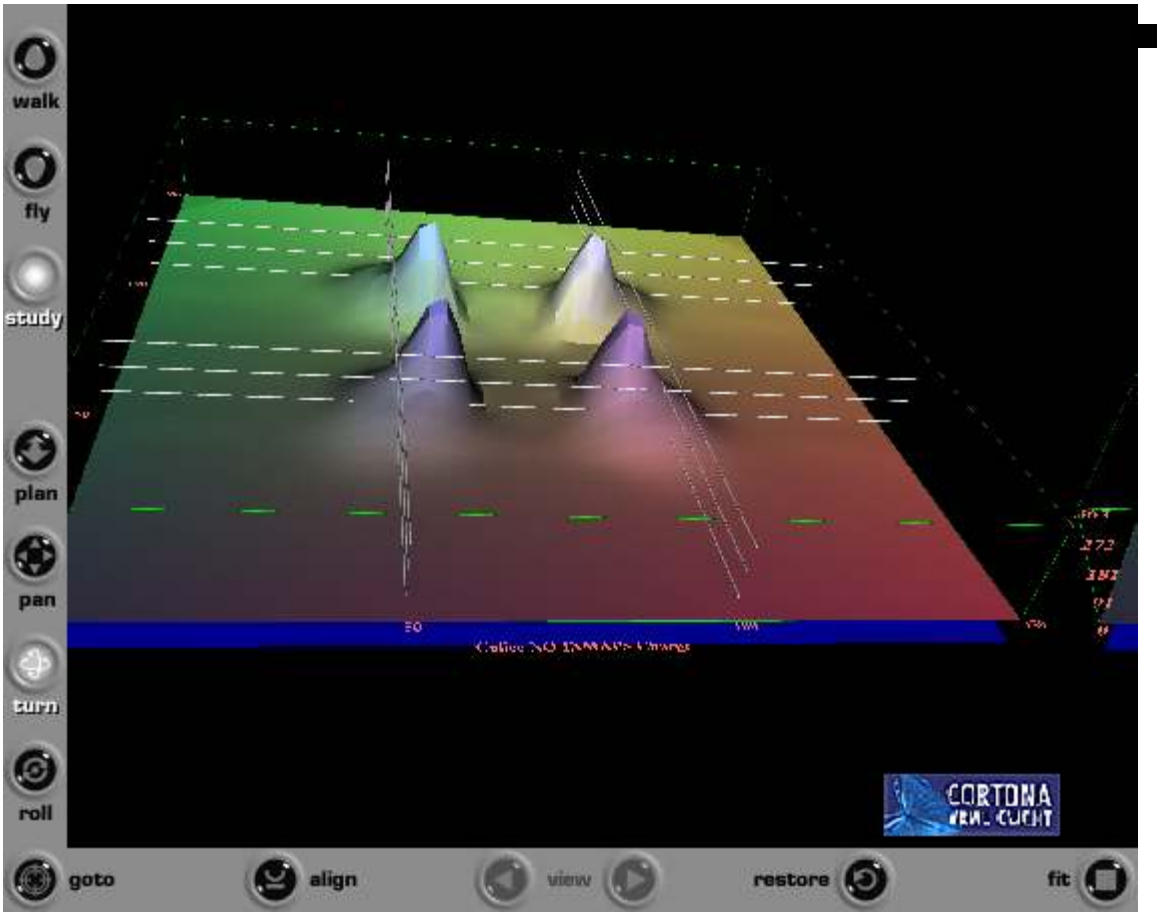


Figure 9 Charge collected (e^-) by NO INMAPS pixel vs. MIP orthogonal hit.

The average, maximum, minimum and standard deviation value of pixel's collected charge in e^- deduced from the simulated hits points of figure 2 are reported in the table below:

Pixel collection	Charge (e^-)
<Q>	87
Q_{max}	362
Q_{min}[1]	5
Q_{stdev}	107

[1] minimum located at Hit 1, figure 2

For the NO INMAPS process the asymmetry of the pixel is not compensated for because of the lack of the shielding Deep PWell. Therefore, there is a higher inaccuracy in the building of the Q(x,y) relying on the 21 hit points compared to the INMAPS solution.

Hit	Q (e^-)	Hit 21 Q (e^-)	De	%De
22	155	134	21	13.5
23	150	134	16	10.6
24	138	134	4	2.8
25	592	134	458	77.3

The standard solution (no INMAPS) shows a huge reduction of signal and a bigger difference between maximum and minimum compared to the INMAPS solution. A S/N ratio of 10 or more can be obtained only near the collecting diodes, as shown by the contourplots below:

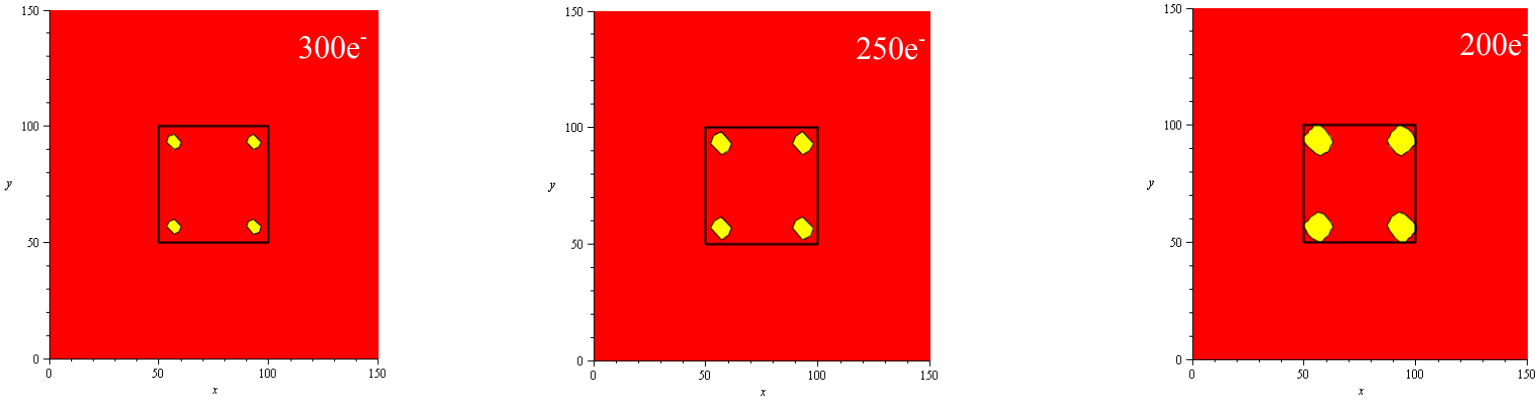


Figure 10. Contourplots for different Charge(e^-) thresholds

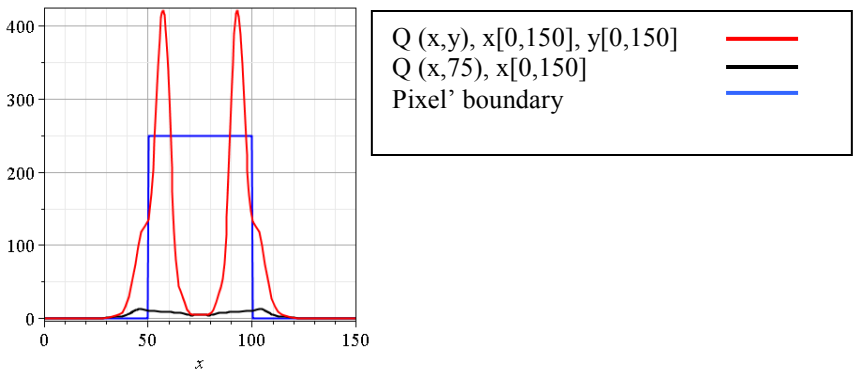


Figure 11 Sample of Q(x,y)

The charge collection time surface for the NO INMAPS solution is shown below:

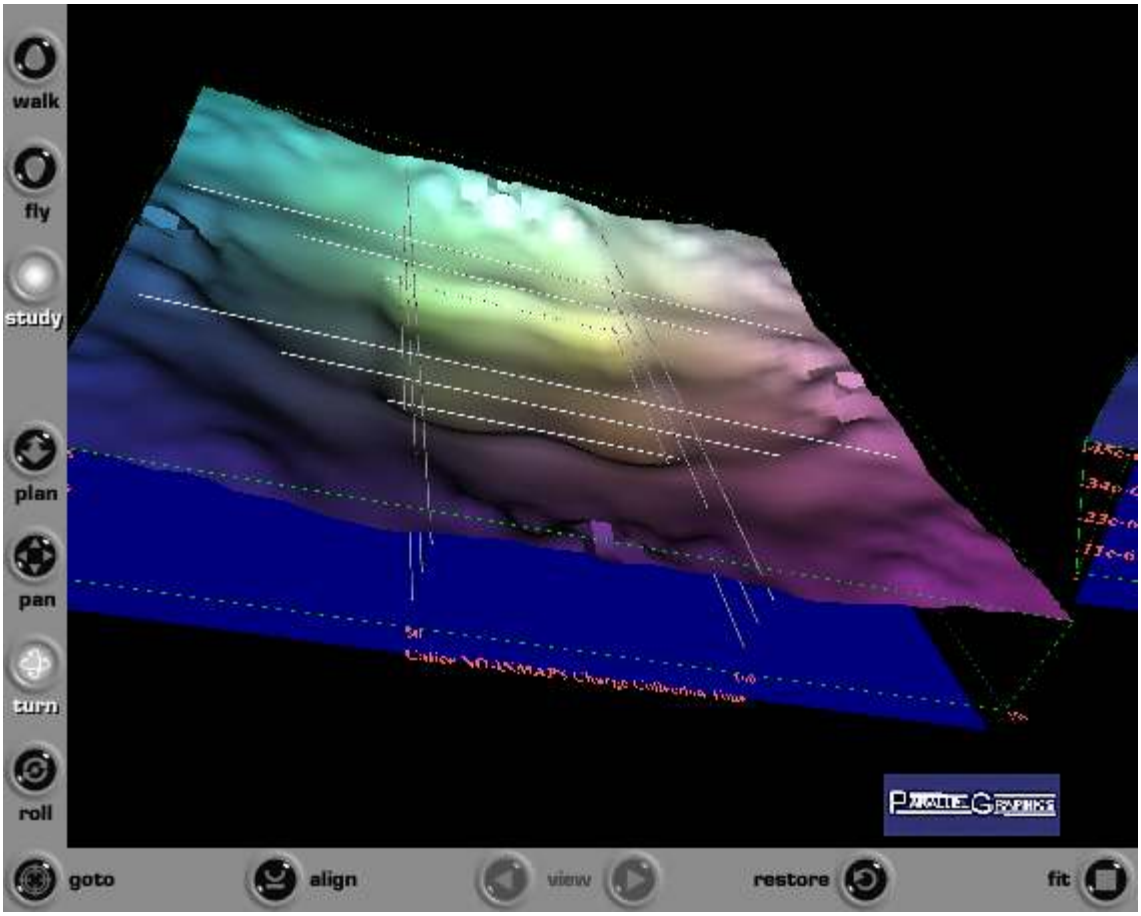


Figure 12. Charge collection time (s) by NO INMAPS pixel vs MIP orthogonal hit.

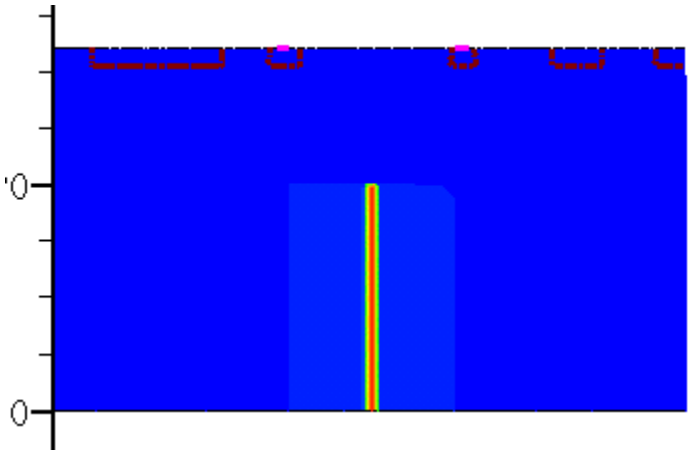
For the NO INMAPS process, the average, maximum, minimum and standard deviation value of pixel's time of charge collection deduced from the simulated hits points of figure 2 are reported in the table below:

PixelTime	Collection time (ns)
$<T_c>$	47.1
T_{cmax}	96.3
T_{cmin}	16.7
T_{cstedv}	18.8

Compared to the INMAPS process, there is faster charge collection because of the reduced efficiency (i.e. only the charge generated near the collecting diodes is collected).

Substrate contribution

The average of the total charge collected by the NWells or by the P contacts for hits 1-21 is 1242e^-. This would seem to suggest that approximately 3.5 μm max of the substrate are contributing to the total charge collected.



To study this, a simulation for hit 1 where the MIP frees charge only within the substrate has been carried out for the INMAPS process. The results are shown in the table below.

Q(e^-)	D1-D5	QDTOT	QNWTOT	QPW
	91	186	67	-252

Where:
D1-D5 is the total charge collected by the diodes of the central pixel;
QDTOT is the total charge collected by the 4 x 9 = 36 diodes of the 3 x3 array;
QNWTOT is the charge collected by the NWells;
QPW is the charge collected by the PWell contacts.

The total collected charge amounts to 252e^-, corresponding to approximately an equivalent 3.1 μm of substrate effective in charge creation, after a 12um deep epitaxial layer. This compares well with the typical diffusion length for Si at the substrate doping level (i.e. around 3.1um of diffusion length for N_A = 4.0 E 18, [2]).

Conclusions

According to simulations, the INMAPS process shows remarkable improvement in charge collection efficiency compared to a standard, NO-INMAPS solution.
The collection time is in the order of 200ns for the INMAPS process, and approximately half this value for the NO-INMAPS, but this is due to the much smaller efficiency in charge collection in the latter case.

The achievable S/N for the INMAPS is expected to be around 10 for the whole pixel's surface, despite the complexity of the readout implemented within the pixel.

The substrate contribution to charge collected has been evaluated to be around 3.1µm maximum. This seems to suggest that even a deep back thinning should guarantee unaffected charge collection performances. Also, a thinner epitaxial layer (i.e. < 12µm) could guarantee good performances if the generated charge could somehow be kept within pixel's boundaries (i.e. by decreasing charge spread).

Appendix : numerical data simulations

CALICE INMAPS sims results hit 1-21

CALICE INMAPS sims results hit 1-SUBS ONLY

CALICE NO-INMAPS sims results hit 1-21

References:

[1] H. C. Andrews and C. Patterson, Outer product expansions and their uses in digital image processing, *American Mathematical Monthly*, 82:1 (1975) 1–13.

[2] J.G.Fossum et al. "Carrier recombination and lifetime in highly doped Silicon", Solid-State Electronics, vol. 26, no. 6,pp.569-76, 1983