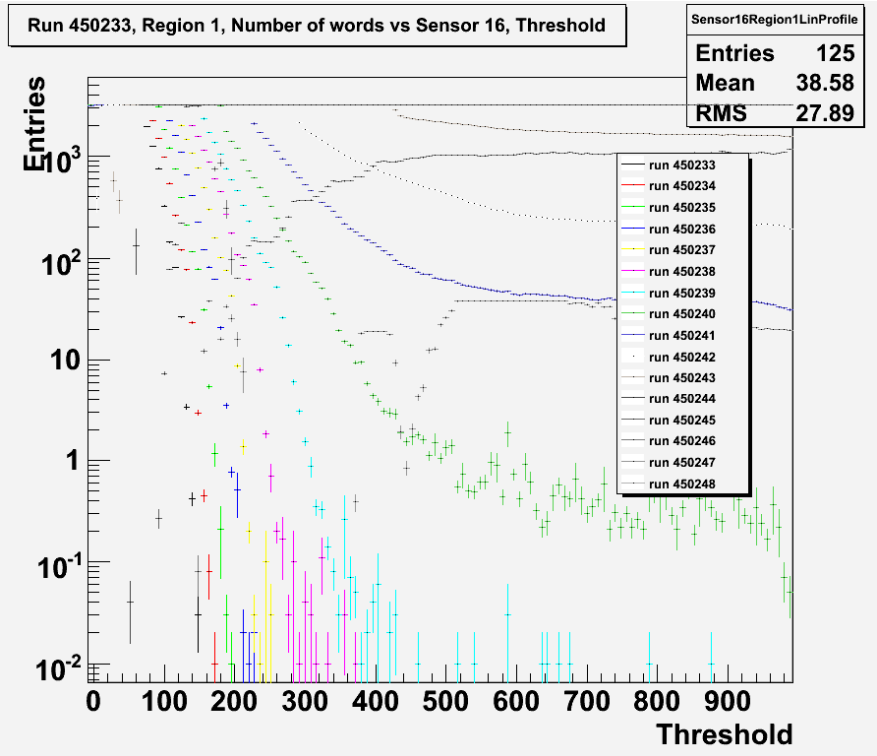
Recent progress

Jamie C

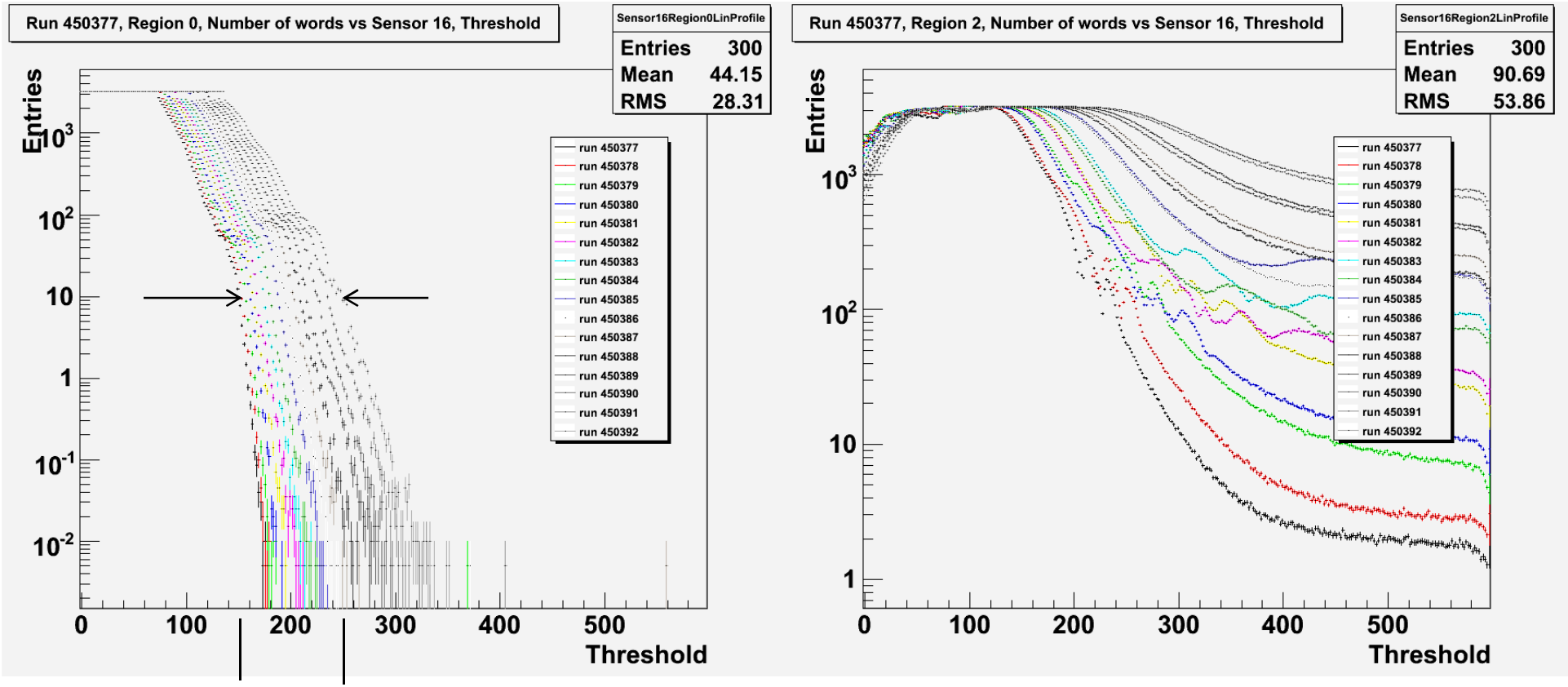
31st March 08

TRIMS

- Were looking odd…….
- Step size too large!
- Tested some new values…
  - R73=180k
  - R75=180k
- Need to check this covers pixel spread! (TBD)



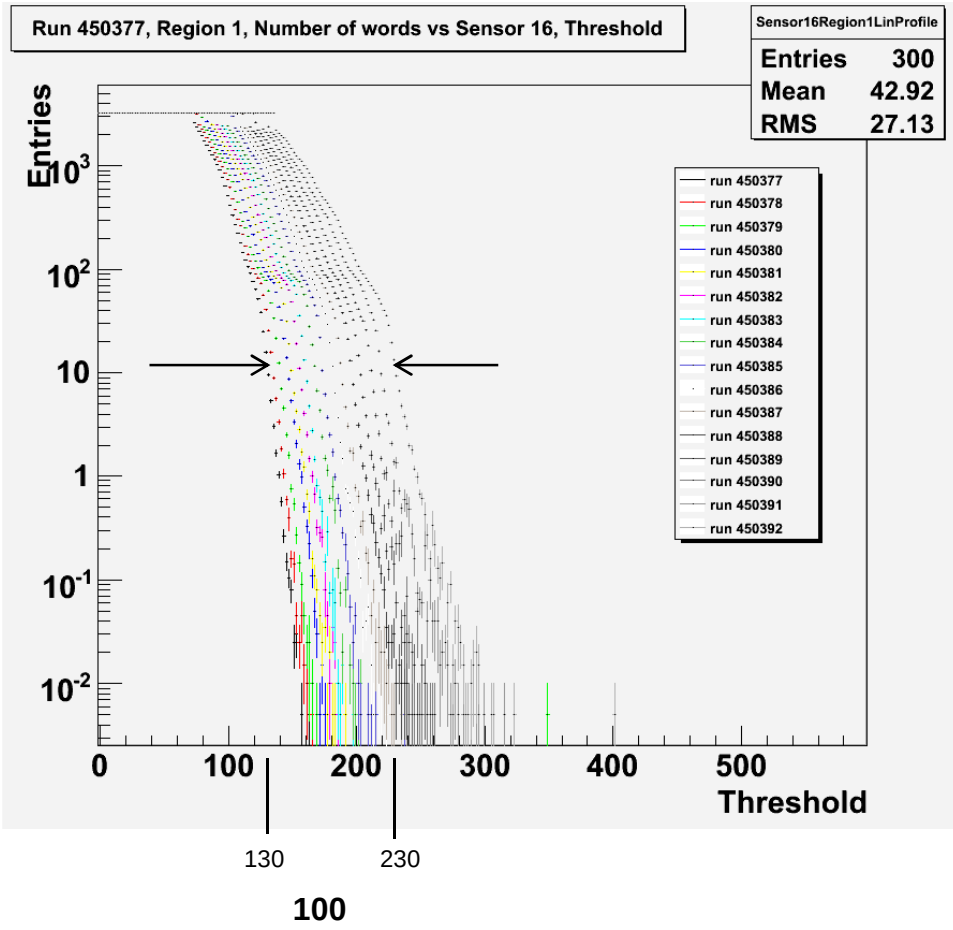
TRIMS 0à 15 $DAC_{(8,11)}$=3000

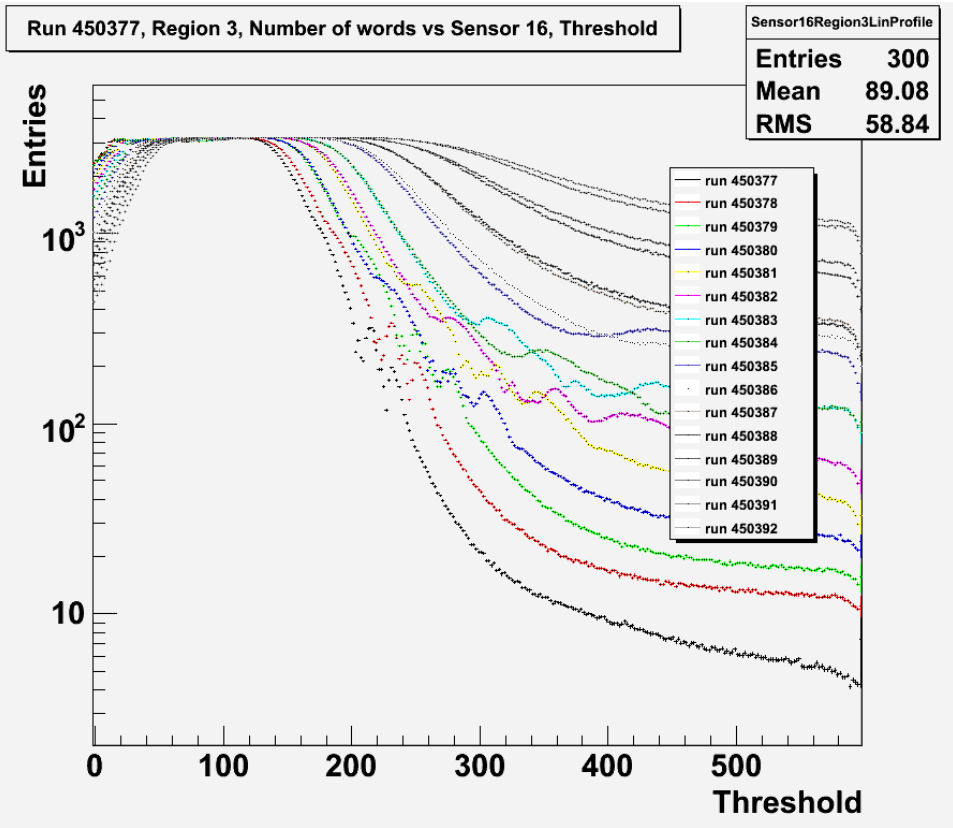


150 252

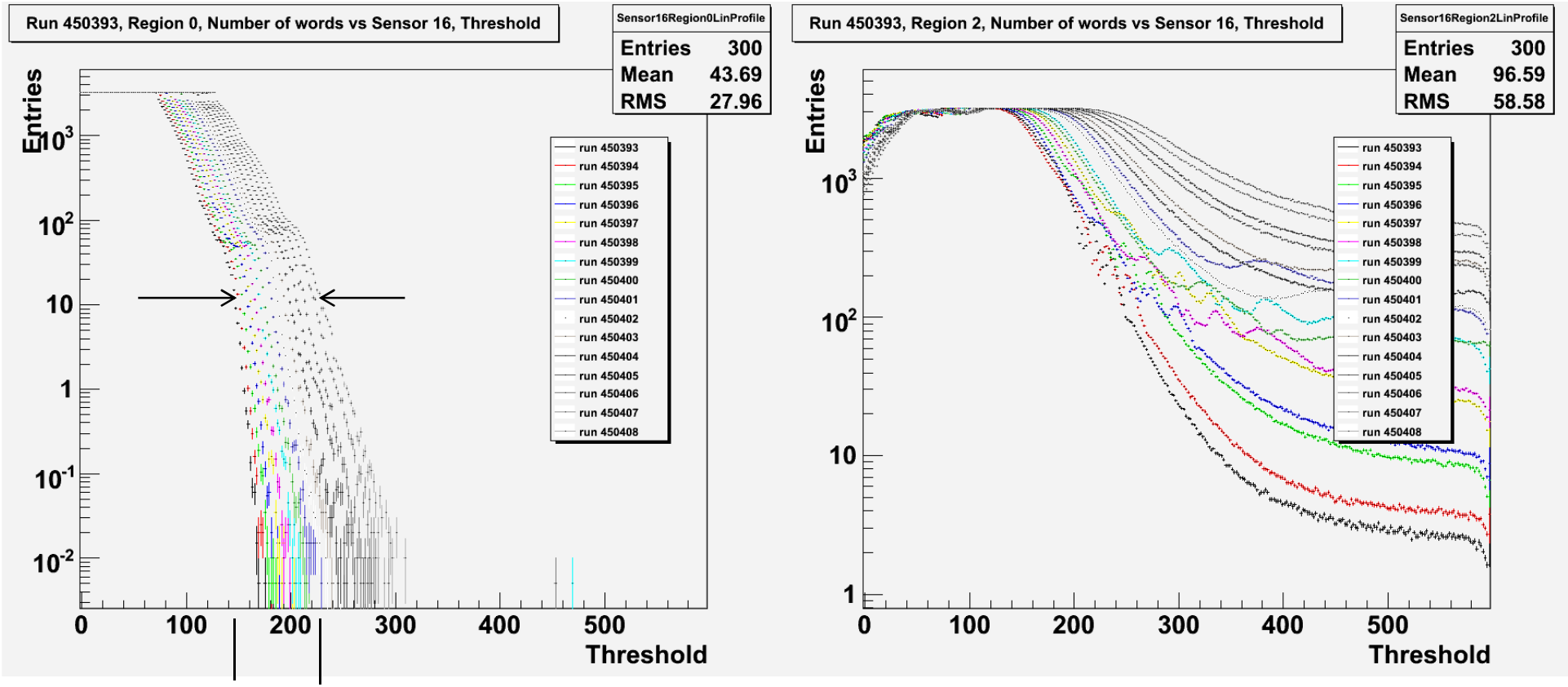
102

TRIMS 0à 15 $DAC_{(8,11)}$=3000





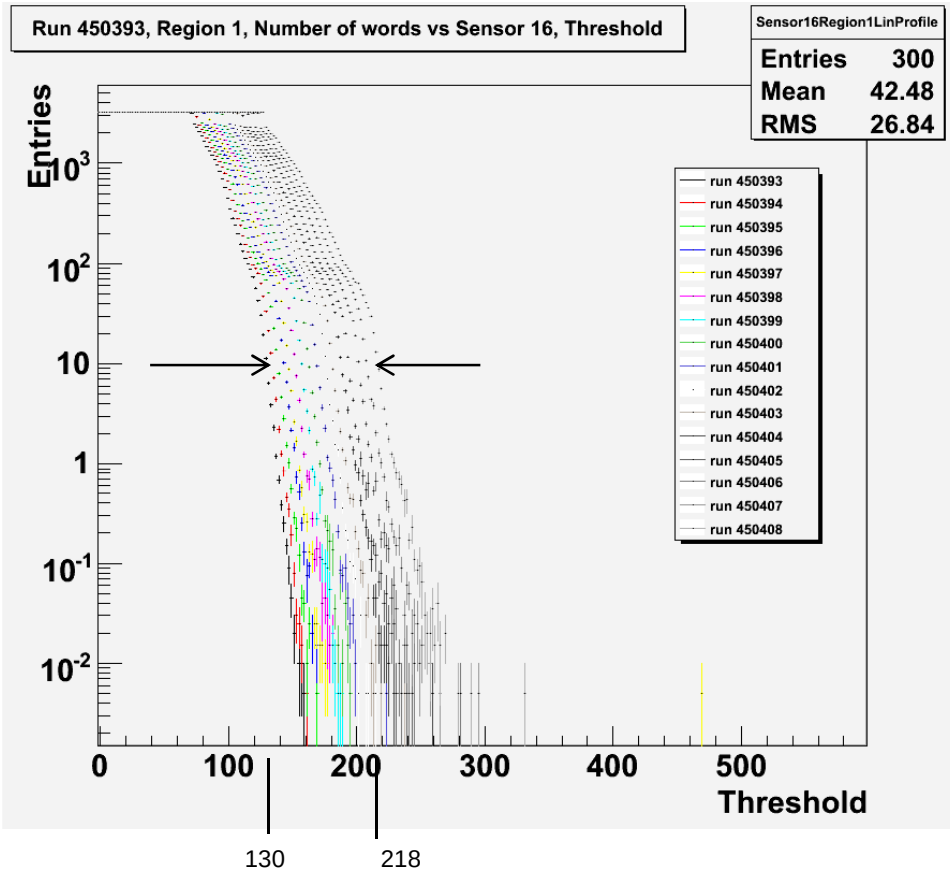
TRIMS 0à 15 $DAC_{(8,11)}$=1000

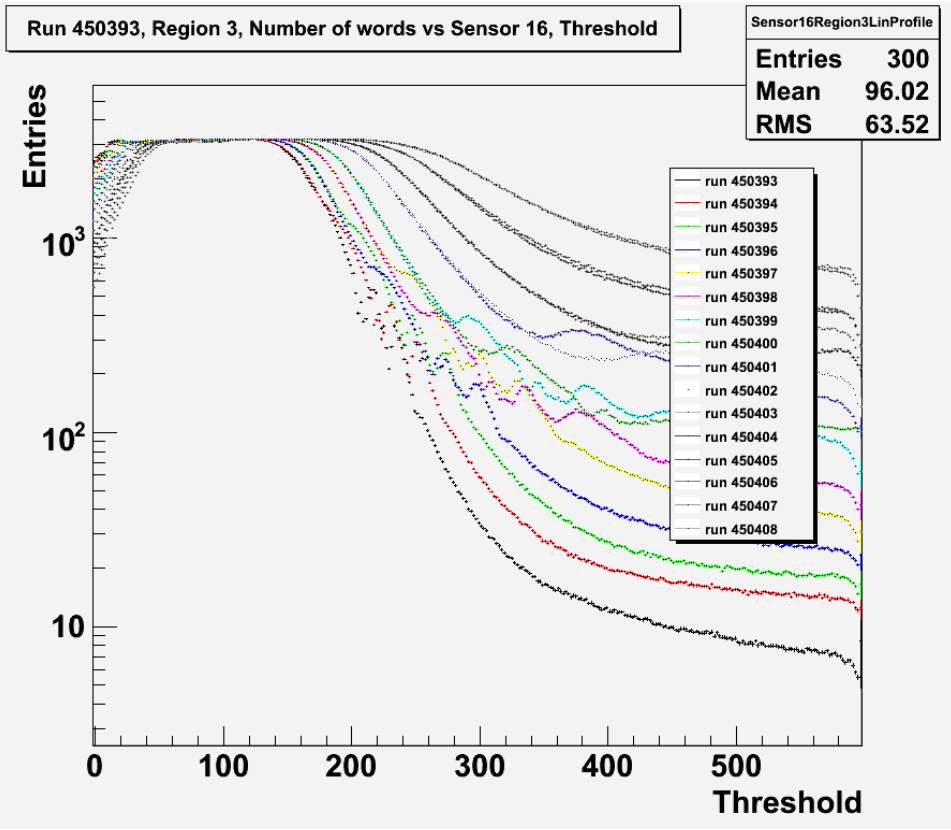


142 228

86

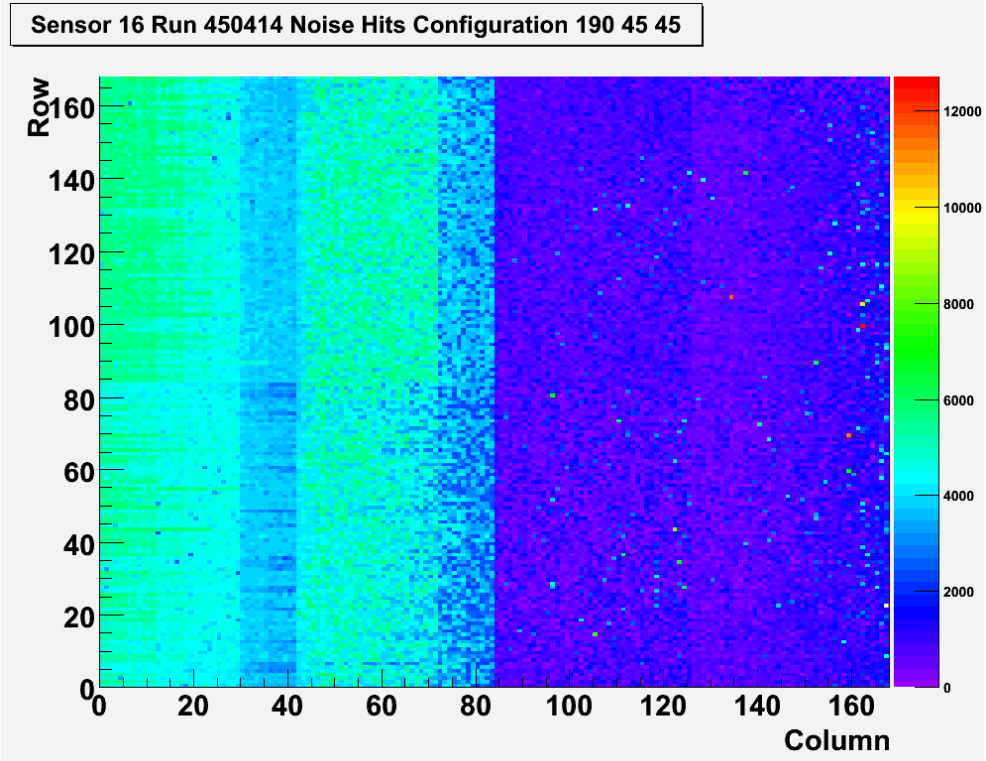
TRIMS 0à 15 $DAC_{(8,11)}$=1000





Cold Columns?

- Marcel reported uneven distribution of noise hits in different regions of the shapers à



- <u>Explanation</u>:
  - Effect seen only at very low threshold levels
  - Sensor is therefore seeing hits in ~all pixels (~override mode)
  - Therefore memories fill sequentially
  - Not enough memory to store three full rows of hits, hence “cold columns”
  - Hits are stored from banks:

1	2	3	4	5	6	7	1	2	3	4	5	6	7	1	2	3	4	5

Yield/Bonding/PCBs

- See spreadsheet…
  - boards-yeildtracker.xls
- Missing ORE signals is a common failure of W10 parts
  - For further investigation…
- Stock (12u+DPW)

  W8 9
  W10 >9

  W# 60 (sealed)

Outstanding issues

- Per-pixel scan data analysis
  - What spread do we see? (per pixel type)
  - What range of trims are required?
- Would like to run threshold scans while holding pixels in reset?
  - Matt says firmware will support this
  - Paul needs to confirm if software will override settings?
- Check for BANK=0 in raw data
  - Low priority as “cold-columns” now explained
  - But should still be run on all sensors to check data integrity, otherwise would be losing hit data with no knowledge
- Sensor #9 at IC
  - Mods done?
  - Threshold scan ok?
- Marcel will show
  - Row address corruption & per-row masking scans
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