APACHE - Advanced Pixel Architectures at upComing HEP Experiments

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This proposal describes the APACHE proposal of developing highly performant advanced pixel structures with analog readout for future HEP experiments. Their main application would be for precision tracking in dense environments, providing the ultimate resolution for pattern recognition. The technology developed herein will have wide applicability to other projects using silicon pixels sensors. It also builds on significant UK expertise in designing advanced pixels.

1. Introduction

The capability to precisely "track" particles passing through a detector volume has been a key to the success of modern high energy physics. This is usually done by using a set of sensitive layers that record the hits caused by the particle passing through.

The reconstruction of the particle trajectory is usually done in two steps, pattern recognition and track fitting. The pattern recognition provides a set of hits that are likely to belong to a given particle passing through. The track fitter then fits all these to a trajectory, returning a probability of this being a valid hypothesis. The ideal tracking sensor would then have a very low material budget and a very precise point resolution.

Given their material properties silicon sensors can provide an extremely precise hit measurement, which makes them almost ideal for tracking. However, from the material budget point of view, silicon of course is less favorable than e.g. a gaseous detector, and thus is limited in the number of possible layers in a detector. The first silicon-based tracking detectors have been designed as silicon micro-strip sensors, typically only providing rφ coordinates of the hits. Later developments then led to the usage of finely pitched silicon pixel sensors, like the CCD pixels used in the SLD Vertex Detector at the SLC[1]. For the ATLAS and CMS experiments at the LHC[2], the 3 layered pixel detectors closest to the interaction region are the workhorse for the pattern recognition, as they provide three precise hit points with a resolution of (10 micron check numbers). The silicon pixel sensors at the LHC are readout using a readout chip which is bump-bonded on the silicon pixel sensor.

Given this design, these pixel layers were very difficult and expensive to manufacture, primarily due to the bump-bonding. Also concerning the material budget and their power consumption, the usage outside of the three innermost layers of the tracking proved to be prohibitive. For future experiments, which will require unrivaled tracking performance, silicon pixel technology offers a path to provide a solution. This would enable silicon pixel arrays of potentially several 100 m^2 with 10^{10} individual pixels.

[1] Stanford Linear Collider
[2] Large Hadron Collider

To evolve silicon pixel sensors as outlined above, we must address and optimize the following factors:

- Granularity/ Resolution
- Intelligence
- Power Consumption
- Readout speed
- Radiation Tolerance
- Cost

In terms of upcoming high energy physics experiments at currently proposed colliders like the SLHC[1], the linear collider, a Super-B factory and muon collider, the requirements have been summarized in Table 1:

	SLHC	Linear Collider	Super-B factory	Muon Collider
Granularity	moderate	very small	small	very small
Radiation Tolerance	high	low	low	medium
Power Consumption	very high	high	small	high
Readout Speed	fast	slow	medium	slow
req. intelligence	clustering triggering	clustering	none	clustering
Detector Size	big	big	small	big

Table 1 Challenges for upcoming HEP experiments

The UK has already considerable expertise in designing silicon pixels for tracking applications, using CCD[2], ISIS[3] and MAPS[4] based pixel designs. In this proposal we intend to build on this expertise in order to develop pixel solutions addressing these problems.

Silicon pixel sensors are the technology of choice considering power requirements, material budget and resolution. They allow a minimization of tracking layers in the material, allow to implement track-triggering and they have applications in tracking, vertexing and calorimetry.

2. The project

The main requirement of a tracking pixel is having high granularity and analog readout. We are planning on using pixel sizes between 50x50 to 75x75 micron as a target size for this development. In order to reduce power, ease construction and keep the material budget low, we intend to integrate some readout electronics within the pixel, creating “intelligent” pixel architectures. We envisage usage of a 4 or 5 bit ADC to give sufficient dynamic range and provide good signal resolution. We also envisage more intelligence on the module level to further reduce the data rate by applying on-module clustering of the hits. This has the potential of drastically decreasing the necessary cabling infrastructure and therefore the material budget of a tracker. Also it will allow us to explore new ideas like extremely fast track triggers based on silicon pixel as are foreseen for the SLHC.

[1] Super LHC
[2] Charge Coupled Devices
[3] In-Situ Image Storage
[4] Monolithic Active Pixel Sensor

In terms of speed, future accelerators may well have an even shorter time between two collisions than at the LHC (25 ns). Hence being able to collect the signal charge within a few ns is essential. The high granularity of a pixel detector will keep the occupancy below 1%, that the actual data readout can be slower and take advantage of on-pixel buffering as well. It is however clear that there will be always a trade-off between speed and power consumption, but in this proposal we intend to push the envelope of today's technology.

Depending on the application and the type of the accelerator, radiation is also an issue and a certain level of radiation hardness will be required. For proton-proton machines the particle flux is dominated mainly by protons and pions, the remnants of the collisions. For lepton colliders, the flux is dominated by highly energetic photons and electrons from beam–beam interactions, which lead to a very different radiation field. This will require irradiation with both kinds of particles to get a comprehensive understanding. All designs will go through extensive testing of radiation hardness and the latest design guidelines for radiation hardness will be included.

The cost of pixel systems assembled to date was dominated by the required specialized processes used and the price of interconnects for the pixel sensor and the readout chip. The method used was bump-bonding which was both expensive and error-prone, leading to a lower yield in module production. The usage of MAPS sensors would eliminate the need of bump-bonding the readout chip, as all readout electronics has been integrated. In order to be cost-effective, the usage of industry standard processes based on CMOS will be the goal, as this would allow manufacturing large areas (several 100 m^2) with high yield and at low cost.

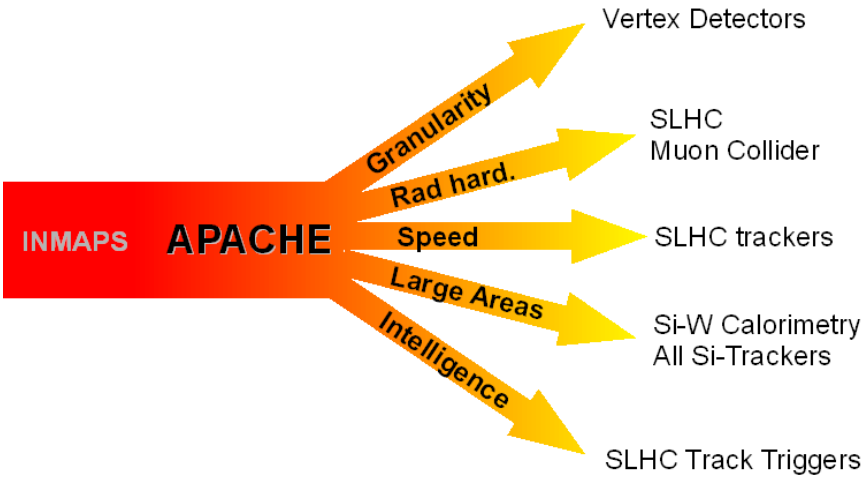

Figure 1: The roadmap for silicon pixel detectors based on the APACHE design

The APACHE pixel will do the required R&D to address the open issues for quite general tracking pixels and will be the switchyard from which different optimizations for specific applications can emerge. E.g. for vertexing it is clear, that the granularity will be increased by a large amount, but the area required will be quite small (1 m^2), which is one extreme case for the optimization. Another one will be the need for large areas as is foreseen for Si-W calorimeters for particle flow reconstruction.

We plan for a duration of 3 years for the entire project.

2.1 Proposed technology

Silicon technology offers a variety of choices of technologies for implementing pixel architectures, but in this proposal we will focus on the most promising technology for the pixel realization, both in performance as in cost and availability

2.1.1 Monolithic Active Pixel Sensors

Monolithic Active Pixel Sensors (MAPS) have left the stage of prototypes and are routinely employed in science and in industry. A MAPS sensor is based on industry-standard CMOS technology integrates the active area in which the charge is generated with the readout electronics. The charge is then collected by using one or several n-well diodes. Only recently there were limitations in the design of MAPS, as only p-well components could be used, since n-well components in the electronics would parasitically collect charge as well, severely affecting the available signal This was recently overcome by an innovative process pioneered in the UK by a Rutherford Appleton Laboratory, / Imperial / Birmingham consortium funded by an STFC grant (CALICE WP3) and a CMOS foundry as industrial partner.

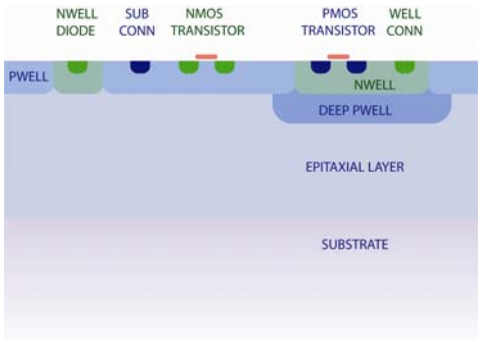

Figure 2: Cross section of a MAPS using deep p-well. It clearly shows the substrate (bottom), the epitaxial later with the charge collection and the electronics on top. A n-well used by a PMOS transistor is then isolated by a p-well implant below it, hence the name deep p-well.

The embedding of a deep-p implant below the electronics prevents this undesired behavior and allows almost infinite possibilities of embedded readout electronics. This innovative process has been already shown on several international conferences and it has received a lot of attention.

However all pixel designs based on MAPS technology have two fundamental challenges to overcome. As the signal charge generated in the about 15 micron thick active area – the so-called epitaxial layer- is very small (1500 electrons maximum). It therefore requires extremely low noise electronics and high gain amplifiers. Both are challenging and lead also to an increase in power consumption. The charge collection in a MAPS pixel is done by diffusion only, since one can't deplete the epitaxial layer sufficiently to collect the generated charge by drift as it is done by e.g. the LHC hybrid pixels. This leads to charge collection time of about 150 ns.

To address these issues, we propose to use high-resistivity silicon as material for the epitaxial layer instead of the usual low-resistivity material. By applying a bias voltage, it could be then completely depleted. This would immediately speed up the charge collection to less than 15 ns since the charge is collected by drift. It also leads to significantly larger amounts of generated charge of about 3000 electrons, as the active area will be made much larger due use of the high resistivity silicon. This will ease the requirements on the integrated readout electronics by a large amount.

Combining the deep-p-well process and a high resistivity epitaxial layer would be likely be the ultimate MAPS sensor combining high integration and low power consumption. Furthermore we will explore this technology further with our industrial partners in the CMOS industry.

3. Individual Work packages

The project can be split in several individual work packages, which are described in detail below. Altogether the APACHE project consists of six work packages including one central managing package to administer common infrastructure and the travel budget (see **Figure 3**)

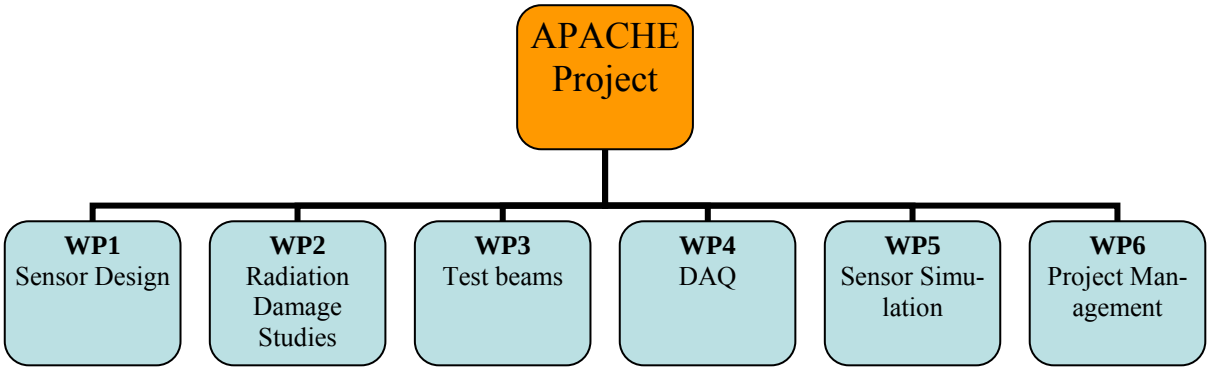

Figure 3: APACHE Work packages

3.1 WP1: Sensor Design

In this the core work package of the project, we intend to design and submit three iterations of chips, call APACHE-Pre, APACHE-I and APACHE-II.

Apache-Pre will be a technology demonstrator to test the new high resistivity silicon process at the foundry. It will be significantly simpler and will illustrate basic functionality only. This is definitely necessary before going to larger structures and will help characterizing the process in great detail.

APACHE I will consist of a 1x1 cm pixel array with 150x150 pixels and will include in-pixel intelligence and a built-in ADC. We plan to integrate a four or five bit ADC into the pixel, presumably realized as flash-ADC to avoid running clock signals over the entire pixel. This first iteration will serve to thoroughly test the integrated electronics and to quantify the ADC performance. The data bus will be all parallel in order to ease testing. A preliminary layout of the pixel electronics is shown in **Figure 4**.

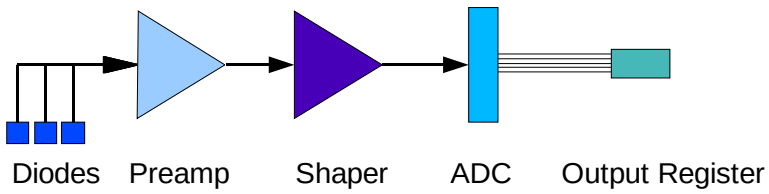

Figure 4: The planned pixel architecture

The diodes collect the charge and feed into a pre-amp before the shaper forms the signal into a suitable form for the 4 or 5-bit ADC. The conversion value is then stored in the output register, where it will be readout by on chip-logic.

APACHE II will be a 2x2 cm area with 300x300 pixels which will be a final design ready for a test beam. It will be bump-bondable and will be mounted on a stave structure to evaluate system performance and to test the higher level intelligence features like on-stave clustering. The stave will consist out of 6 APACHE-II sensors with 540000 pixels altogether, a sketch is shown in **Figure 5**. The output of the chip will

be driven by a serial bus to lower the bond pad count and will be feed into an FPGA for the on-stave sparsification. We intend the usage of an FPGA instead of an ASIC to lower cost and to keep larger flexibility in developing the sparsification. Another project could be to design the in-stave intelligence for the use in an extremely fast track trigger for SLHC. For the pixel design, we envisage building on the expertise acquired with TPAC1 design for CALICE, the StarTracker and the OPIC.

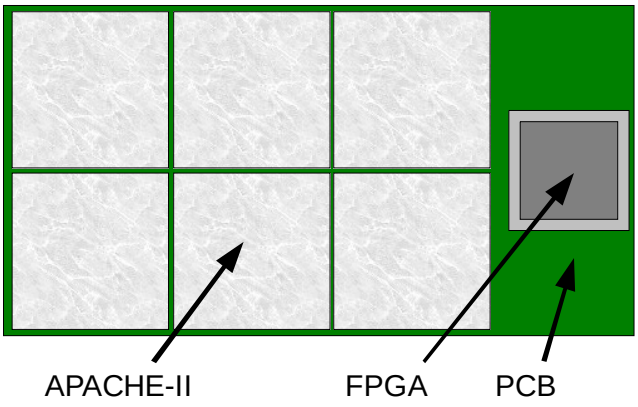

Figure 5: The APACHE-II Stave with 6 APACHE II and an FPGA

In terms of minimizing the risk involved in using a novel process using high-resistivity epi wafers, we can always fallback to standard CMOS wafers using deep-p and deep n-wells without endangering the entire project. The deep p-well process is already well established and has been used for several chip submissions. In this case however, we are certainly limited in the speed of the charge collection and the signal size could however still complete all other aspects of the project.

This work package does also include the initial testing of the chip using radioactive sources, laser beam and cosmic rays.

3.1.1 Resources

3.1.2 Deliverables

- A technology demonstrator proofing High-resistivity MAPS technology
- APACHE I 1x1 cm structure
- APACHE II 2x2 cm structure
- Demonstrate stitching

3.2 WP2: Radiation Damage studies

In order to assess the radiation hardness of the process, all three generations will be irradiated with protons, neutrons and x-rays. Radiation hardness is mainly an issue for the SLHC, were the immense levels of radiation severely limit the life time of any silicon detector. But also future lepton colliders have quite a high flux of particles (mainly photons) in the forward regions. Therefore the radiation hardness has to be taken into account for lepton machines, although the levels are still orders of magnitudes lower than for hadron machines. We presume that the irradiation test will be done at DESY and Fermilab.

3.2.1 Resources

	Year 1	Year 2	Year 3
Oxford RA (FTE)	1.0	1.0	1.0
Oxford Rolling Grant (FTE)	0.4	0.4	0.4
Total (FTE)	1.4	1.4	1.4

Table 2 WP2 Resources

3.2.2 Deliverables

- Irradiation of all three sensor generations using x-rays, protons and neutrons

3.3 WP3: Test beam

In order to test the performance of the APACHE-II we intend to make an extensive beam test with at least four modules. This will allows us to a real-world test of this architecture and will e.g. enable us to study the tracking efficiency using real particle tracks. Also the rates achievable in a test beam environment are much higher than the ones that can be achieved using radioactive sources, cosmic rays or laser setups. The preparation of the beam test does require one FTE, especially to prepare all the infrastructure and testing all the associated software tools.

3.3.1 Resources

3.3.2 Deliverables

- Provide test beam infrastructure (Mechanics, PMT fingers)
- Conduct test beam analysis of APACHE-I and APACHE-II
- Run control software

3.4 WP4: DAQ

The DAQ for the sensor is a central part of the entire project and we intend to build extensively on the experience gained the CALICE-MAPS DAQ board. The DAQ board is planned to be as versatile as possible, so it can be used for all three iterations of the processor. We will however require three different versions of the sensor printed circuit board, where the sensor will be mounted. The DAQ boards will the buffer the data before moving into a PC using Gigabit Ethernet. We prefer Gigabit Ethernet compared to USB, as it allows the usage of fibers for the readout and longer cable length, which will be very helpful especially for the test beam setups. Also readout speed and latency are much better than USB 2.0. The board itself will be using industry-standard components like FPGAs and we intend to avoid custom solutions if at all possible. From the experience with the CALICE MAPS DAQ, we intend to maintain the one sensor - one board design, since it makes scaling quite straightforward. We will also include the possibility of running a series of boards in a master-slave configuration in terms of synchronization.

3.4.1 Resources

3.4.2 Deliverables

- General DAQ board
- Daughter boards for sensor mounting
- DAQ software

3.5 WP5: Sensor Simulation

In order to minimize the number of submissions one must go through an extensive cycle of simulations trying to optimize the pixel's design before the first submission is made. For a first evaluation of basic design ideas like resolution, occupancy etc, a simulation based on GEANT4 is used. To simulate the pixel architecture itself, taking into account all the semiconductor properties, will require the usage of industry-grade software like Centaurus TCAD. This will allow us to study charge collection within the pixel in detail and optimize its design in terms of size, doping profiles, charge sharing between the pixels and further possibilities.

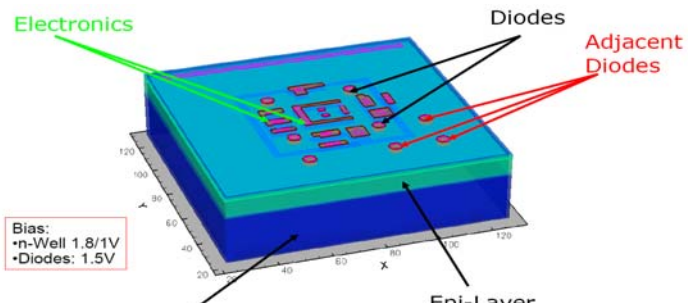

Figure 6: A MAPS architecture simulated in Centaurus TCAD, in this case the CALICE TPAC1 using a 0.18 micron CMOS deep p-well process.

An example of such a simulation made for the CALICE TPAC1 is shown in **Figure 6**

Finally, to understand the test beam data it is essential to have a well-modeled description using GEANT4 and implementing the charge spread as modeled in Centaurus TCAD.

The test beam data will also be very valuable to validate the simulation and to help improving the descriptions within GEANT4 and Centaurus TCAD.

3.5.1 Deliverables

- Physics level simulations using GEANT4
- Accurate simulation using Centaurus TCAD
- Accurate Test beam simulation using GEANT4 to compare the test beam data with simulation.

3.6 WP6: Project Management

This work package provides effort for the project management. It will also centrally manage the travel budget. The collaboration structure will look as outlined in **Figure 7**:

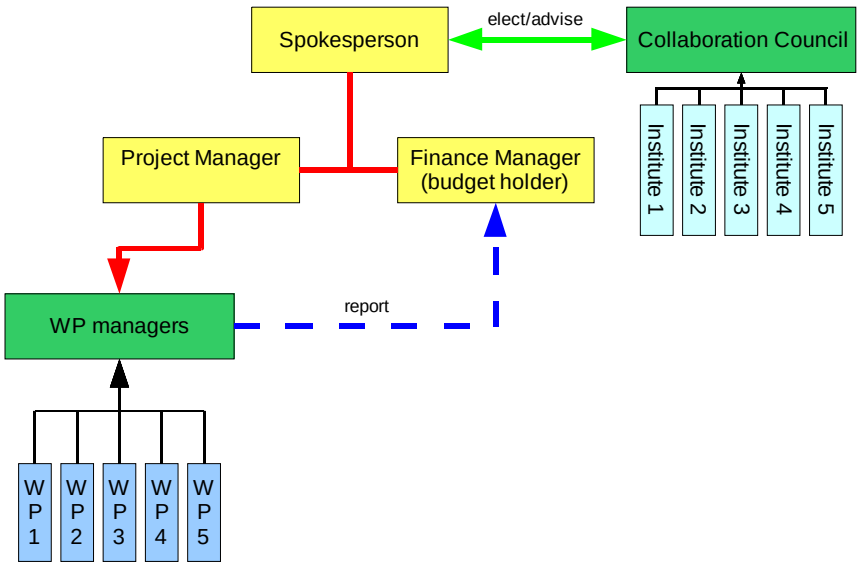

Figure 7: APACHE Collaboration Structure

3.6.1 Deliverables

- Project budget management
- Project deliverables management
- Managing the travel budget.

4. Resources

4.1 Travel Resources

We are planning on having a travel budget of 20000 GBP a year, which can be roughly split in 6000 GBP a year for travel within the UK and 14000 GBP for European and international travel. While this includes a few conference participations, we also expect a significant amount of travelling to our industrial partner foundries and to the test beam facilities at DESY, CERN and Fermilab.

4.2 Effort

The total Award would be £ 2.8 over three years, which would be sufficient to achieve all the goals of the project.

5. Project plan and Milestones

An outline of the project plan is shown in **Figure 8**, illustrating all the necessary steps and also shows the nice interplay between the different work packages.

5.1 Deliverables

The deliverables of the individual work packages have been summarized there, for the entire project we foresee three deliverables, the three chip generations with accompanying simulation work, radiation studies and test beam results

- APACHE-PRE

- APACHE-I
- APACHE-II

6. Summary

This proposal aims at developing intelligent MAPS pixels try to address several of the limitations of current pixel architectures and will be a corner stone for upcoming pixel developments in the next decade. The technology developed will allow the UK to stay at the forefront of detector development and to be leaders in any upcoming experiment.

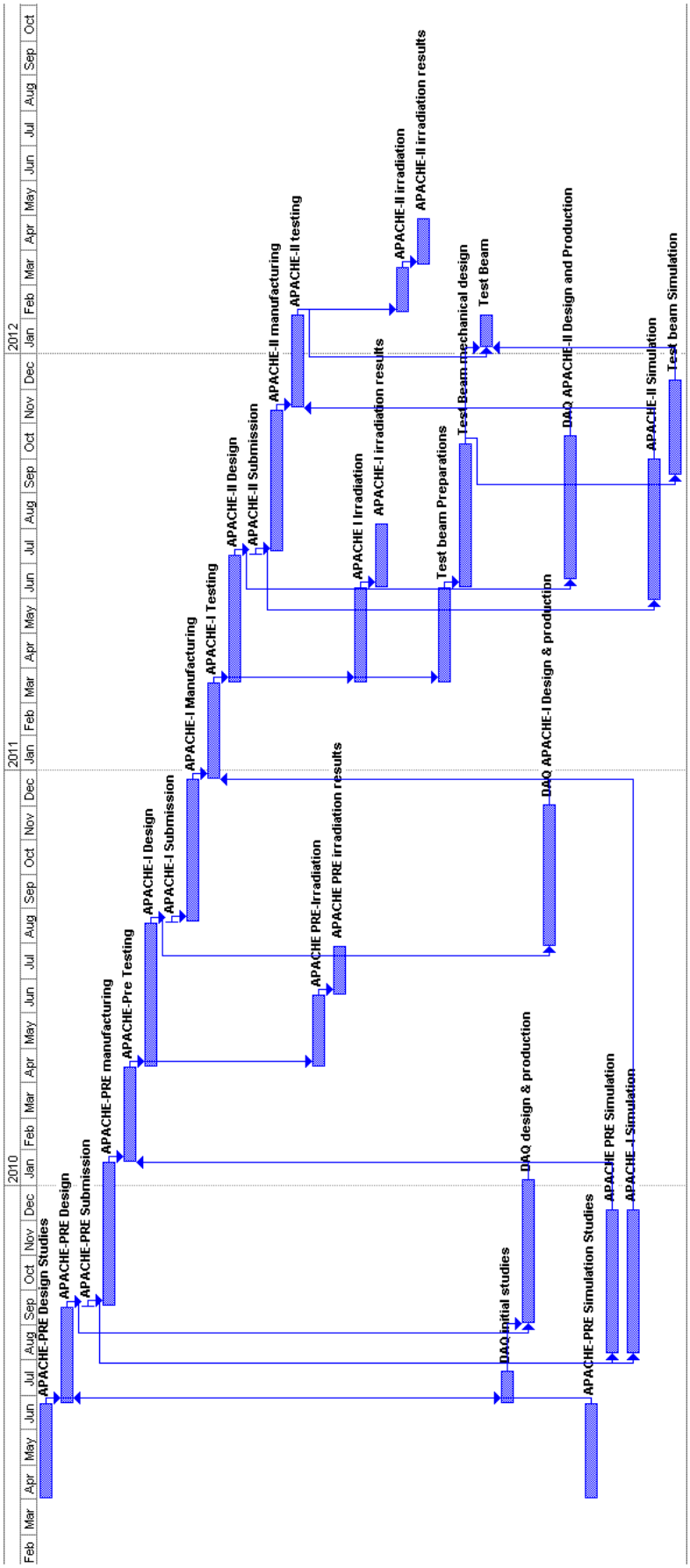

Figure 8: Project timeline

Appendix A References

1) **Detector backgrounds for a high energy muon collider.** O. Benary (Brookhaven) , S. Kahn, I. Stumer (Tel Aviv U.) . BNL-67248, Sep 1999. Prepared for Workshop on Studies on Colliders and Collider Physics at the Highest Energies: Muon Colliders at 10-TeV to 100-TeV (HEMC 99), Montauk, New York, 27 Sep - 1 Oct 1999. Published in **AIP Conf.Proc.530:1-12,2000**. Also in *Montauk 1999, Colliders and collider physics at the highest energies* 1-12