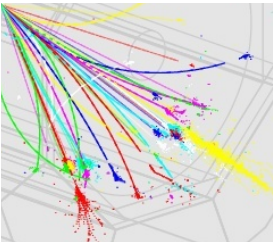
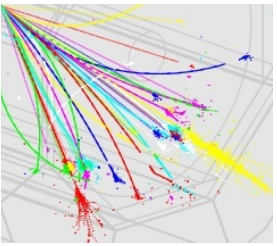


High resistivity EPI

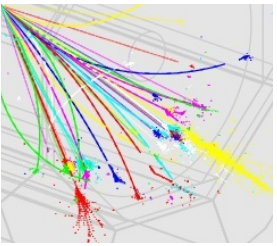
RAL 04/06/2008

J. Crooks, M. Stanitzki, R. Turchetta, G.Villani



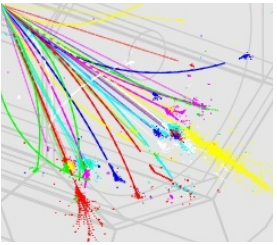
Why High resistivity EPI

- A standard INMAPS
  - Collects charge by diffusion
  - has charge spread
  - Only uses part of the epi layer ...
  - charge collection efficiency in the corner is about 27 %
- Moving to high-res Epi
  - deplete the EPI (with ~ 1.1 Volts), so collection by drift
  - eliminate most of the charge spread
  - Should be able to use the full epi
  - Charge collection efficiency in the corner is about 38 %



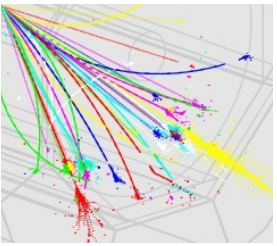
Additional benefits

- Radiation Hardness
  - The fast collection time should help making a more rad-hard MAPS
  - Something we could evaluate
- Noise
  - Depleted Silicon has a lower noise (depends how big that effect is)
  - Faster charge collection should lower noise as well
    - could use hold to gate the signal
    - Simulation to verify this
  - In general I expect superior noise performance



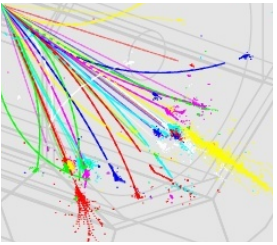
More benefits

- Make use of thicker epis
  - can have 20 µm epi and fully deplete it (means going from 960 to 1600 electrons)
  - could trade of signal and amplification (power)
- Fast charge collection vital for a warm machine
  - Also good for a cold machine



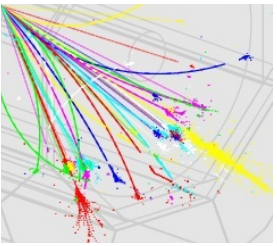
Preliminary simulation

- Giulio made some quick studies
- Charge collection in the corner goes from 260 to 310 electrons (20 % gain)
- At the edge between two diodes from 281 to 455 electrons (60 % gain)
- collection speed at least factor 2 faster
  - theoretically I'd expect it to be around 15 ns
  - that's only for a strip detector



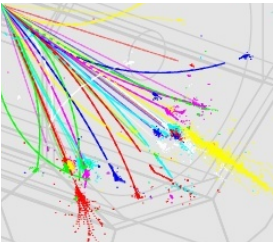
Risks

- Electronics remains unaffected
  - but need deep-p well everywhere
  - issue of charge under the logic strip
- But risks during processing
  - latch-up
  - charge-up
- Layout changes minimal
  - Guard ring
  - Deep p-well everywhere



Solutions

- Processing
  - Foundry A knows what they are doing
  - have test structures on each wafer (Process control)
  - if they say they can do it, we should value their opinion
  - CMOS foundries can't afford a bad reputation these days
- Deep p-well under the logic strip
  - charge there will leak to adjacent pixels making the over efficient (they seem to be under efficient now)
  - do we build up charge there ?
  - we could have a diode-style n-well there, which collects the charge ...



Comments

- high-res epi could be big ...
  - make a fast MAPS
  - keep our technological advantage
- Risks are small
  - but as always non-zero
- This is R&D we should do !
  - we took the same risk with the deep p-well