TPAC1.1 progress

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Status

- FDR changes
  - Single variant ② implemented across all bulk pixels
  - Pixel layout changes as recommended
  - New resistor layout(s)
  - New test pixels - as 3x3 blocks of old/new shaper design
  - Larger bond pads
  - Assorted test devices to occupy spare pad sites
  - Changes for Hi-Res processing
- LVS & DRC
  - Top (without pads) ok, including 18 test pixels
- To do
  - Add test devices to top level schematic/layout
  - LVS including pad cells
  - Antenna checks
  - Auto-fill where necessary
  - DRC the DPW rules
  - Tape out/in & repeat all checks

Resistors (again)

- Now have a better understanding
  - Previous suspicions were unfounded…
  - In the calculation of resistance, the drawn width is adjusted by a $-\Delta W$ term which is large relative to our W: ~O(30%)
  - Some earlier versions of the tools incorrectly omitted this term, leading to incorrect resistance calculations and my subsequent misunderstanding

- Potential issue with resistor matching
  - Various contributing factors in processing
  - Foundry will send me some more data on variation of this ΔW term
  - Mismatch models probably don't account for variation of this term
  - Recommended minimum width makes this ΔW insignificant: ~O(3%) but is impractical in the pixel.
  - Most likely cause of lower-than-expected gain in shapers, although the drawn geometry was actually ok

- Recommended action
  - Target 4Mohm (as original design) but use the larger available space to increase resistor width to improve potential issues with ΔW.
  - Can achieve 4.2Mohm with wider resistor, giving ΔW= ~O(21%)
  - Test structure resistors of the old and new resistor that can be easily measured on each device for monitoring variance

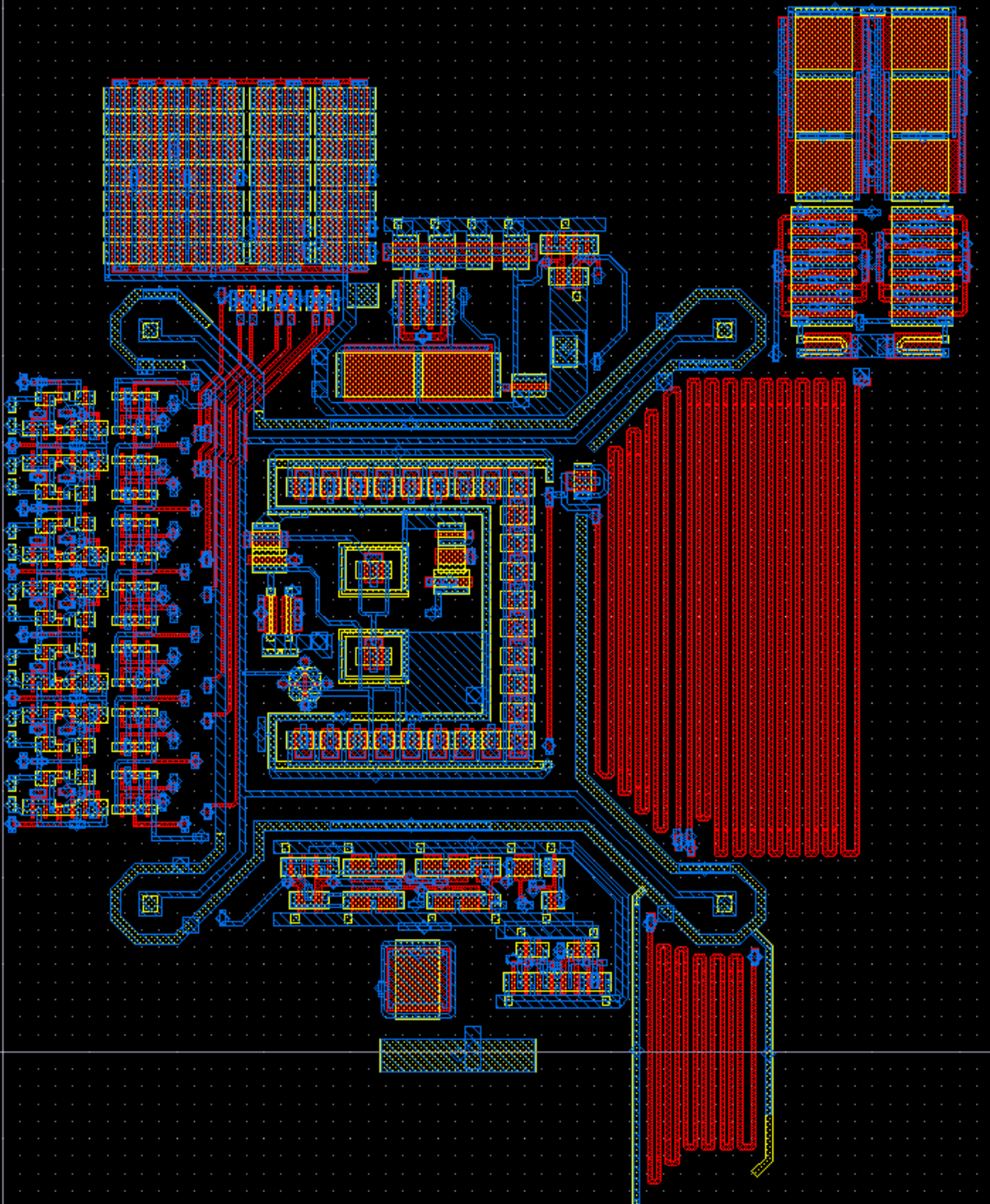# Parasitics in the pixel

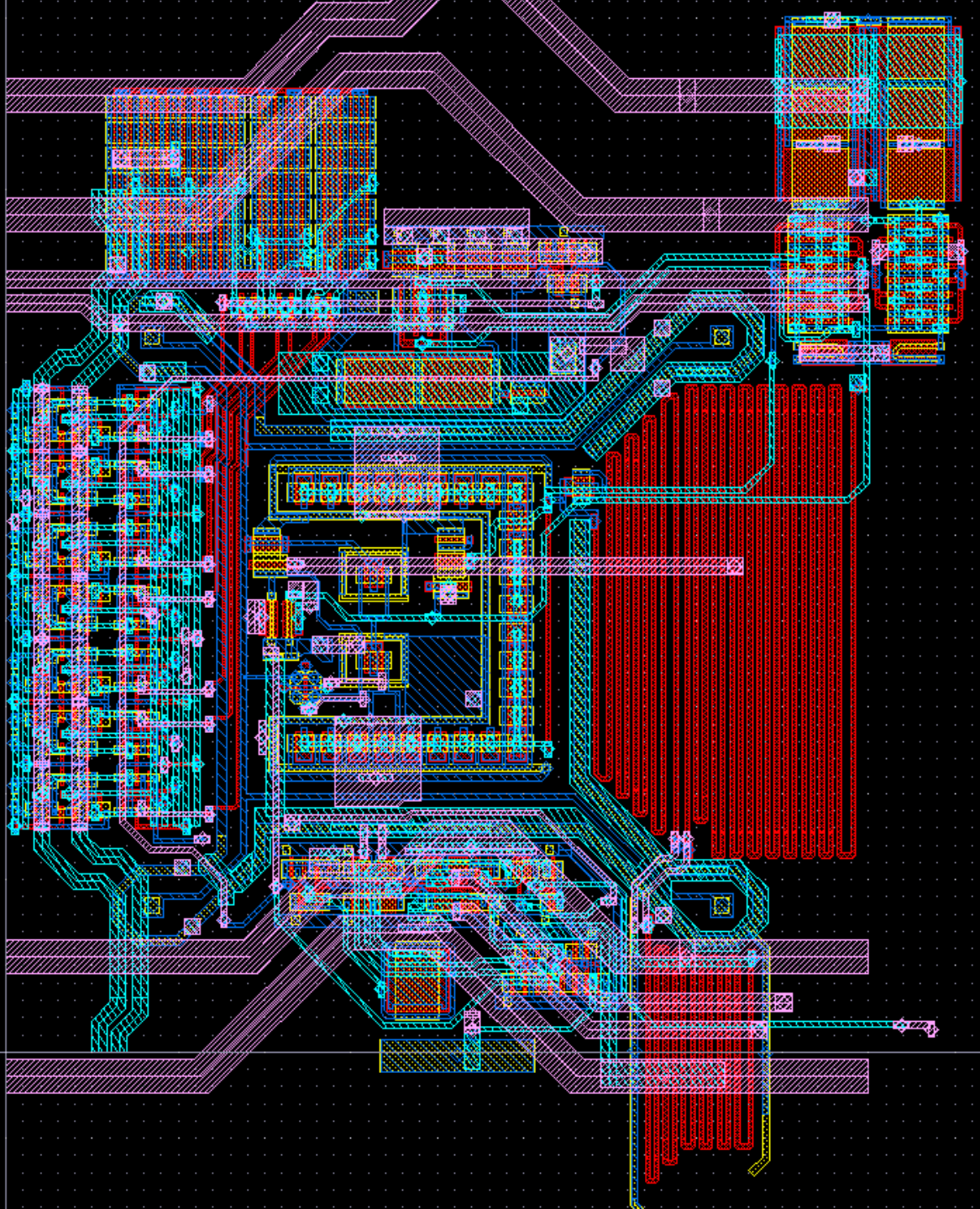- Reduced to < original design
  - 13.7fF
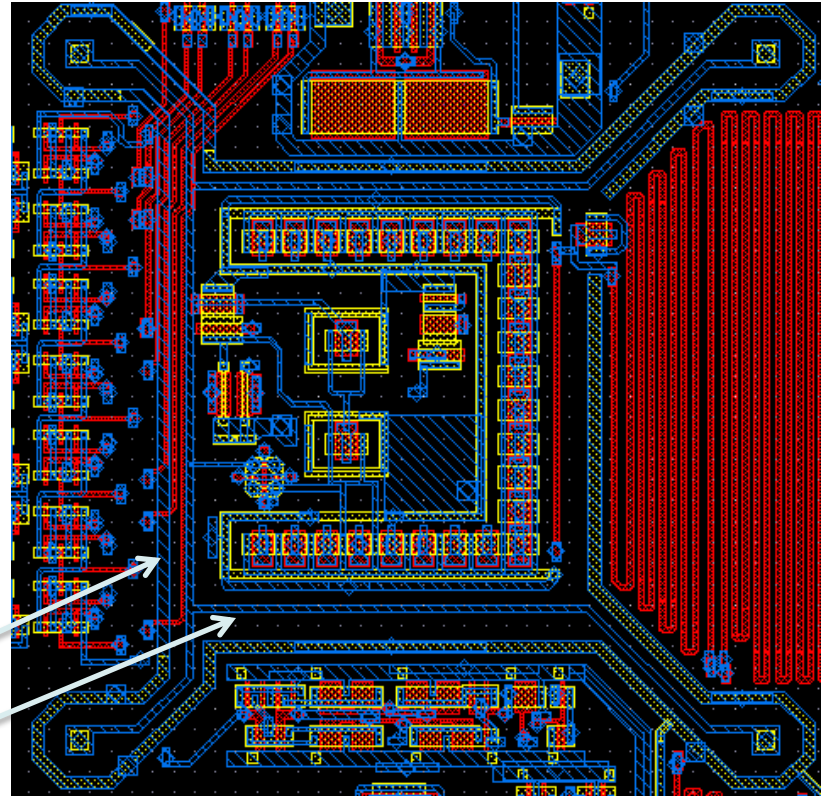
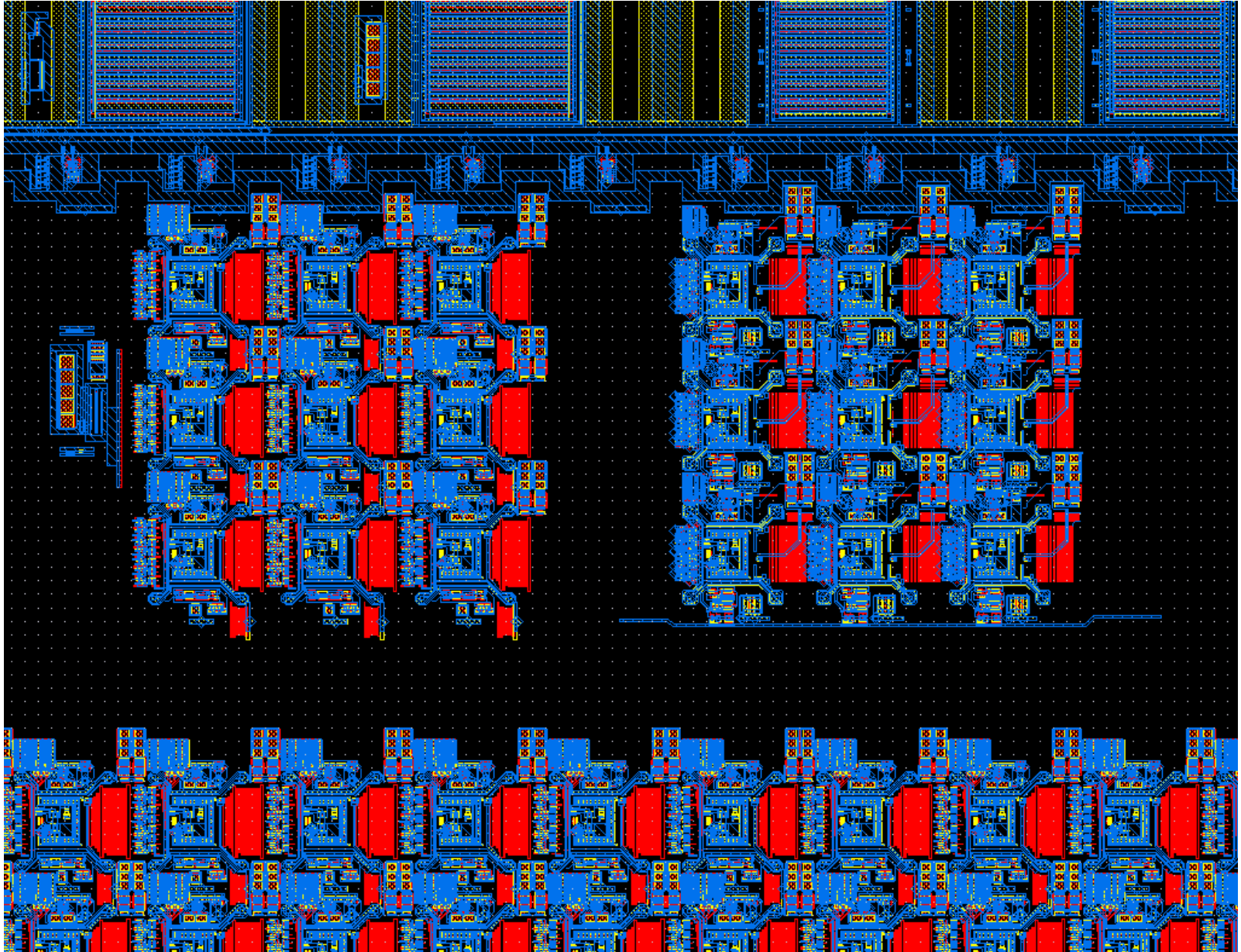Guard ring → diode node separation increased where possible
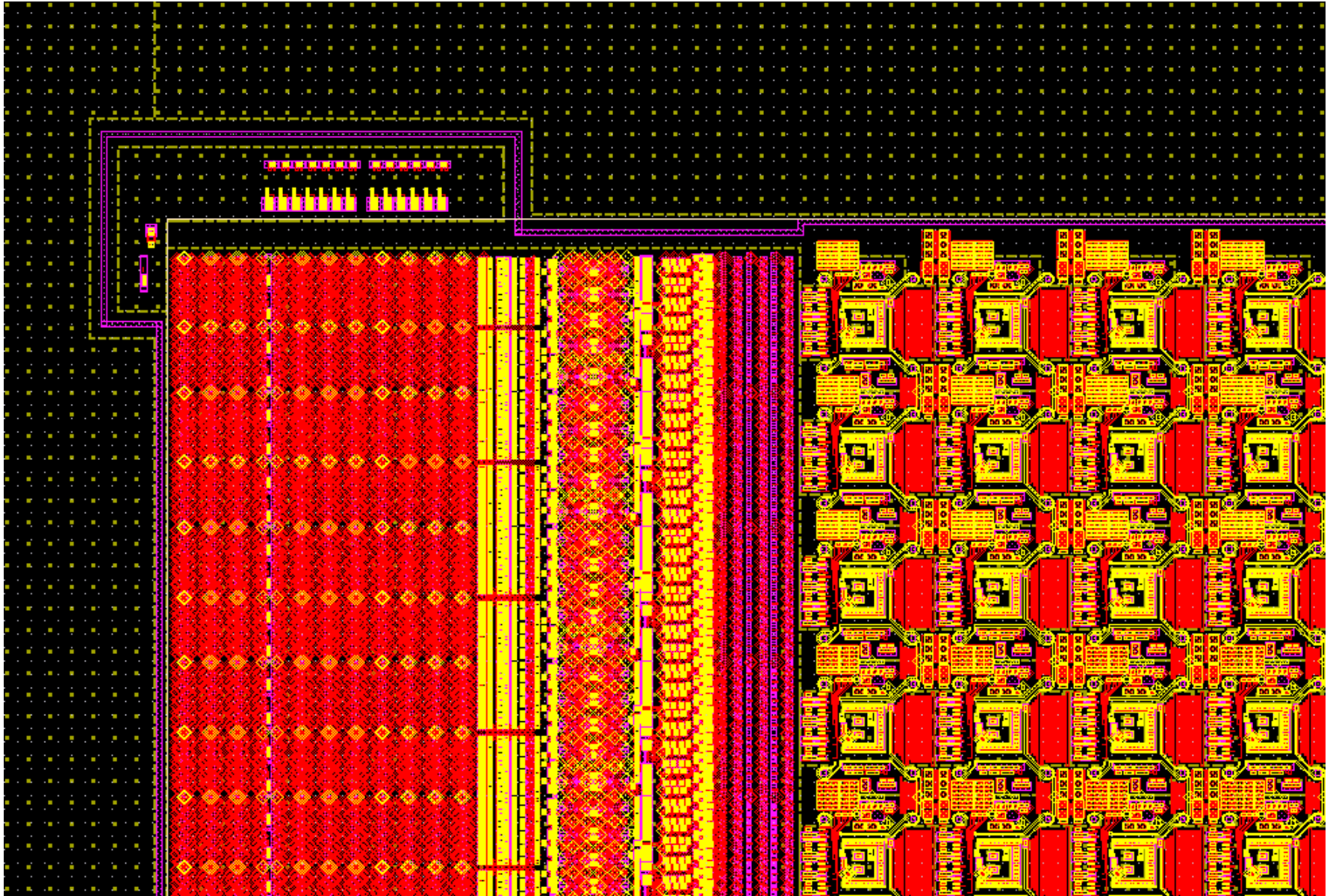
Pixel <M2

Pixel <M4

Test Pixels

Changes for Hi-Res Epi

- Placed a NWELL guard ring around the bulk pixels
  - 2.1um wide constant track around bulk pixels & logic
  - Connected to old VRST pads for external drive
    - (jumper/dac on PCB)
  - Additional guard ring around test pixels
- Placed DPW everywhere except pixels

Guard ring: Example

Test structures

- Transistors
  - Nmos (lv/hv) for characterisation, noise measurement, based on unit cell based on input transistor in preShape pixel design — 15
  - Pmos (lv/hv) for characterisation, noise measurement
  - Additional long device (TBC)

- Diodes
  - 1000 diodes for leakage current measurements — 2

- Capacitors
  - O(1pF) made from the 1x1um pixel cells in parallel
  - O(0.5pF) made from parallel units of 2 series capacitors — 3

- Nwell-Nwell isolation — 3

- Resistors — 2, 5
  - Original 4MΩ
  - New wider 4.2MΩ
  - 2* 4MΩ resistors with larger widths to monitor matching/variance for future projects

- Foundry will place an extra strip of their standard PCM structures — 0
  - One with, one without DPW
  - Will be tested as part of their standard procedure → immediate and directly comparable data for identical structures with/without DPW