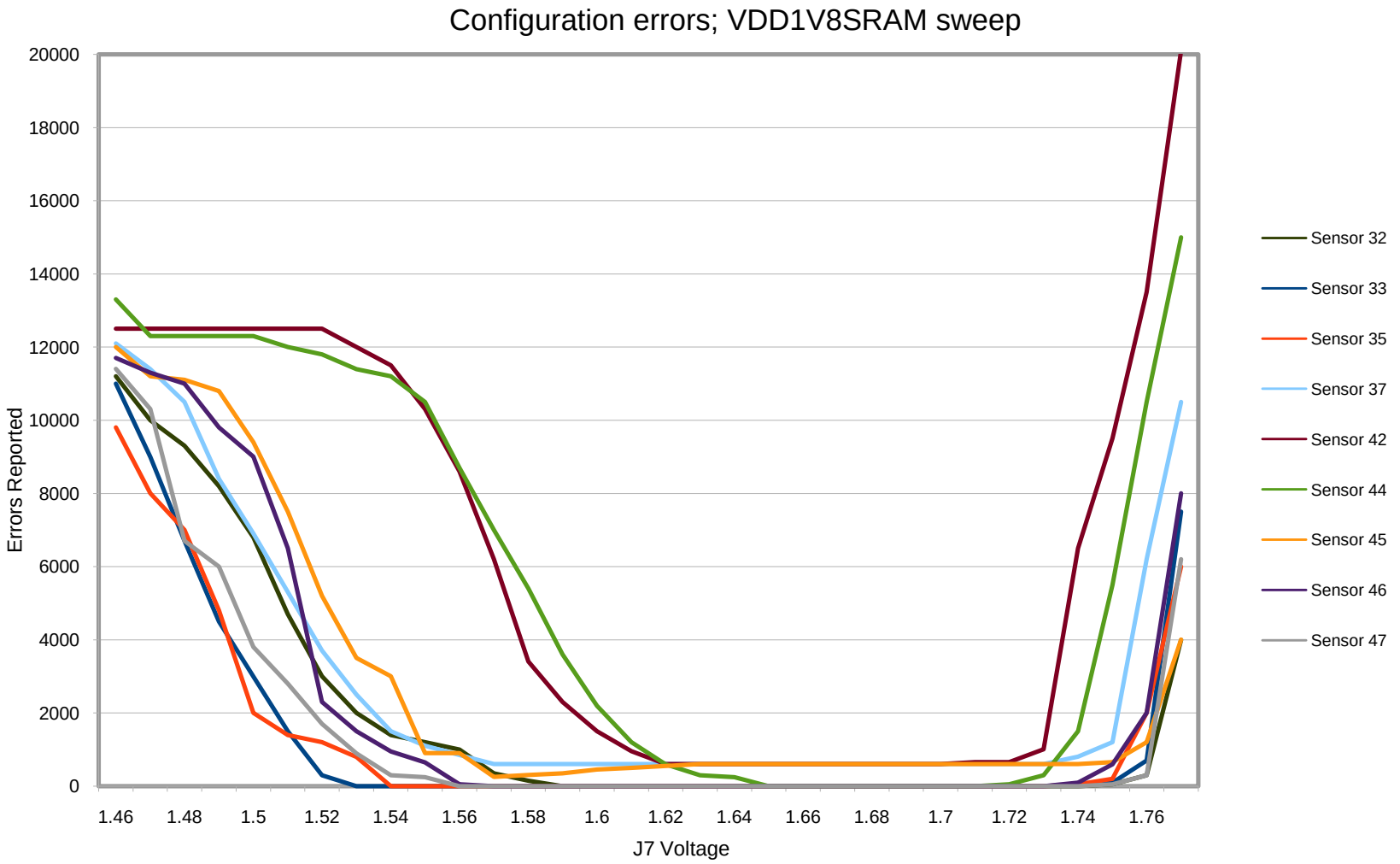
TPAC1.2

JC / 1st July2009

Results from Barnaby Levin (summer student)

Config load errors

- Vary VDD1V8SRAM, plot configuration errors (random data)



Conclusion

- Single-column defects are generally “real” ie cannot be fixed by adjusting VDD1V8SRAM
- Nominal voltage 1.62v (±2%) as previously set up is generally good
- Two sensors tested are “on the edge” at 1.62v and showed variable/increasing dead columns during trimming
  - A special version of the power dongle set to 1.68v (±2%) has been made for these boards
  - No correlation between these chips and wafer

- Similar study at different temperatures will be conducted soon