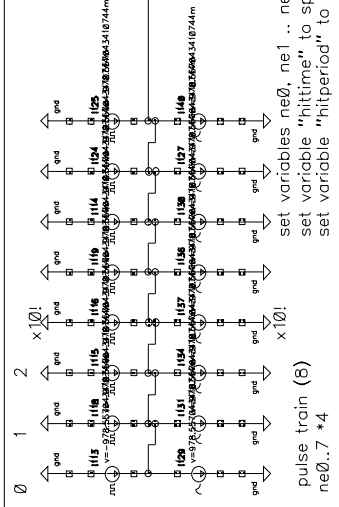
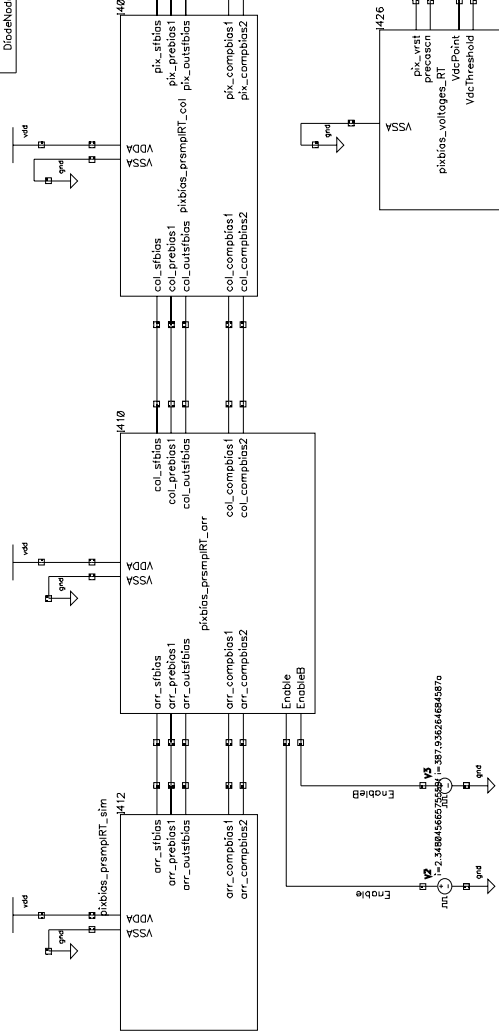
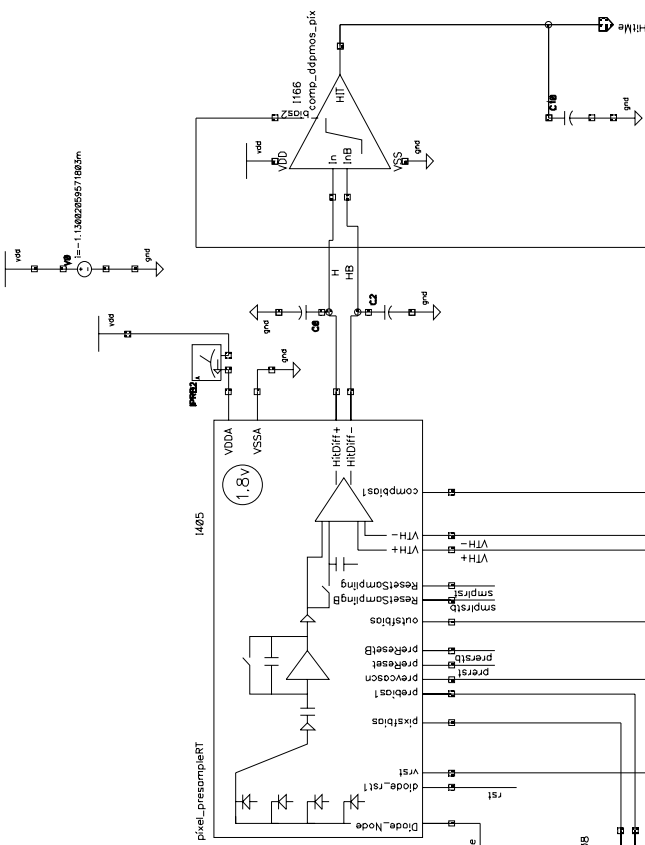


pulse train (8) with individually settable pulse heights

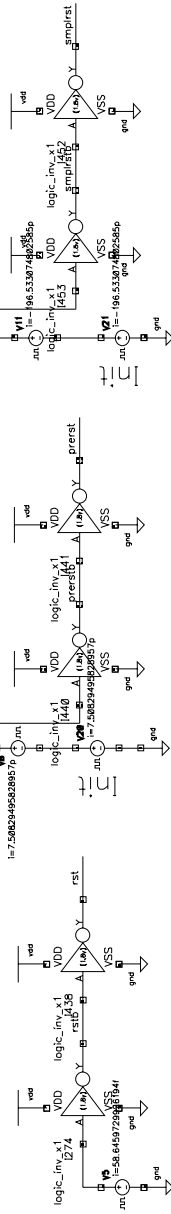


set variables ne0, ne1 .. ne7  
 set variable "hittime" to specify time of first hit  
 set variable "hitperiod" to specify interval between subsequent hits

pulse train (8)  
 ne0..7 \*4



Diode reset pulsed once at start

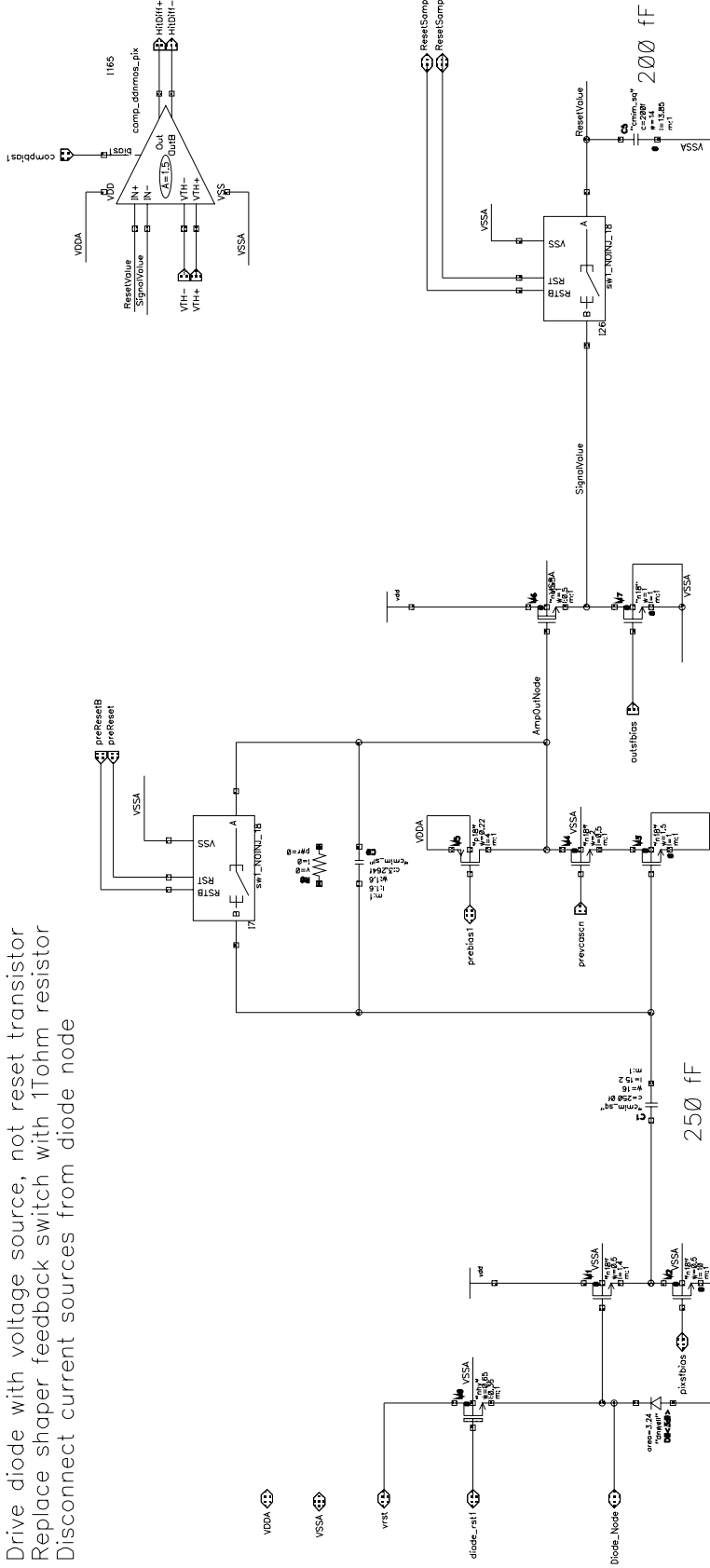


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasibility
Block Name	simplexel_presample_miph12
Last QA Review	
Last Changed	Oct 19 17:24:54 2006

For Noise Analysis:

=====

Drive diode with voltage source, not reset resistor  
 Replace shaper feedback switch with 1Tohm resistor  
 Disconnect current sources from diode node



900nA

250 fF

1.3uA

1.2uA

900nA

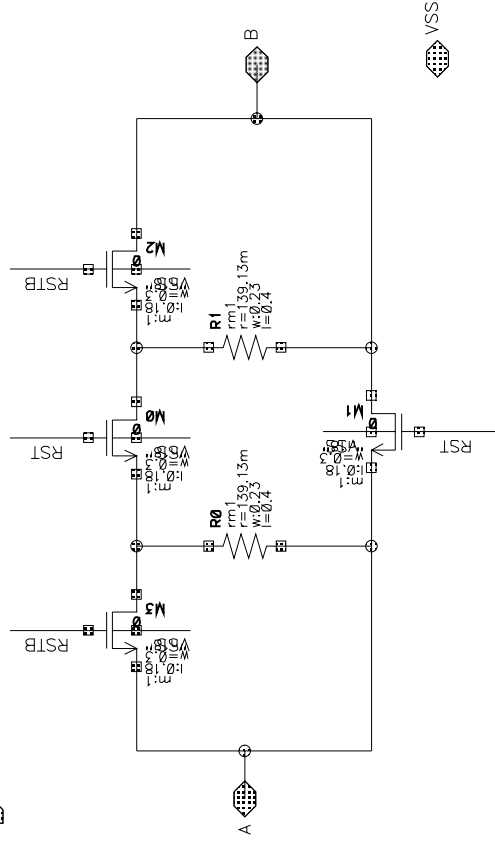
250 fF

1.3uA

1.2uA

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasibility
Block Name	pixel_presamplerRT
Last QA Review	
Last Changed	Oct 19 19:27:45 2006

RST  
RSTB

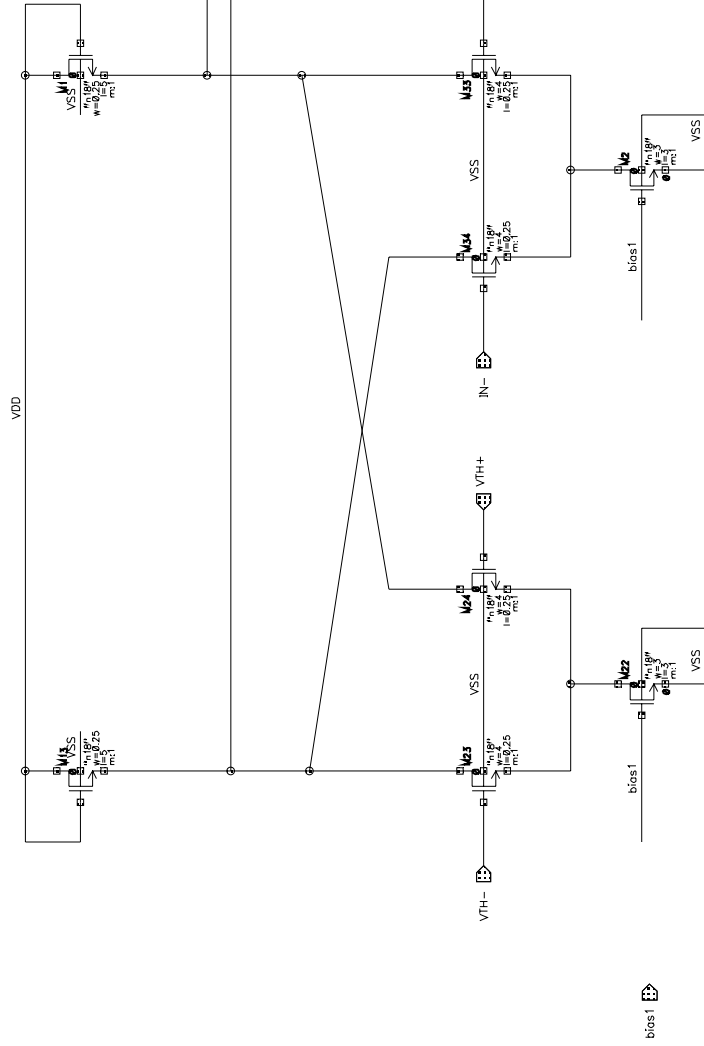


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Project	Tera-Pixel APS for CALICE
Library Name	calice_feasibility
Block Name	sw1_NOINJ_18
Last QA Review	
Last Changed	Oct 13 10:05:15 2006

VSS

VDD



differential (10s of mV)  
 hit signal wired across  
 to\_pmos comparator at r  
 logic

250nA

250nA

RAL Microelectronics Group

Project Tera-Pixel APS for CALICE

Library Name calice\_feasibility

Block Name comp\_ddnmos\_pix

Last QA Review

Oct 17 09:27:22 2006

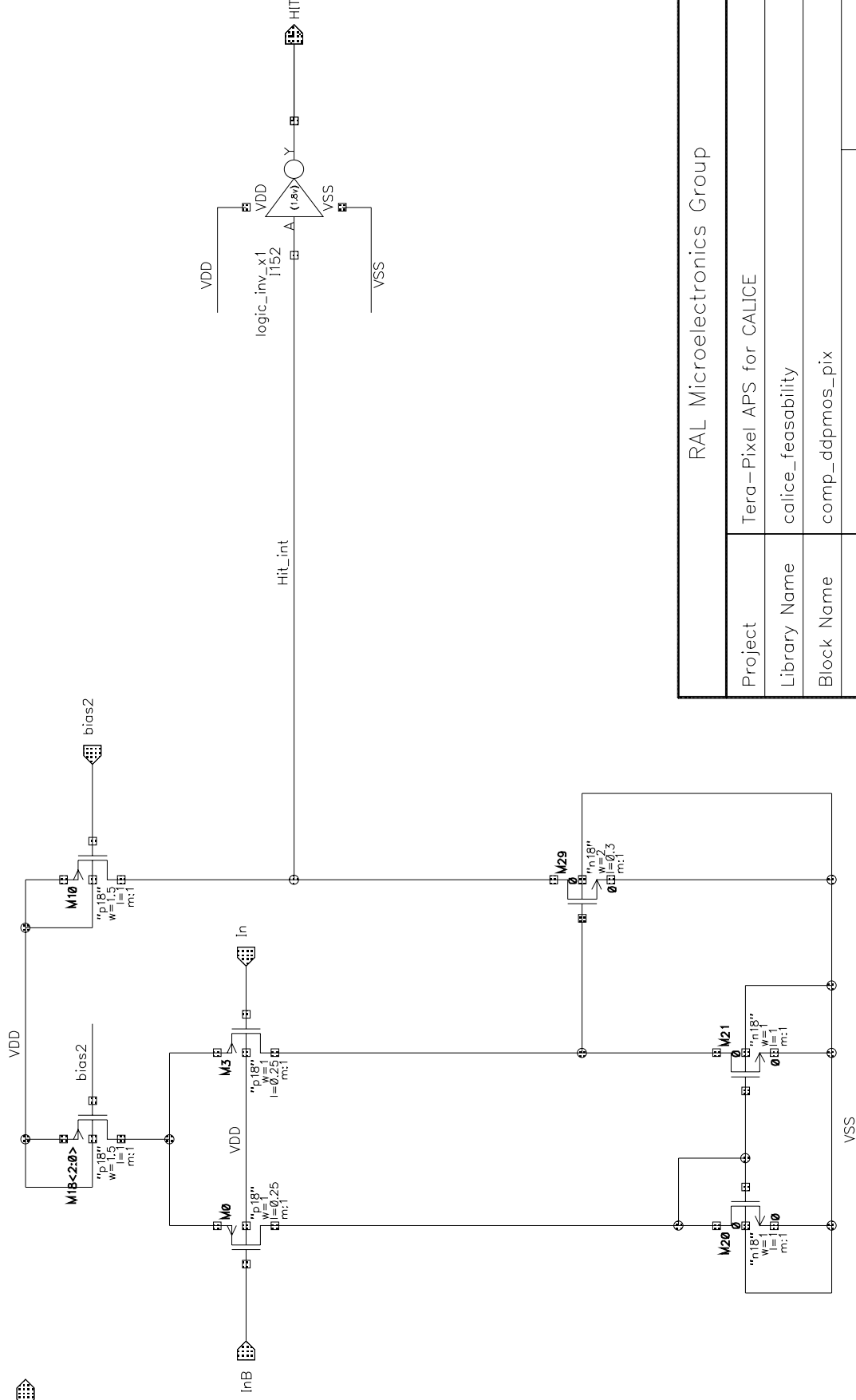
Last Changed

<<<<< AT ROW LOGIC >>>>>

VDD

VSS

500nA 250nA



RAL Microelectronics Group

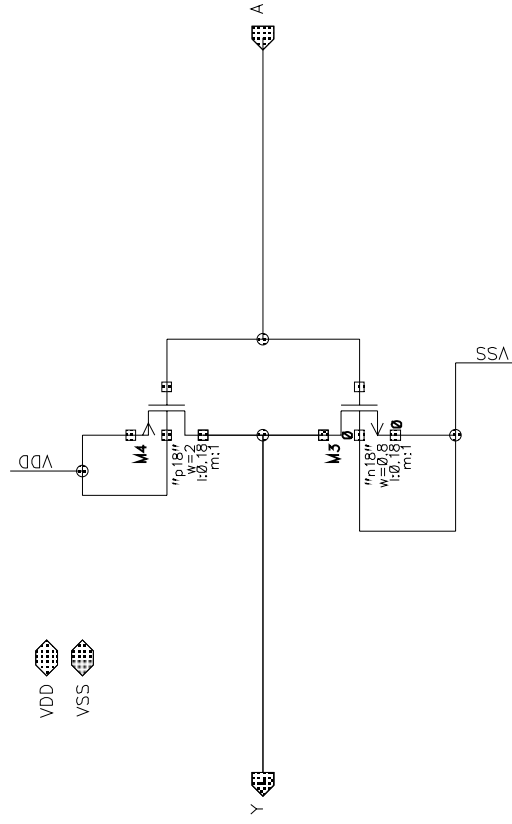
Project Tera-Pixel APS for CALICE

Library Name calice\_feasibility

Block Name comp\_ddpmos\_pix

Last QA Review

Last Changed Oct 16 18:10:12 2006

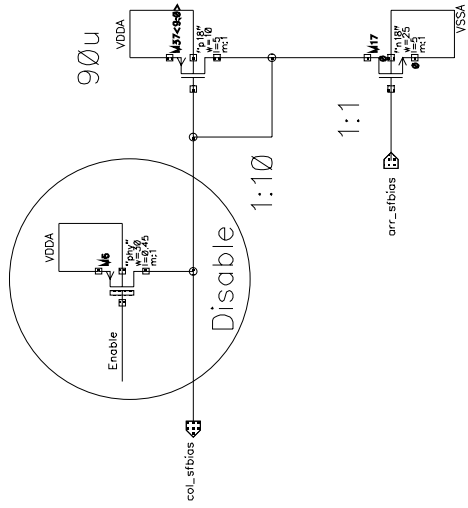


RAL Microelectronics Group

Project	Tera-Pixel APS for CALICE
Library Name	calice_feasibility
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Sep 28 11:46:11 2006

# Pixel SF

# Preamp Bias



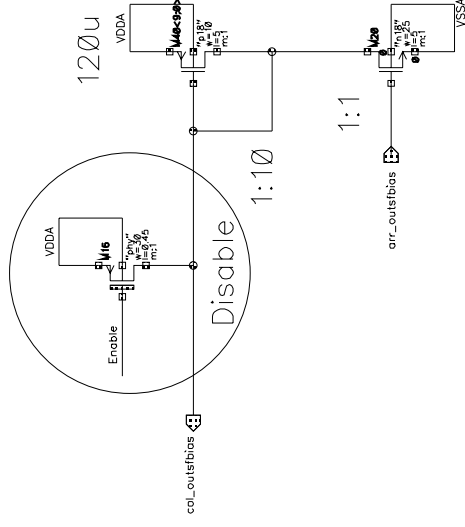
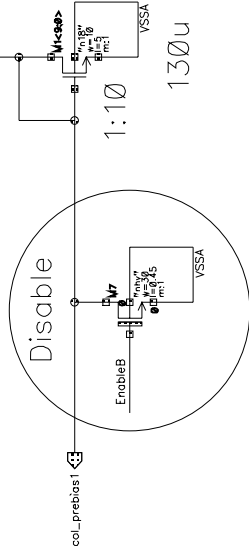
VDDA

VSSA

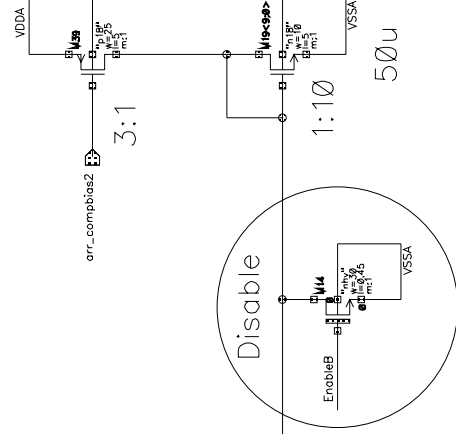
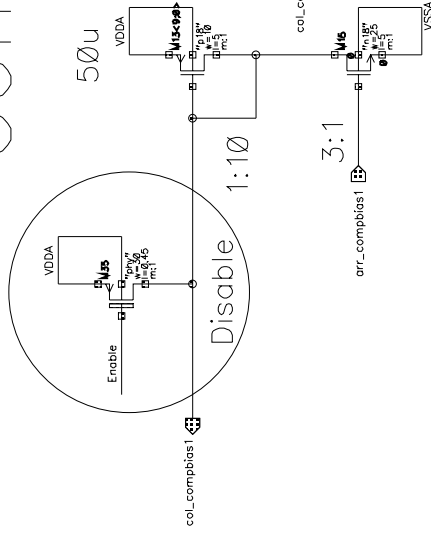
Enable

EnableB

Out SF



# Comparator



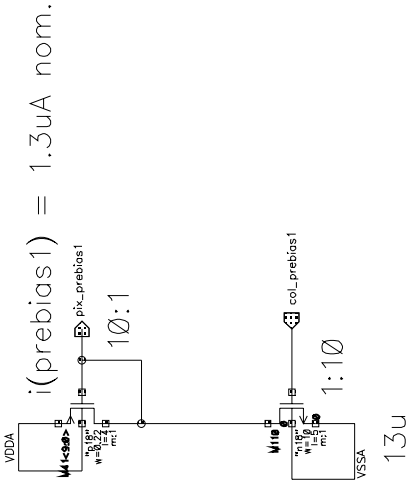
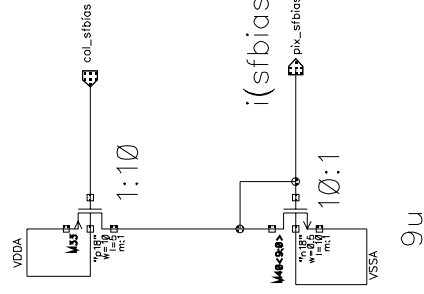
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasibility
Block Name	pixbias_prismpIRT_arr
Last QA Review	
Last Changed	Oct 18 14:29:36 2006

# ARRAY CIRCUITS

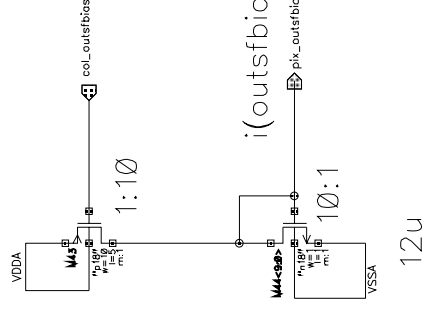
# Pixel SF

VDDA  VSSA 

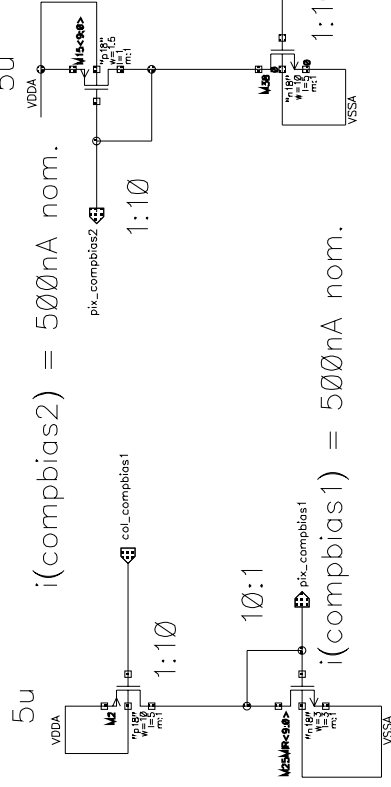
# Preamp Bias



# Out SF



# Comparator Bias

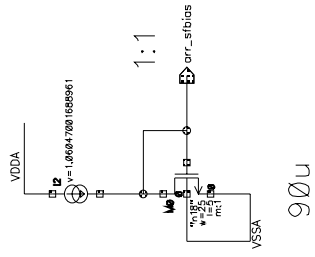


# COLUMN CIRCUITS

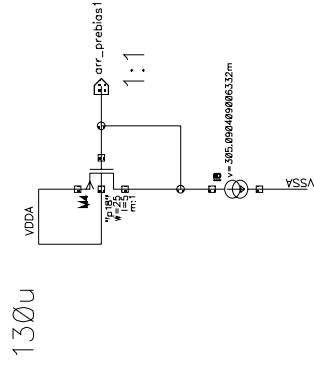
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasibility
Block Name	pixbias_prismPIRT_col
Last QA Review	
Last Changed	Oct 18 14:29:55 2006



# Pixel SF

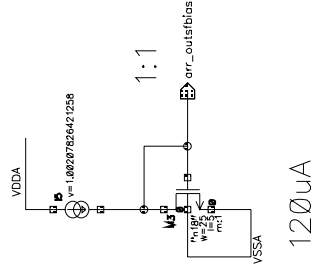


# Preamp

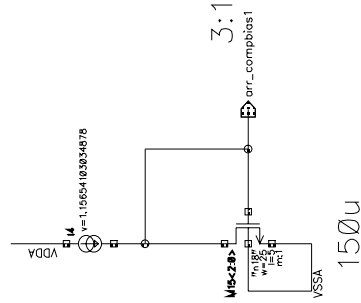
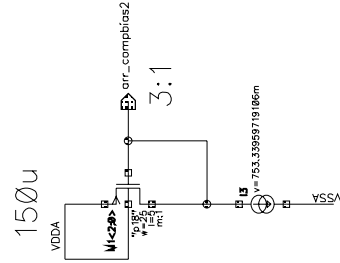


VDDA  
VSSA

# Out SF

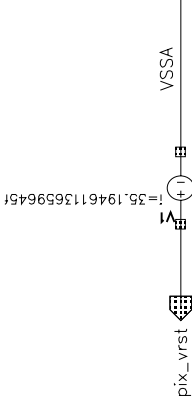


# Comparator Bias



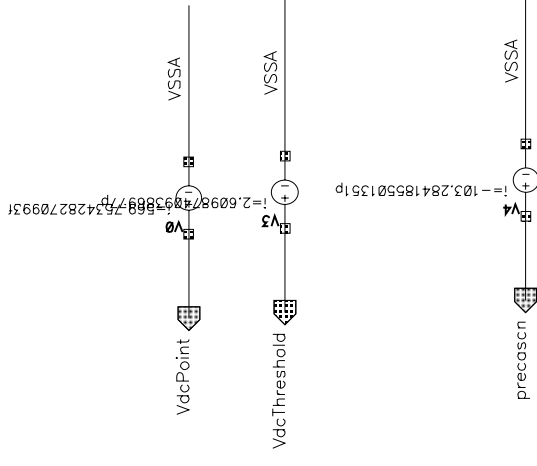
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasibility
Block Name	pixbias_prismpIRT_sim
Last QA Review	
Last Changed	Oct 18 15:09:53 2006

Pixel reset point ~1v  
for hard reset



Vdcpoint = 1.0v nom.

VdcThreshold = Vdcpoint - Vth (35mV nom)



Preamp cascode  
voltage 1.5V nom.

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasibility
Block Name	pixbias_voltages_RT
Last QA Review	
Last Changed	Oct 18 15:31:09 2006