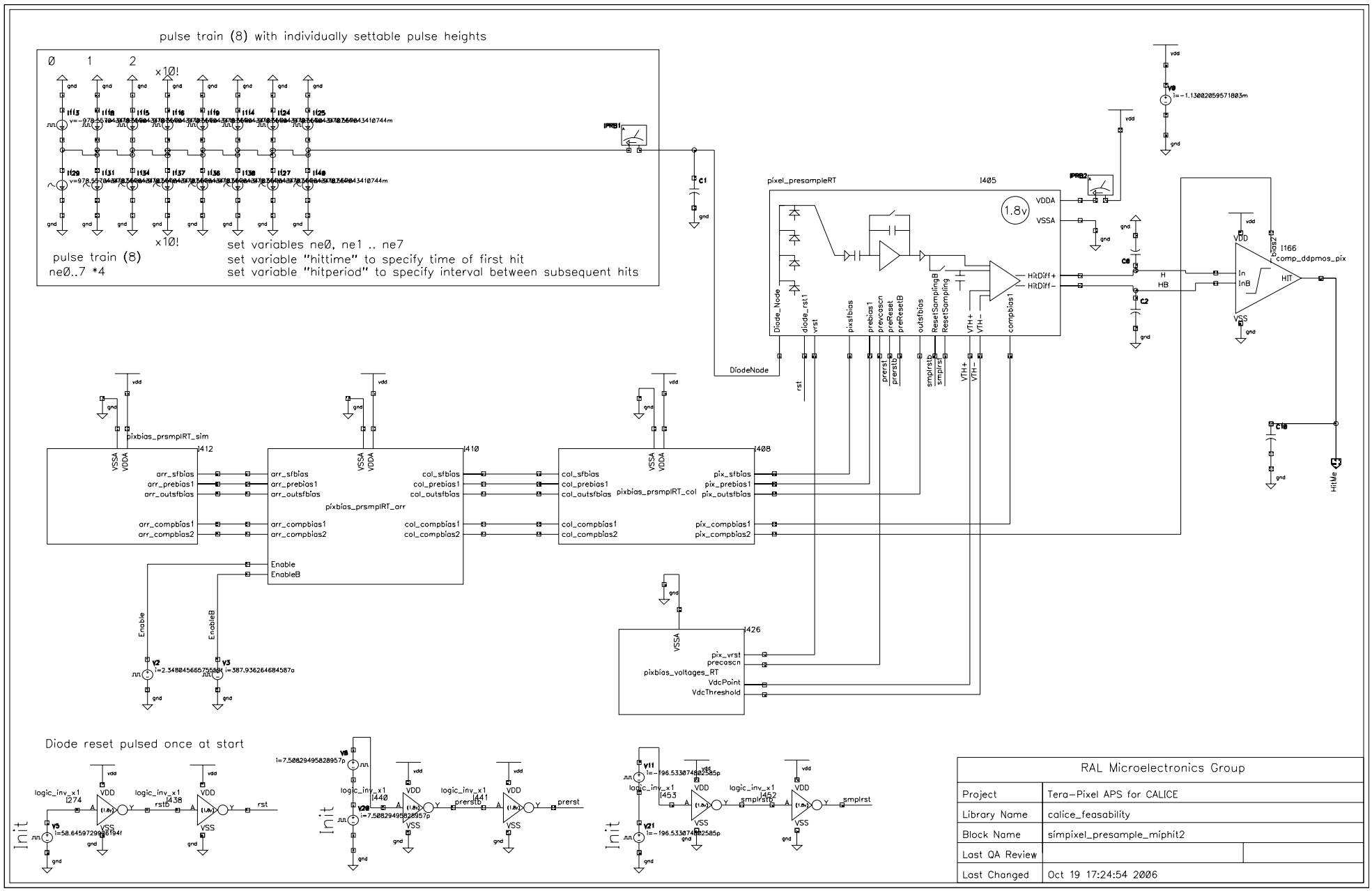
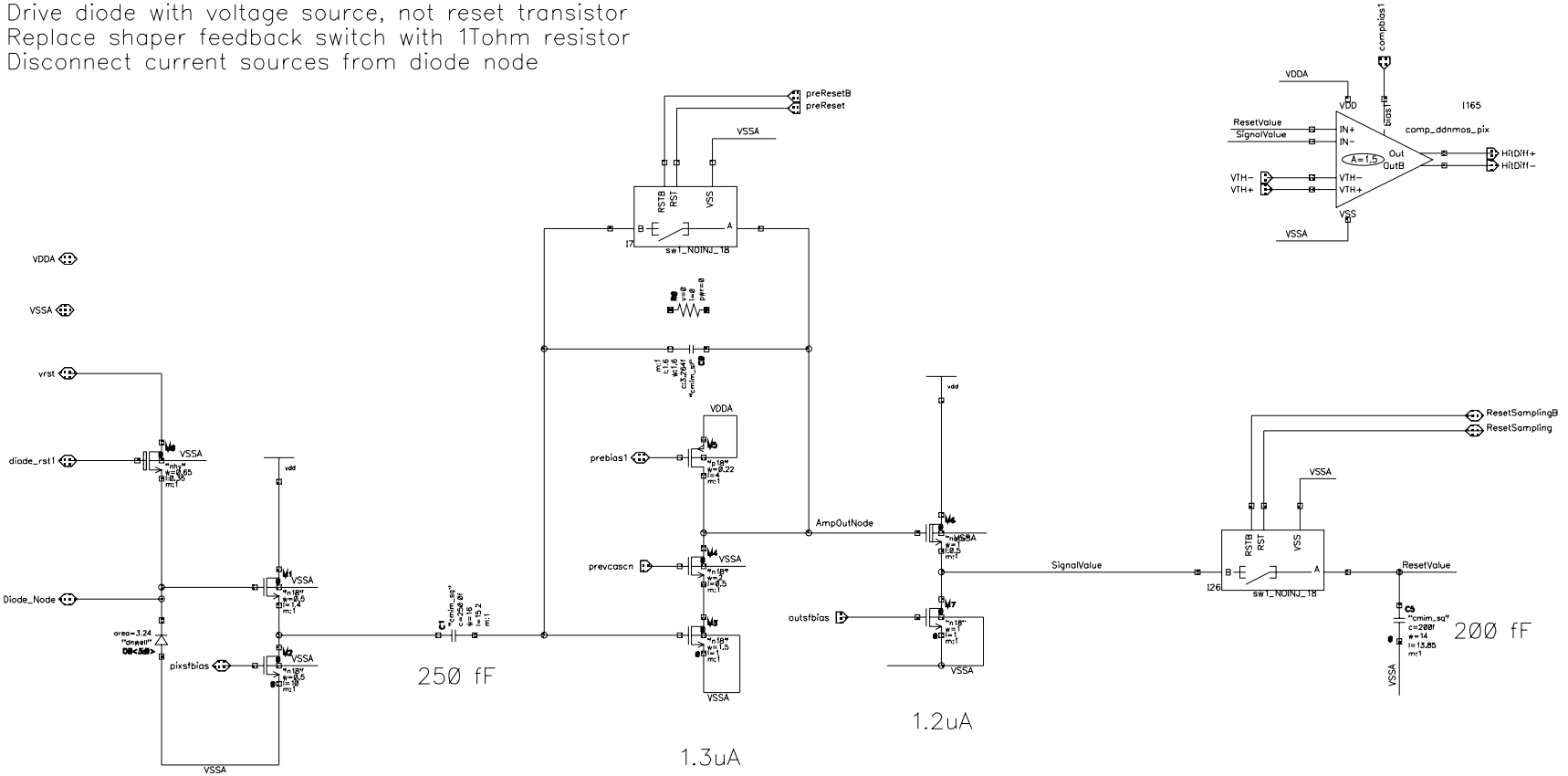


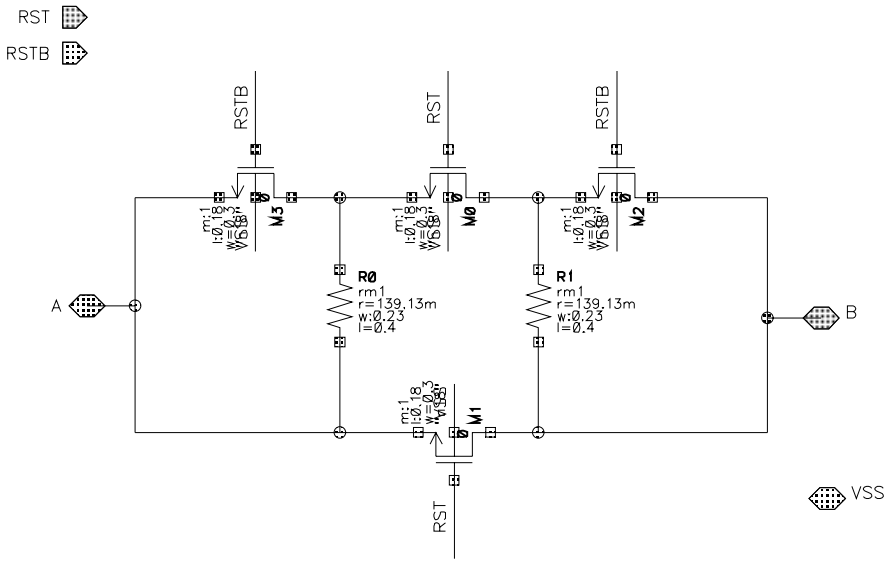
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	simpixel_presample_miphit2
Last QA Review	
Last Changed	Oct 19 17:24:54 2006

For Noise Analysis:
==========

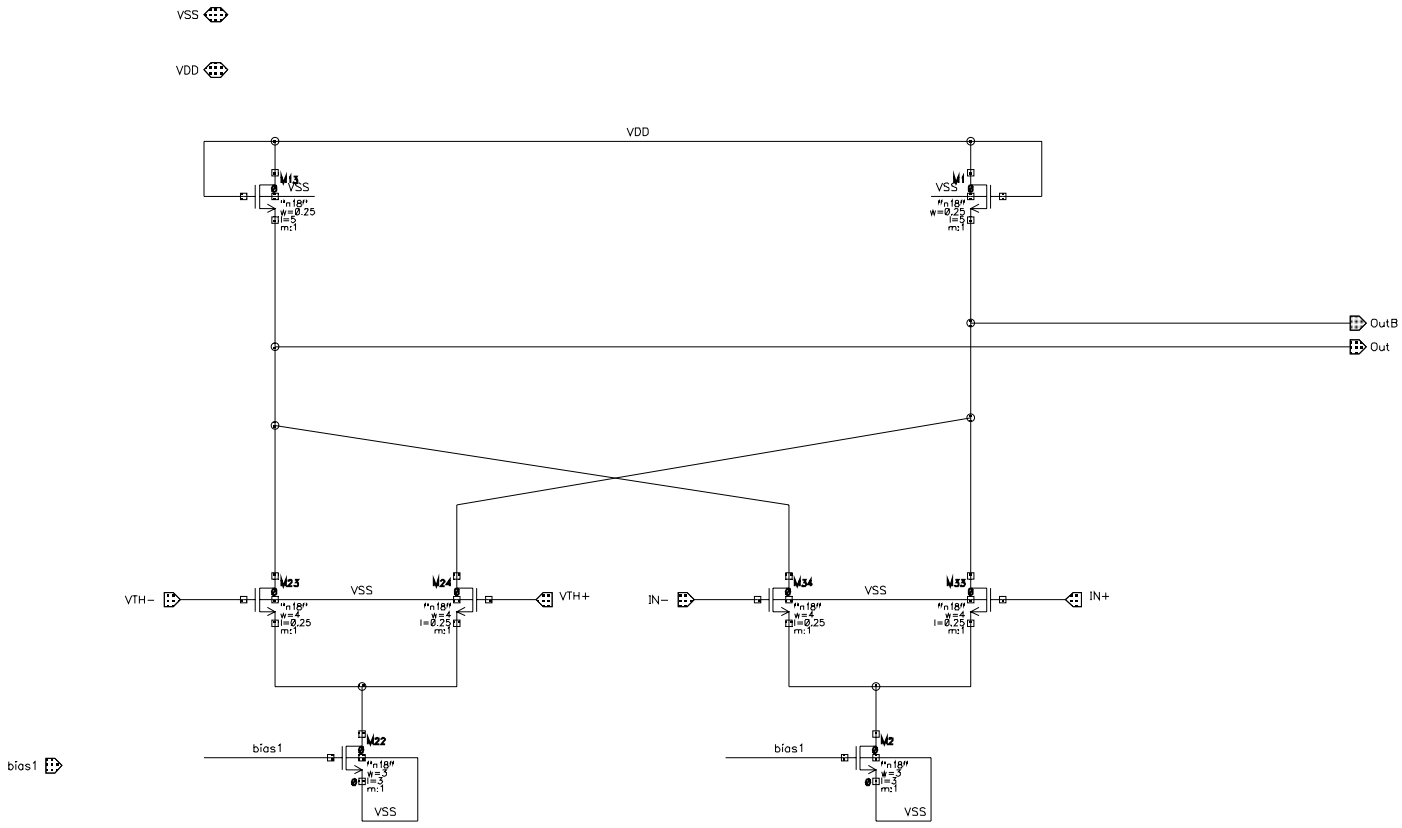
Drive diode with voltage source, not reset transistor
Replace shaper feedback switch with 1Tohm resistor
Disconnect current sources from diode node



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	pixel_presampleRT
Last QA Review	
Last Changed	Oct 19 19:27:45 2006



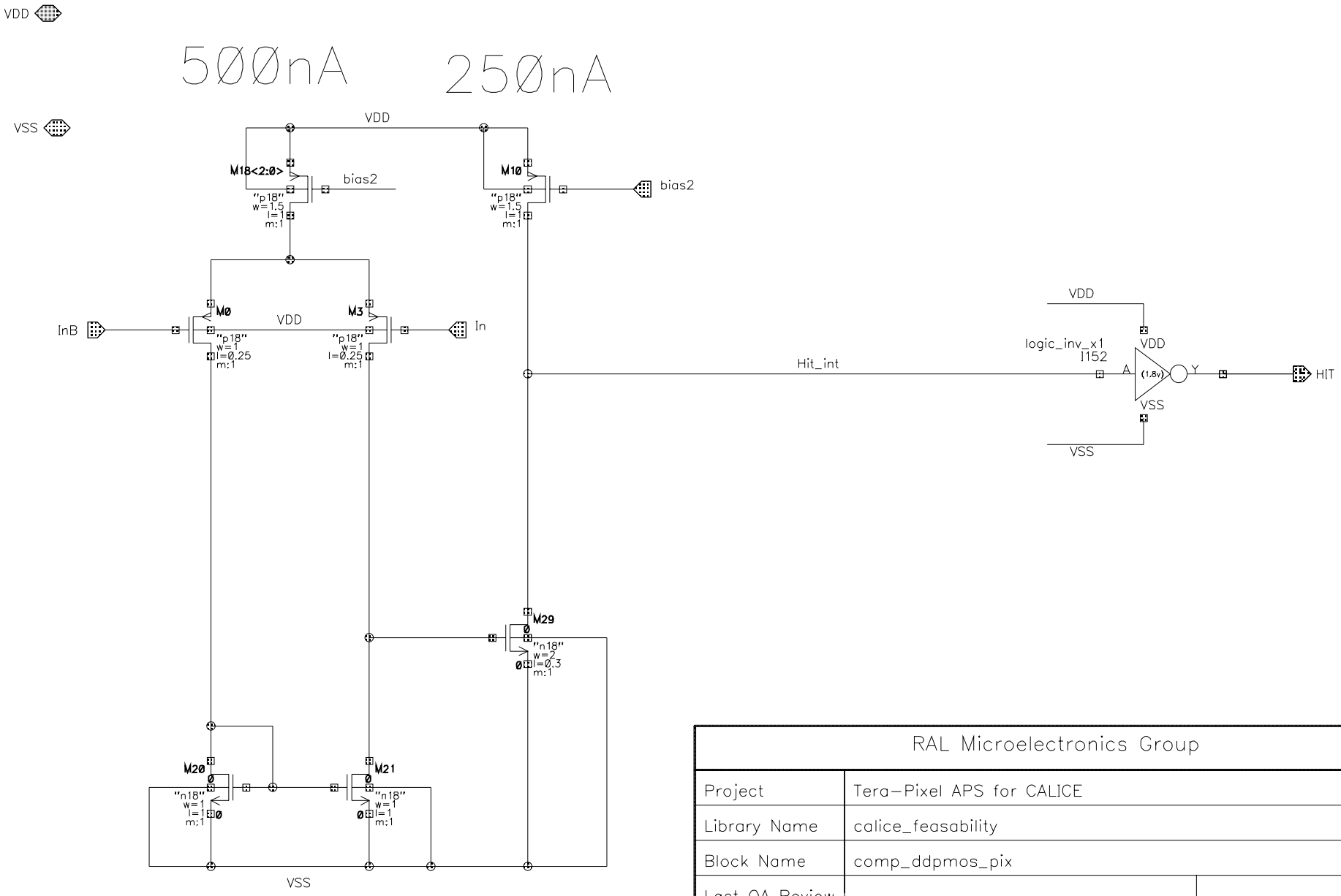
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	sw1_NOINJ_18
Last QA Review	
Last Changed	Oct 13 10:05:15 2006



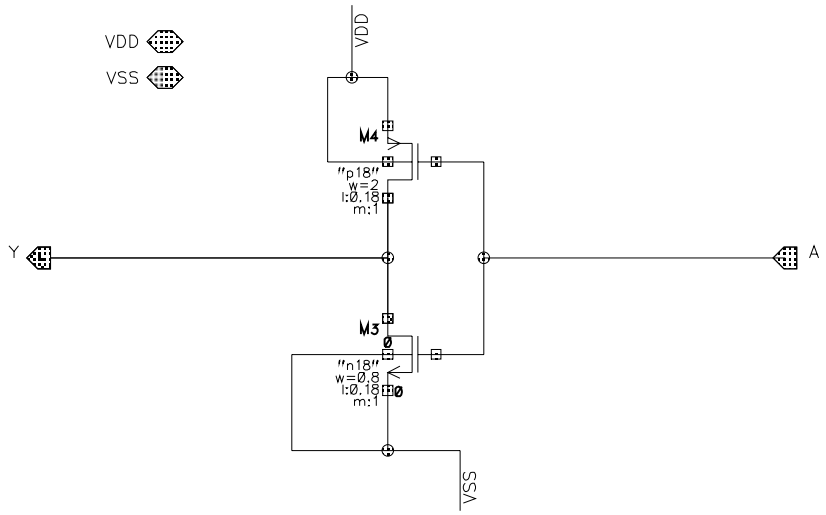
differential (10s of mV)
hit signal wired across
to pmos comparator at ro
logic

RAL Microelectronics Group	
Project	Tera−Pixel APS for CALICE
Library Name	calice_feasability
Block Name	comp_ddnmos_pix
Last QA Review	
Last Changed	Oct 17 09:27:22 2006

<<<<< AT ROW LOGIC >>>>>

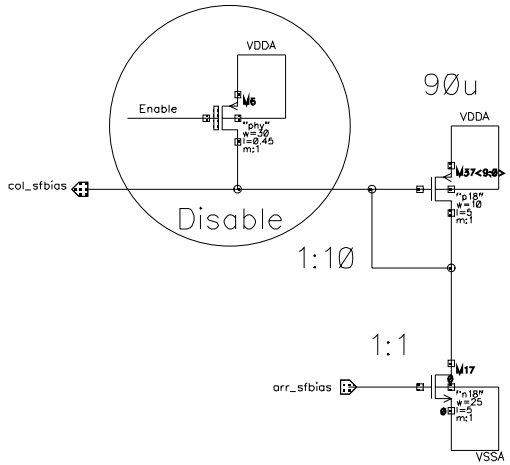


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	comp_ddpmos_pix
Last QA Review	
Last Changed	Oct 16 18:10:12 2006

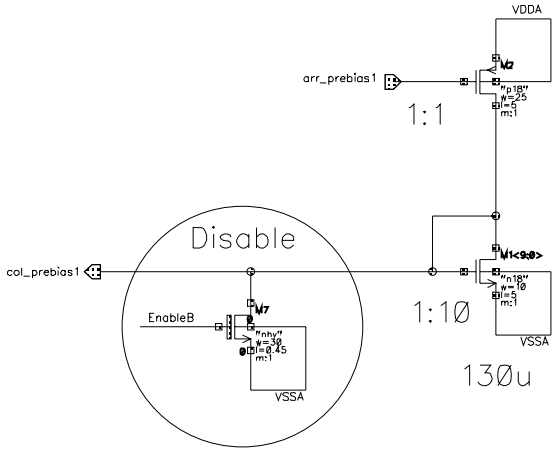


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Sep 28 11:46:11 2006

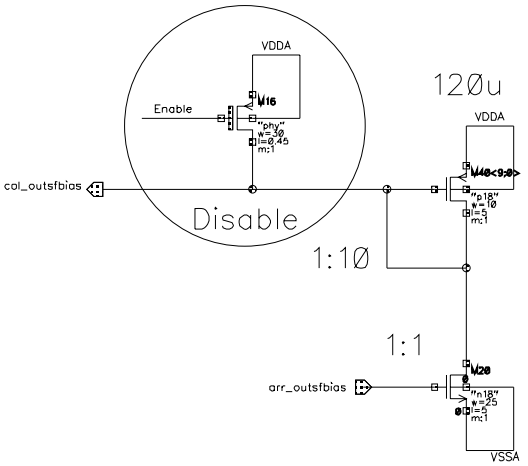
Pixel SF



Preamp Bias



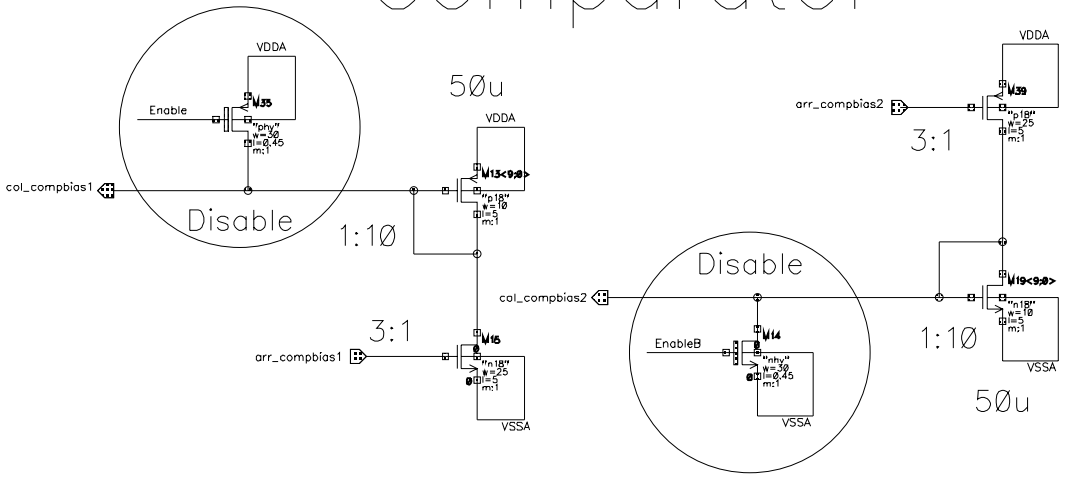
Out SF



VDDA
VSSA

Enable
EnableB

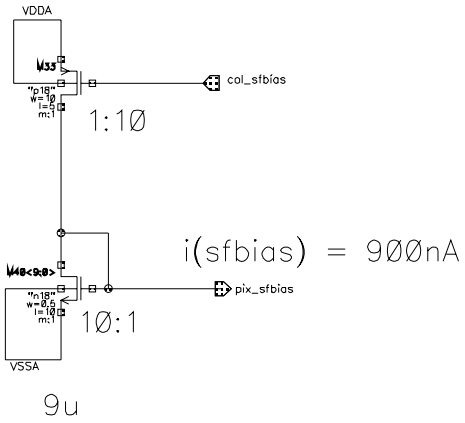
Comparator



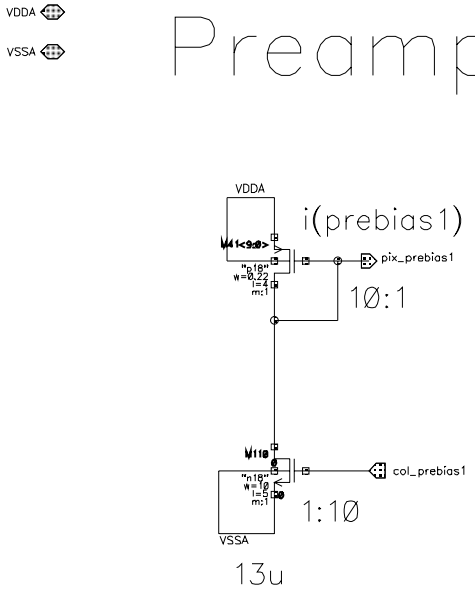
ARRAY CIRCUITS

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	pixbias_prsmpIRT_arr
Last QA Review	
Last Changed	Oct 18 14:29:36 2006

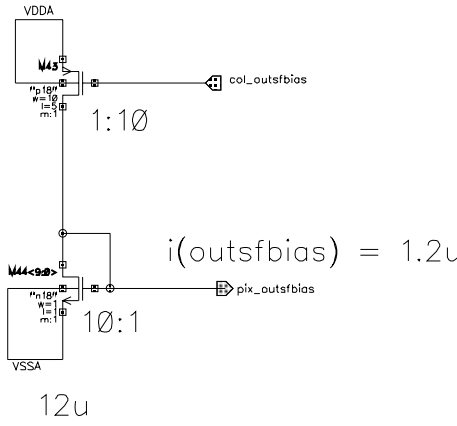
Pixel SF



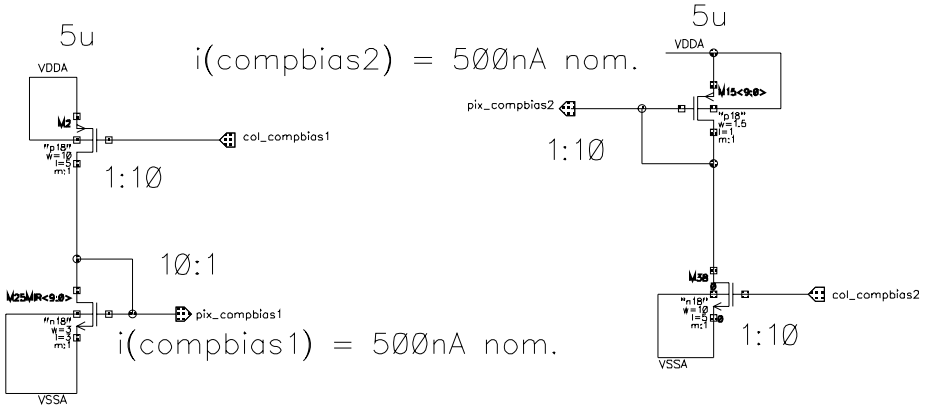
Preamp Bias



Out SF



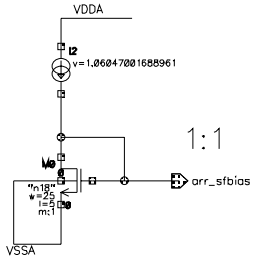
Comparator Bias



COLUMN CIRCUITS

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	pixbias_prsmpIRT_col
Last QA Review	
Last Changed	Oct 18 14:29:55 2006

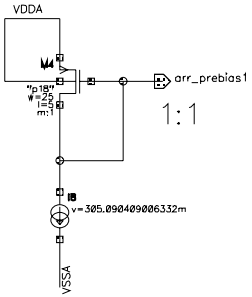
Pixel SF



90u

Preamp

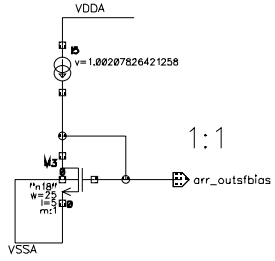
130u



VDDA

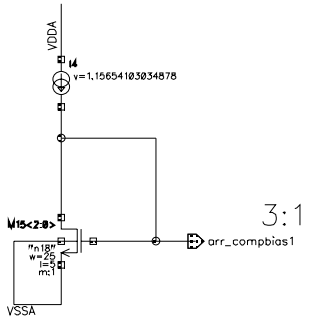
VSSA

Out SF



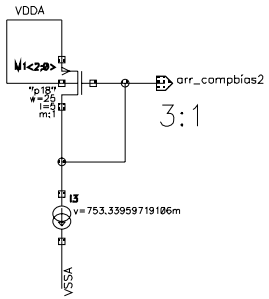
120uA

Comparator Bias



150u

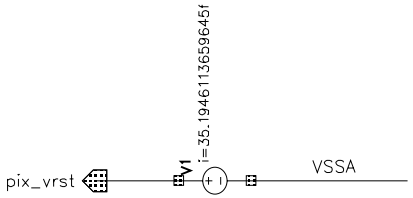
150u



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	pixbias_prsmpIRT_sim
Last QA Review	
Last Changed	Oct 18 15:09:53 2006

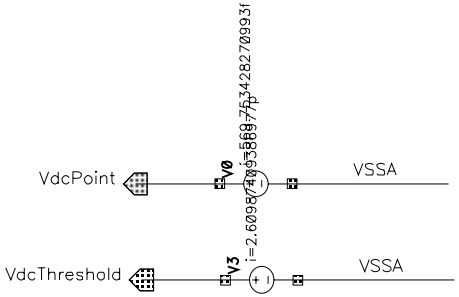
VSSA

Pixel reset point ~1v
for hard reset

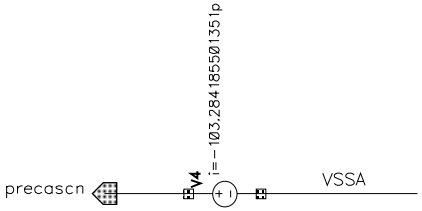


Vdcpoint = 1.Øv nom.

VdcThreshold = Vdcpoint – Vth (35mV nom)



Preamp cascode
voltage 1.5V nom.



RAL Microelectronics Group	
Project	Tera–Pixel APS for CALICE
Library Name	calice_feasability
Block Name	pixbias_voltages_RT
Last QA Review	
Last Changed	Oct 18 15:31:09 2006