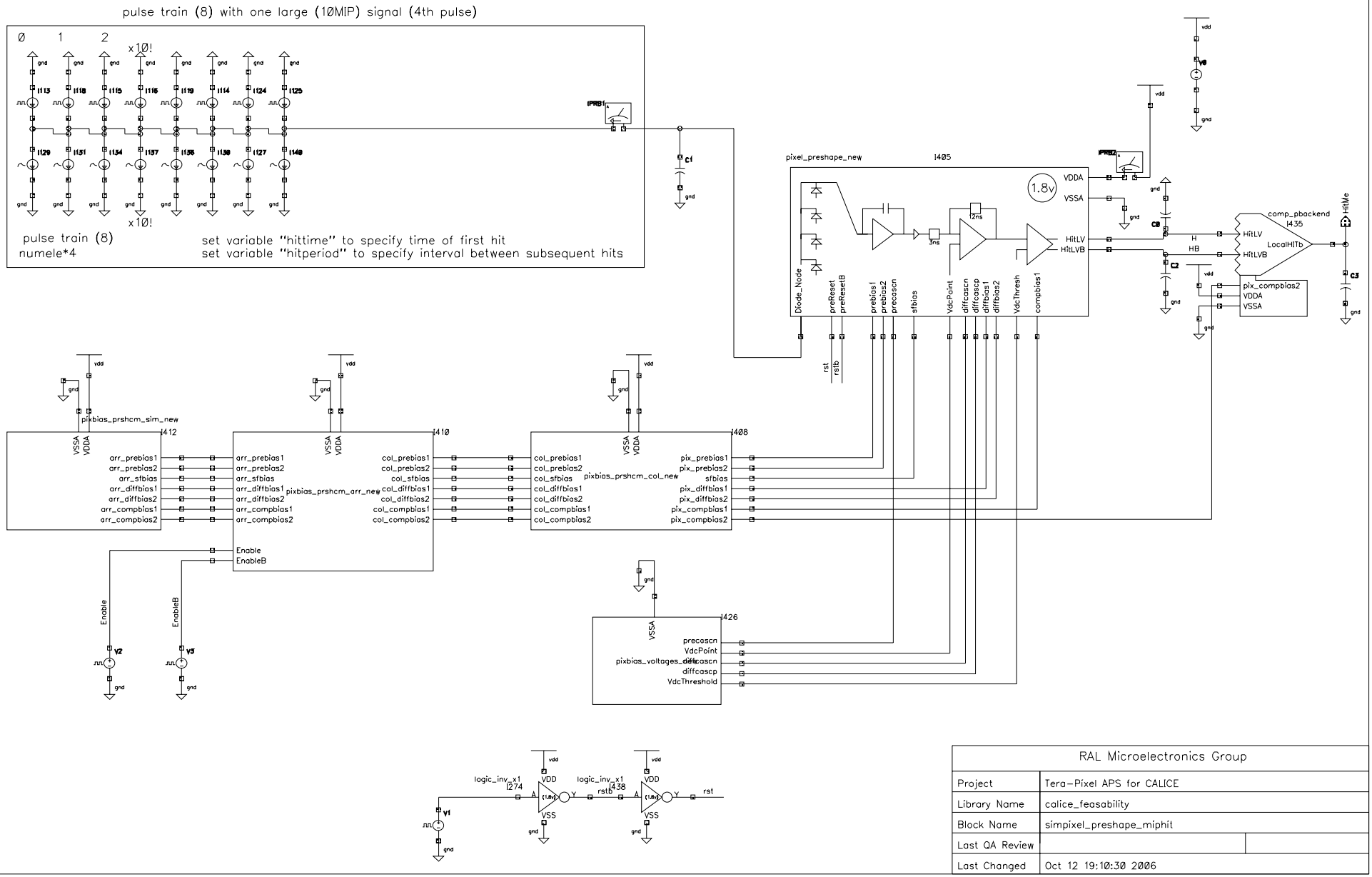
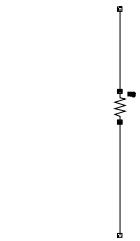

pulse train (8) with one large (10MIP) signal (4th pulse)
0 1 2
x10!
x10!
pulse train (8)
numele*4
set variable "hittime" to specify time of first hit
set variable "hitperiod" to specify interval between subsequent hits
pixel_preshape_new
1405
1.8v
VDDA
VSSA
HitLV
HitLVB
12ns
3ns
Diode_Node
preReset
preResetB
prebias1
prebias2
precascn
sfbias
VdcPoint
diffcascn
diffcascp
diffbias1
diffbias2
VdcThresh
compbias1
comp_pbackend
1435
LocalHITb
HitMe
pix_compbias2
H
HB
rst
rstb
pixbias_prshcm_sim_new
1412
arr_prebias1
arr_prebias2
arr_sfbias
arr_diffbias1
arr_diffbias2
arr_compbias1
arr_compbias2
pixbias_prshcm_arr_new
1410
col_prebias1
col_prebias2
col_sfbias
col_diffbias1
col_diffbias2
col_compbias1
col_compbias2
pixbias_prshcm_col_new
1408
pix_prebias1
pix_prebias2
sfbias
pix_diffbias1
pix_diffbias2
pix_compbias1
pix_compbias2
Enable
EnableB
1426
precascn
VdcPoint
diffcascn
diffcascp
VdcThreshold
logic_inv_x1
I274
logic_inv_x1
I438
rst0
rst
VDD
VSS
RAL Microelectronics Group
Project
Tera-Pixel APS for CALICE
Library Name
calice_feasability
Block Name
simpixel_preshape_miphit
Last QA Review
Last Changed
Oct 12 19:10:30 2006

Charge Preamp

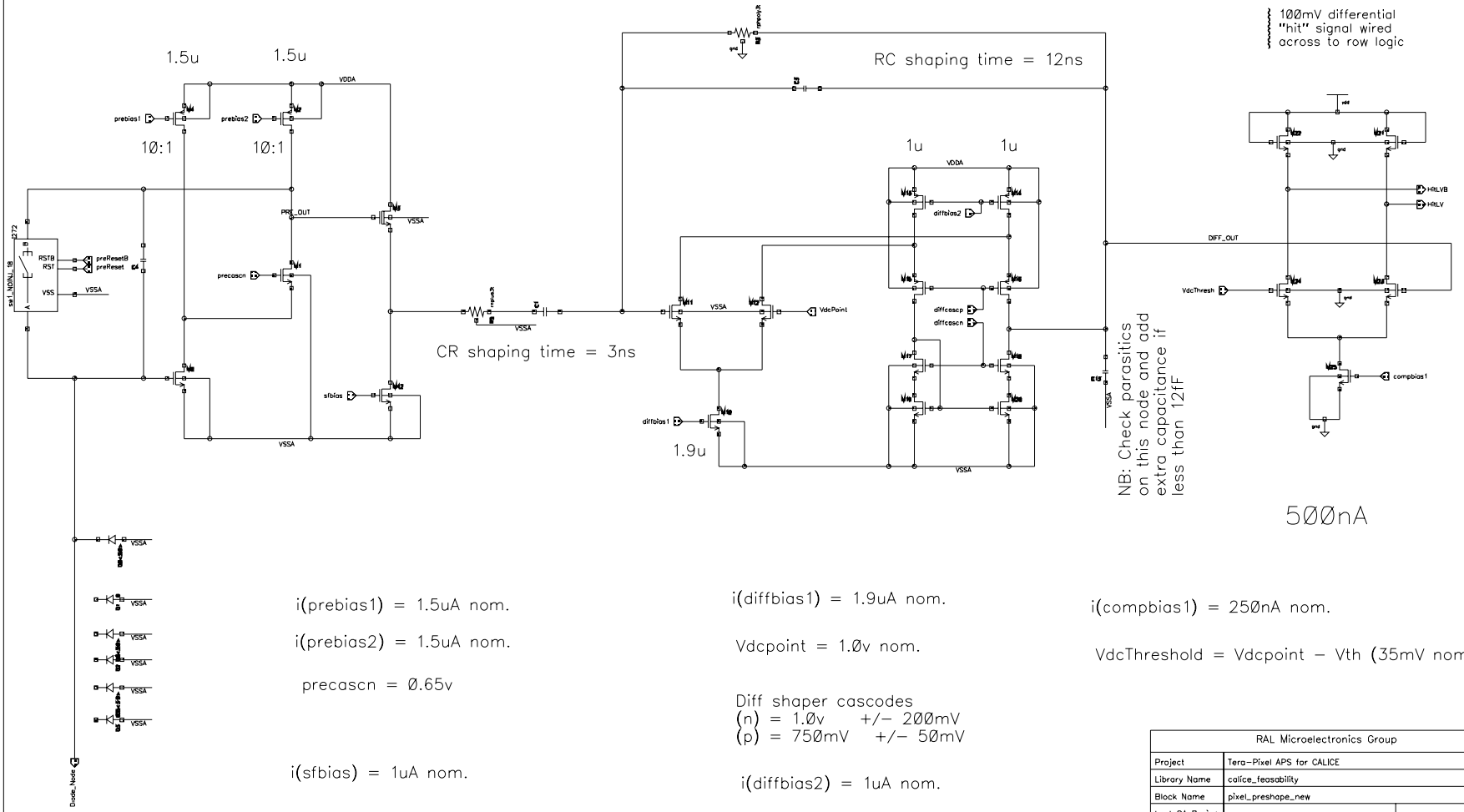
Source Follower

Differential Shaper

Comparator [NMOS–Half]



NB: Connect Rfb for noise analysis



i(prebias1) = 1.5uA nom.

i(prebias2) = 1.5uA nom.

precascn = Ø.65v

i(sfbias) = 1uA nom.

i(diffbias1) = 1.9uA nom.

Vdcpoint = 1.Øv nom.

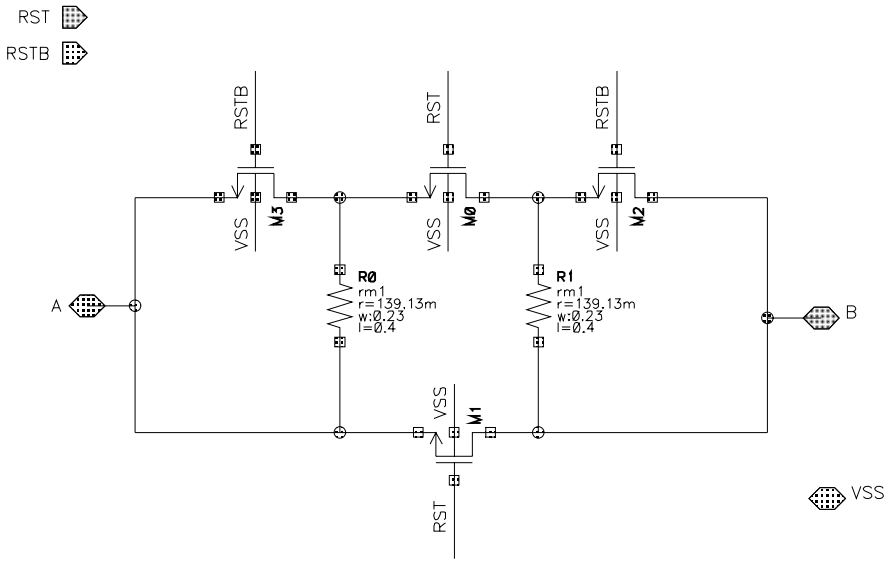
Diff shaper cascodes
(n) = 1.Øv +/– 2ØØmV
(p) = 75Ømv +/– 5Ømv

i(diffbias2) = 1uA nom.

i(compbias1) = 25Ønv nom.

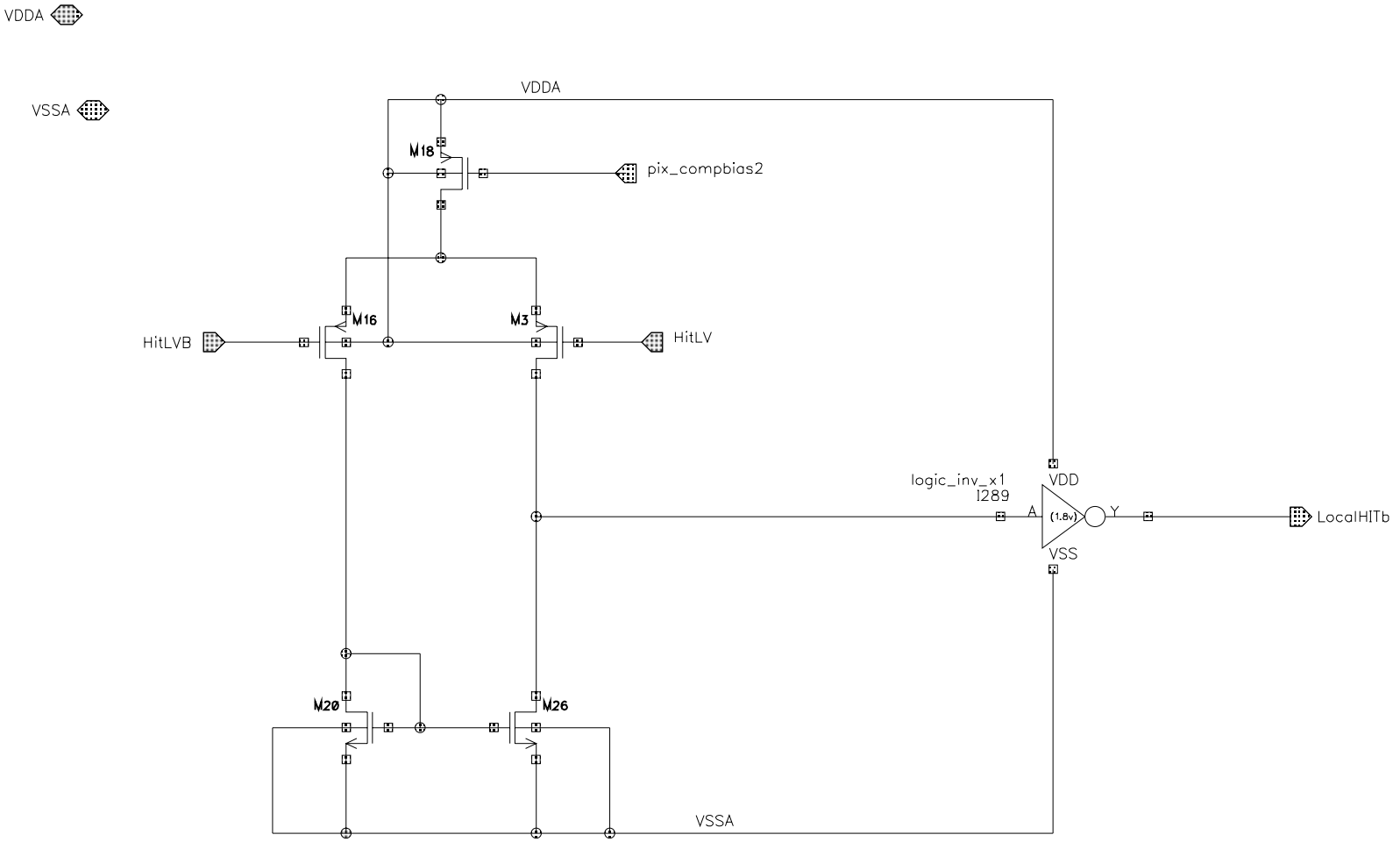
VdcThreshold = Vdcpoint – Vth (35mV nom)

RAL Microelectronics Group	
Project	Tera–Pixel APS for CALICE
Library Name	calice_feasability
Block Name	pixel_preshape_new
Last QA Review	
Last Changed	Oct 13 10:05:29 2006

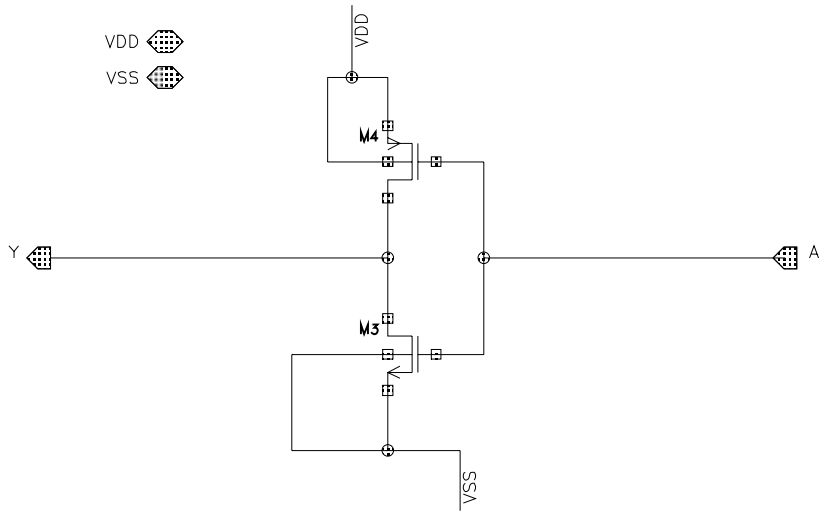


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	sw1_NOINJ_18
Last QA Review	
Last Changed	Oct 13 10:05:15 2006

250nA

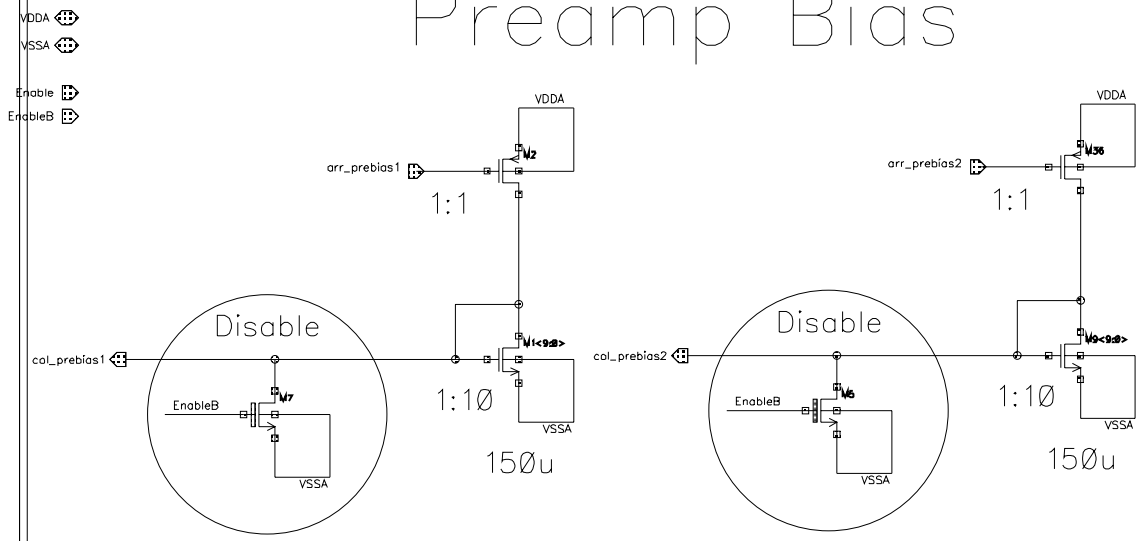


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	comp_pbackend
Last QA Review	
Last Changed	Oct 12 11:06:18 2006

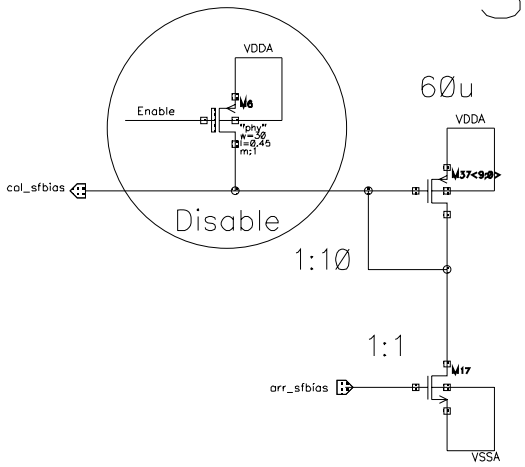


RAL Microelectronics Group	
Project	Tera–Pixel APS for CALICE
Library Name	calice_feasability
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Sep 28 11:46:11 2006

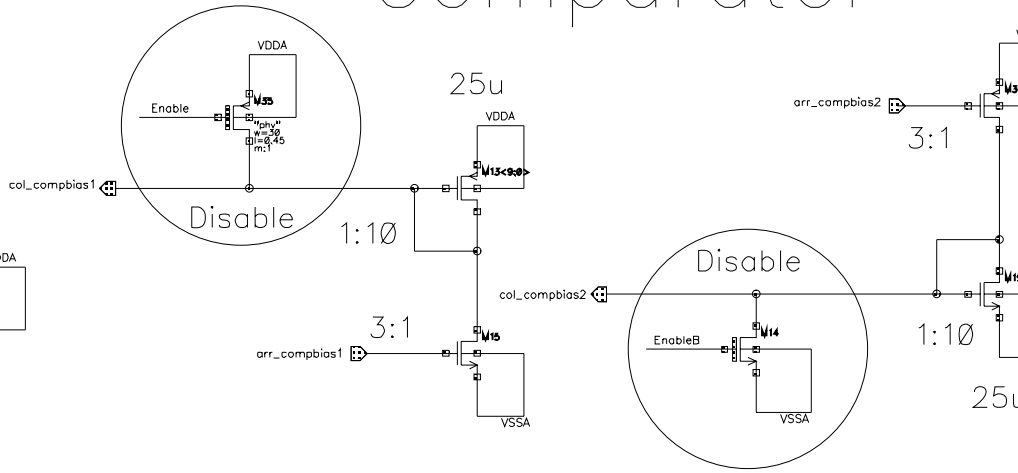
Preamp Bias



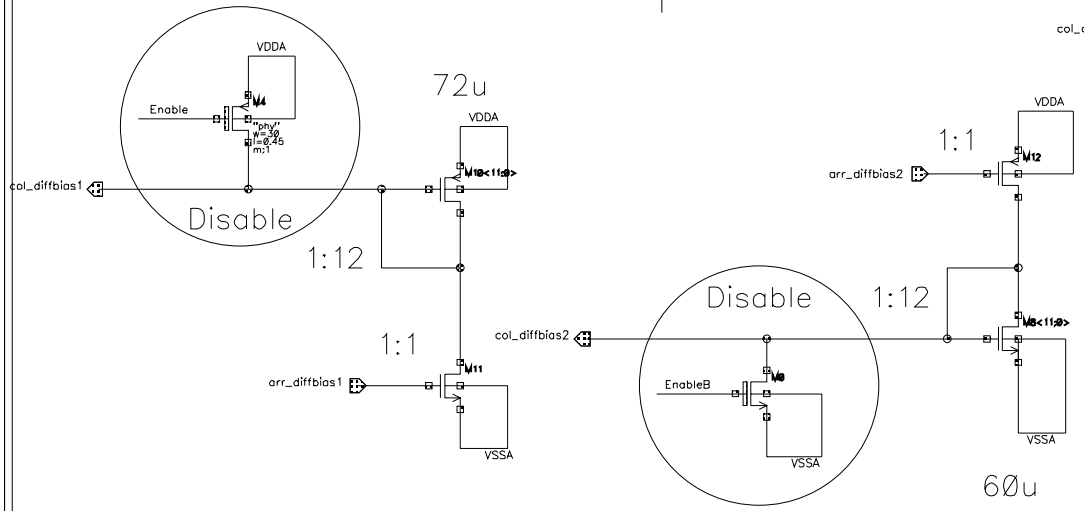
SF



Comparator



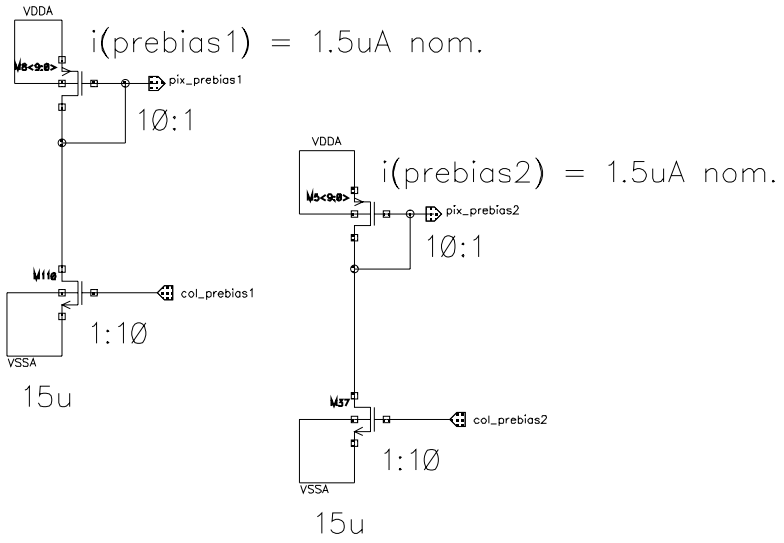
Diff Shaper Bias



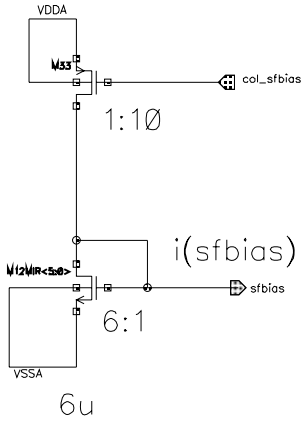
ARRAY CIRCUITS

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	pixbias_prshcm_arr_new
Last QA Review	
Last Changed	Oct 12 14:31:31 2006

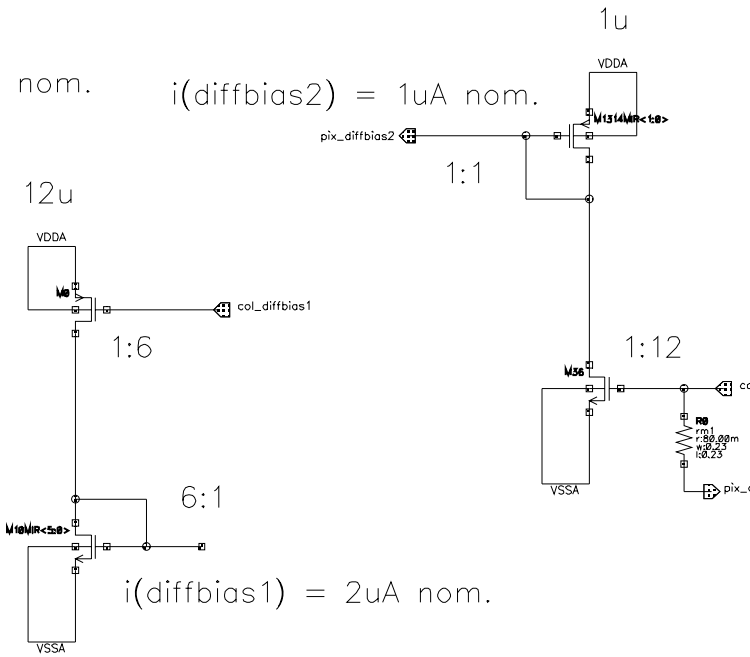
Preamp Bias



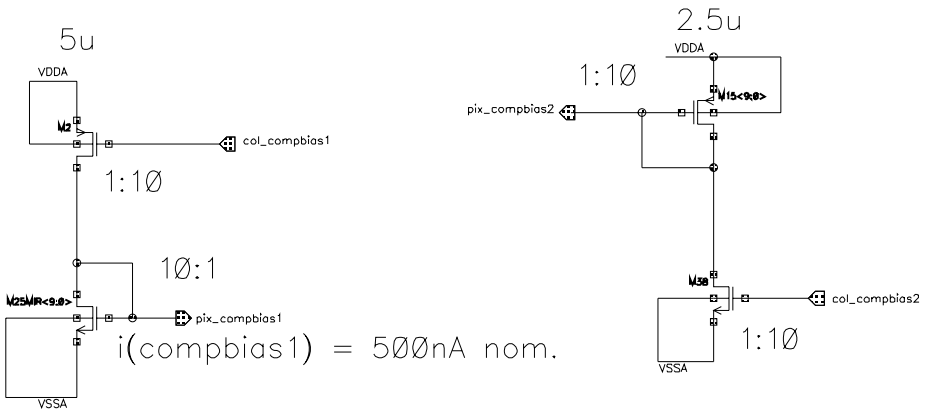
SF



Diff Shaper Bias



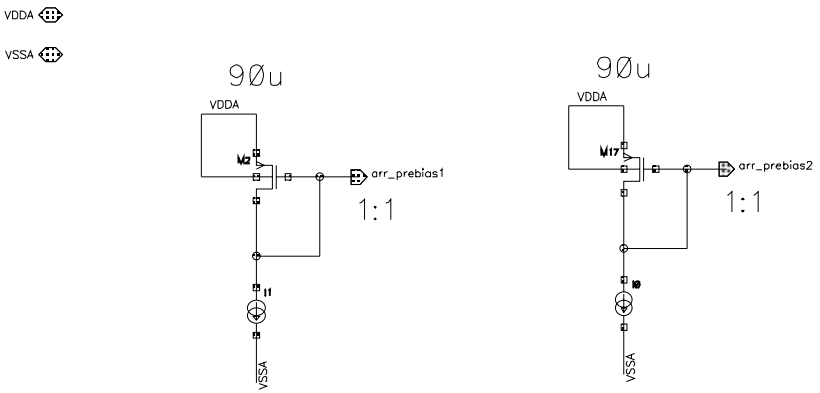
Comparator Bias



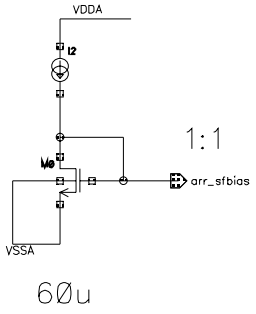
COLUMN CIRCUITS

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	pixbias_prshcm_col_new
Last QA Review	
Last Changed	Oct 12 14:32:53 2006

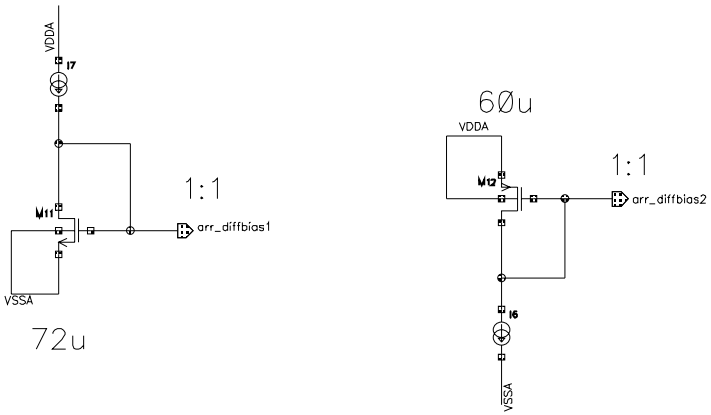
Preamp



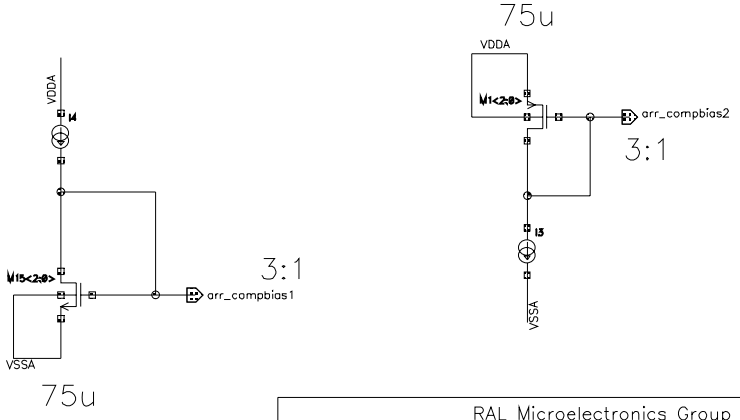
SF



Diff Shaper Bias



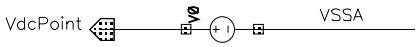
Comparator Bias



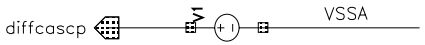
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	pixbias_prshcm_sim_new
Last QA Review	
Last Changed	Oct 12 13:39:59 2006

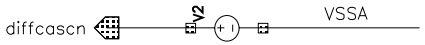
VSSA

Vdcpoint = 1.0v nom.

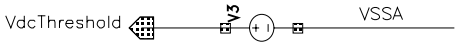


Diff shaper cascodes
(n) = 1.0v +/- 200mV
(p) = 750mV +/- 50mV

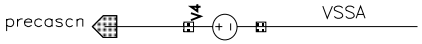




VdcThreshold = Vdcpoint - Vth (35mV nom)



Preamp cascode
voltage 0.65V nom.



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	pixbias_voltages_new
Last QA Review	
Last Changed	Oct 10 14:29:51 2006