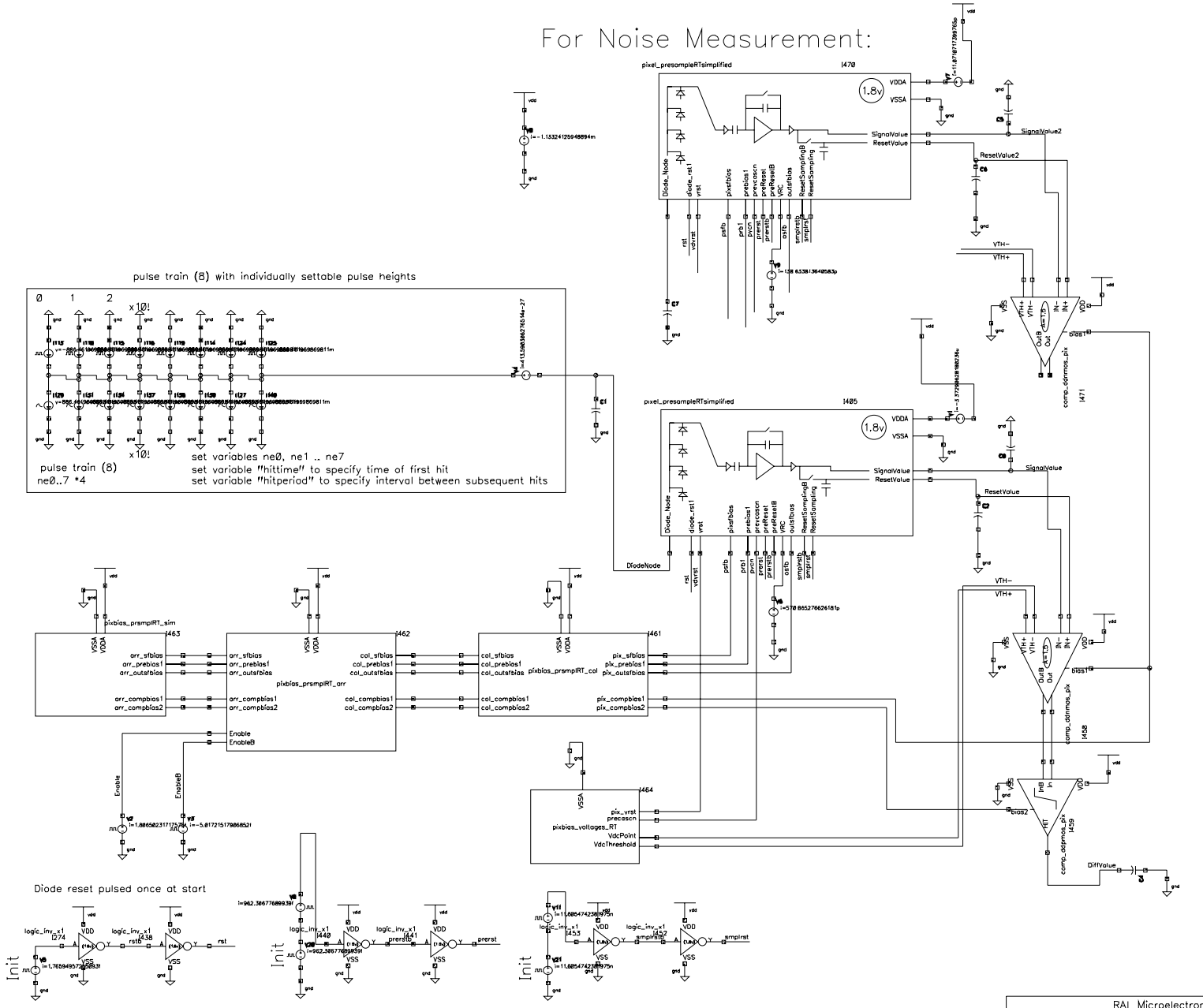
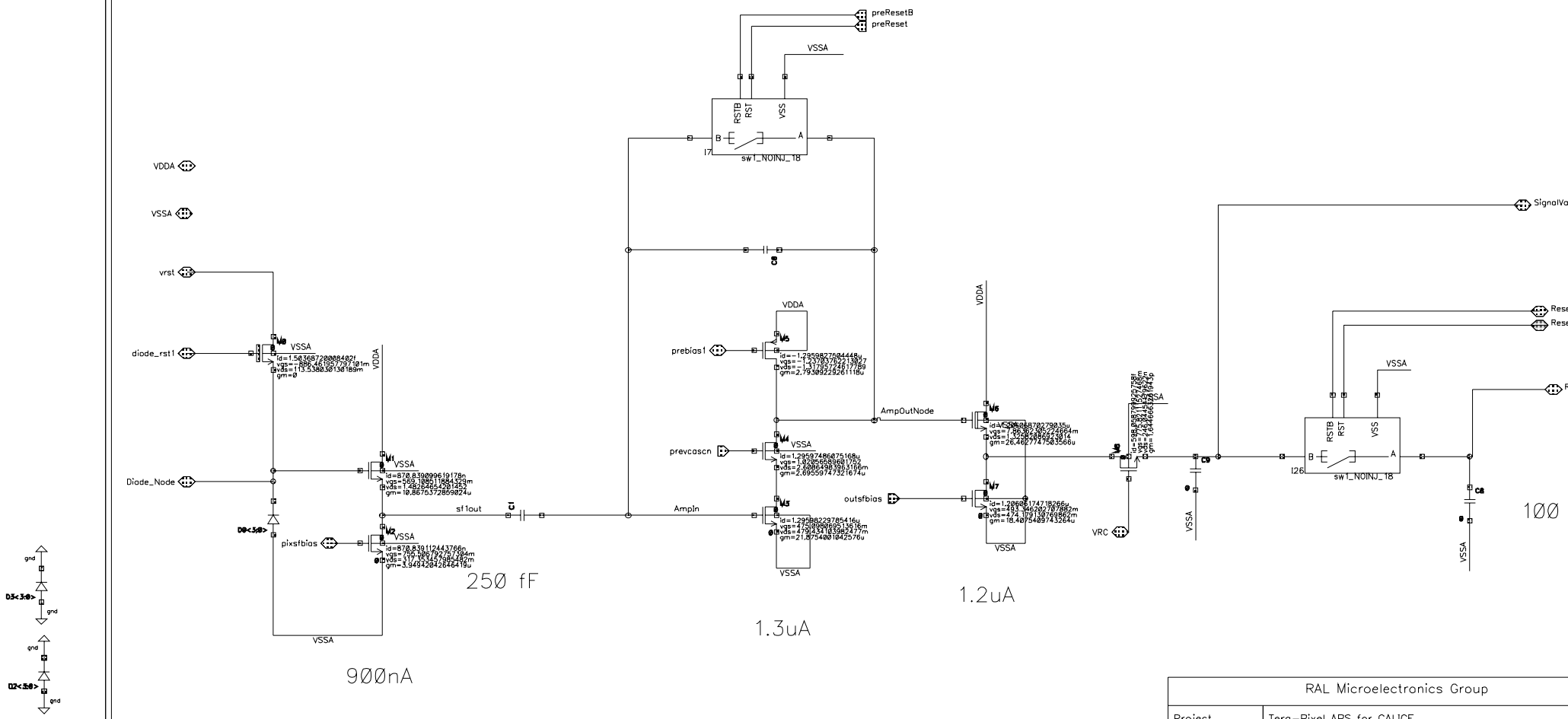

For Noise Measurement:
pixel_presampleRTsimplified
I470
I485
1.8v
VDDA
VSSA
SignalValue
ResetValue
SignalValue2
ResetValue2
pulse train (8) with individually settable pulse heights
pulse train (8)
ne0..7 *4
set variables ne0, ne1 .. ne7
set variable "hittime" to specify time of first hit
set variable "hitperiod" to specify interval between subsequent hits
DiodeNode
VTH+
VTH-
comp_ddnmos_pix
I471
I458
I459
pixbias_prsmpIRT_sim
I463
pixbias_prsmpIRT_arr
I462
pixbias_prsmpIRT_col
I461
I464
Enable
EnableB
Diode reset pulsed once at start
Init
logic_inv_x1
I274
I438
I440
I441
I453
I452
DiffValue
RAL Microelectronics Group
Project
Tera-Pixel APS for CALICE
Library Name
calice_circuits
Block Name
simpixel_presamplefilt_miphit
Last QA Review
Last Changed
Nov 15 11:50:10 2006

For Noise Analysis:
==========

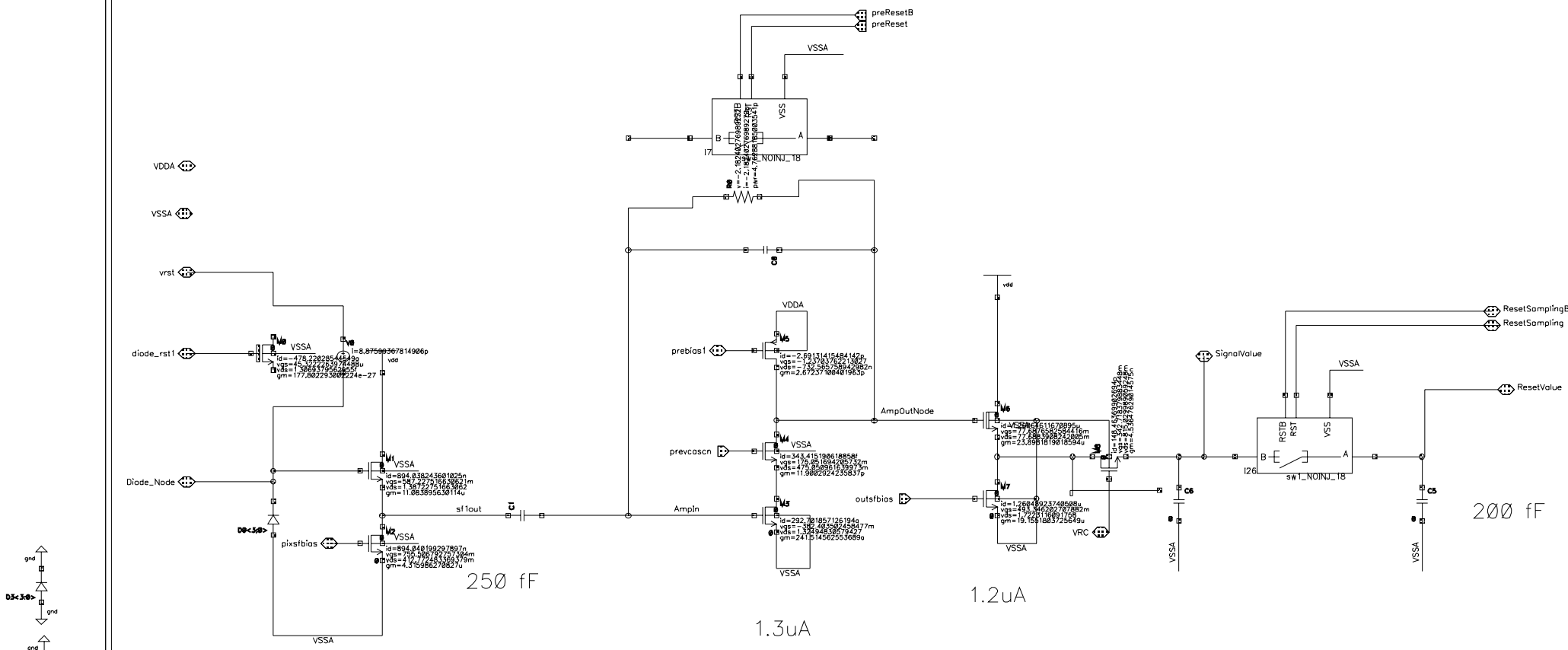
Drive diode with voltage source, not reset transistor
Replace shaper feedback switch with 1Tohm resistor
Disconnect current sources from diode node



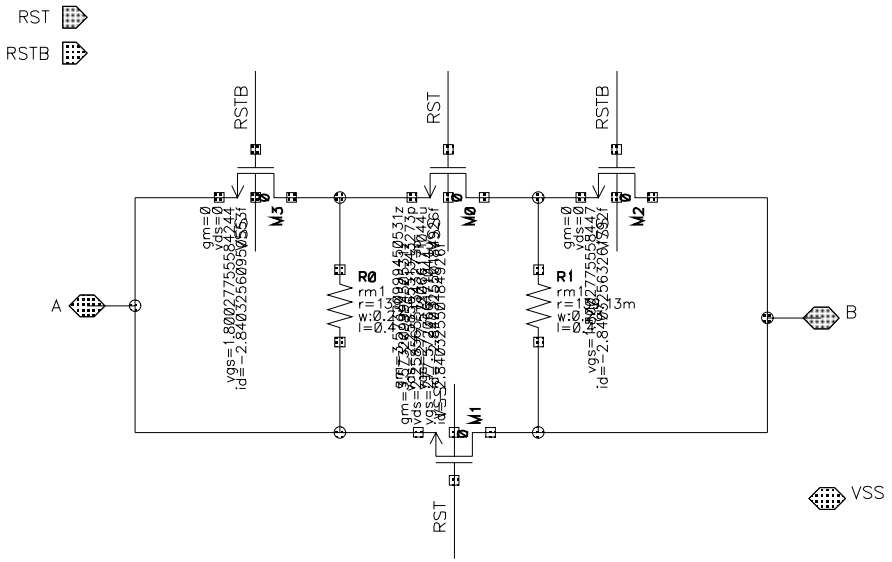
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_presampleRTsimplified_Filtered
Last QA Review	
Last Changed	Nov 15 11:00:36 2006

For Noise Analysis:
==========

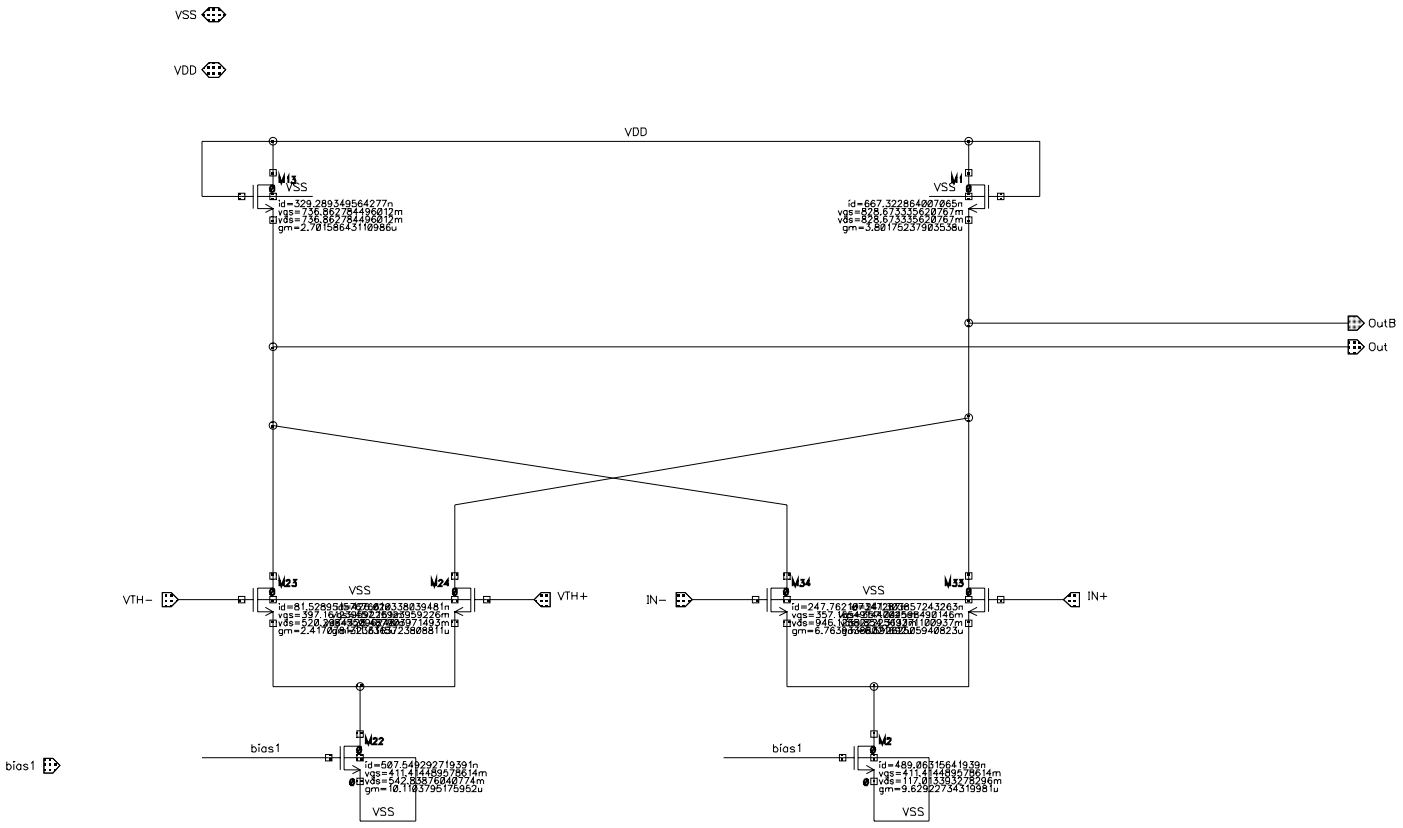
Drive diode with voltage source, not reset transistor
Replace shaper feedback switch with 1Tohm resistor
Disconnect current sources from diode node



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_presampleRTsimplified_Filtered2
Last QA Review	
Last Changed	Nov 15 10:45:27 2006



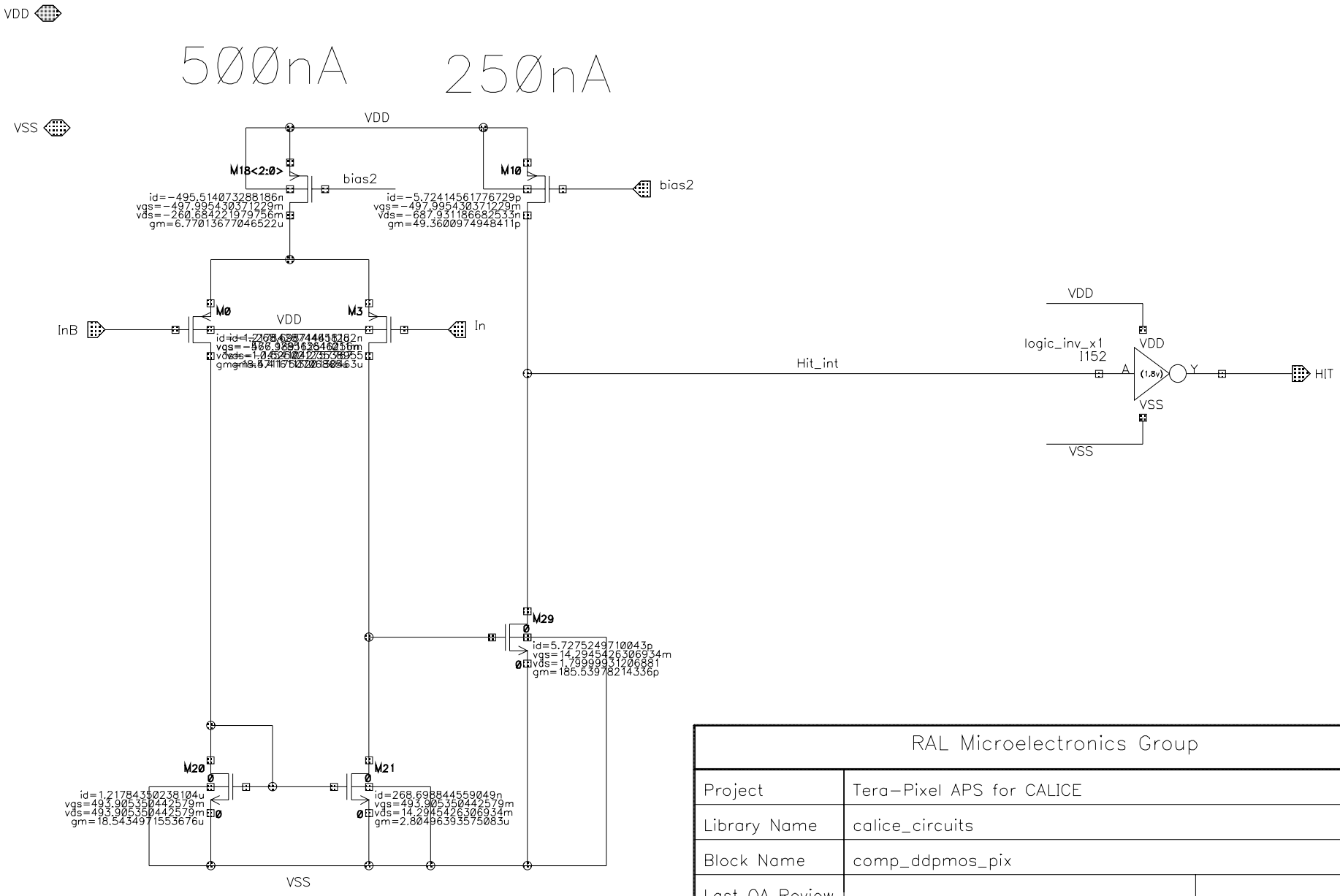
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	caliceRT
Block Name	sw1_NOINJ_18
Last QA Review	
Last Changed	Oct 13 10:05:15 2006



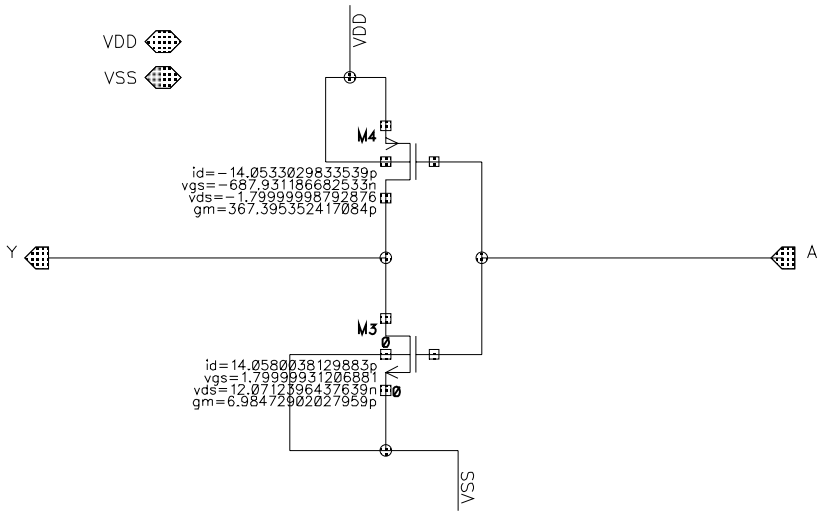
differential (10s of mV) hit signal wired across to pmos comparator at row logic

RAL Microelectronics Group	
Project	Tera−Pixel APS for CALICE
Library Name	calice_circuits
Block Name	comp_ddnmos_pix
Last QA Review	
Last Changed	Oct 17 09:27:22 2006

<<<<< AT ROW LOGIC >>>>>

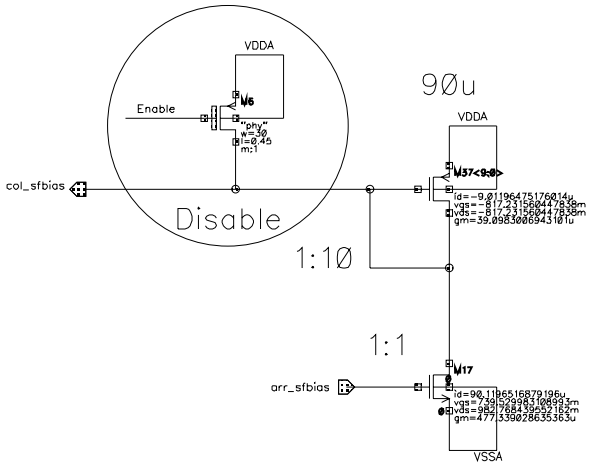


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	comp_ddpmos_pix
Last QA Review	
Last Changed	Oct 16 18:10:12 2006

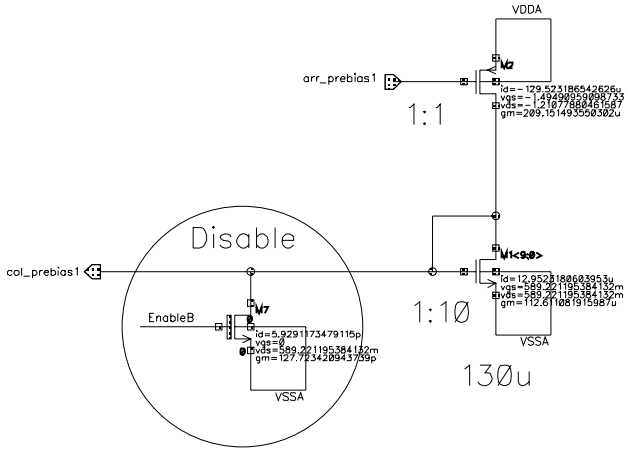


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Sep 28 11:46:11 2006

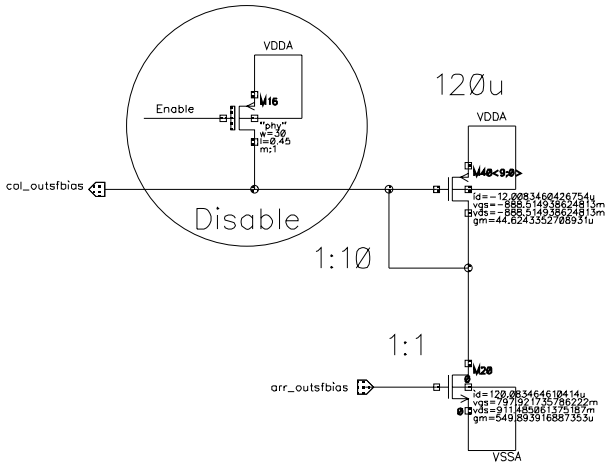
Pixel SF



Preamp Bias



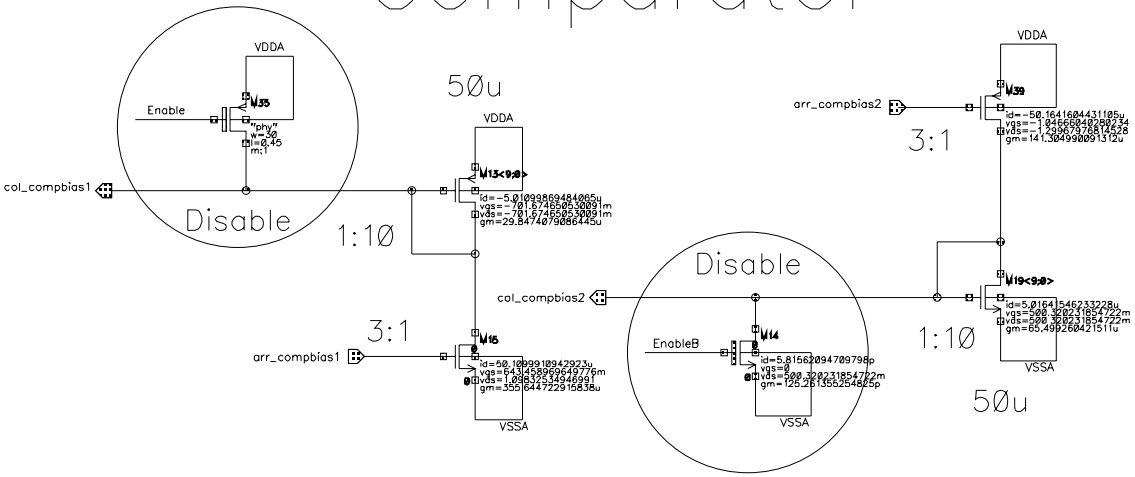
Out SF



VDDA
VSSA

Enable
EnableB

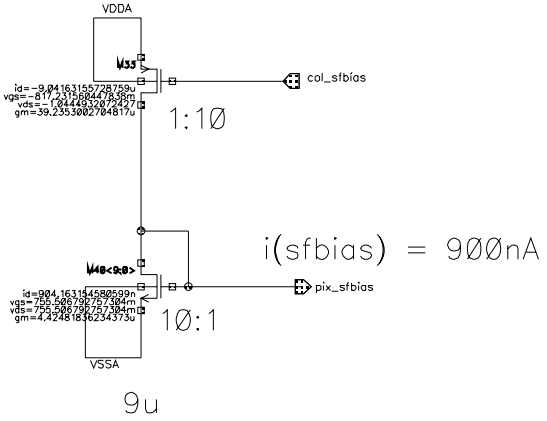
Comparator



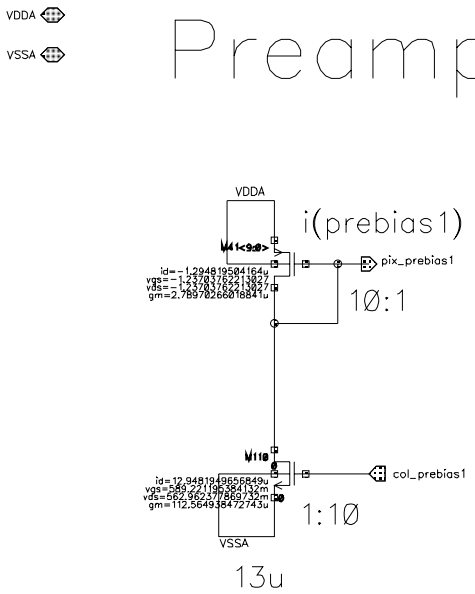
ARRAY CIRCUITS

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	pixbias_prsmpIRT_arr
Last QA Review	
Last Changed	Oct 18 14:29:36 2006

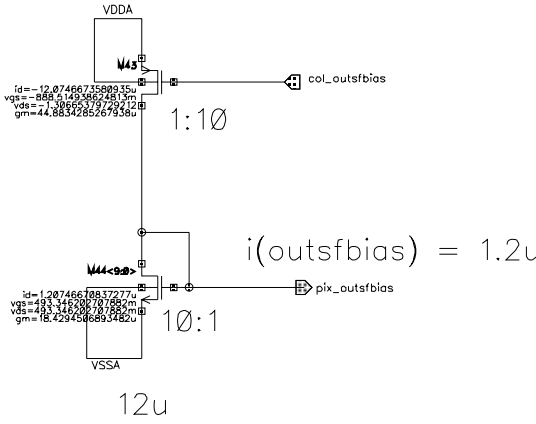
Pixel SF



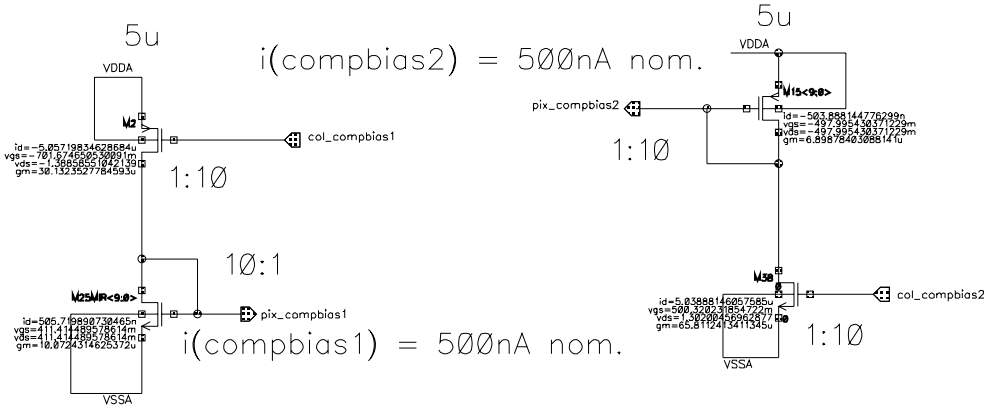
Preamp Bias



Out SF



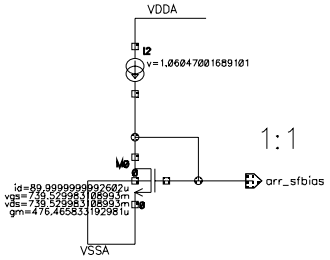
Comparator Bias



COLUMN CIRCUITS

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	pixbias_prsmpIRT_col
Last QA Review	
Last Changed	Oct 18 14:29:55 2006

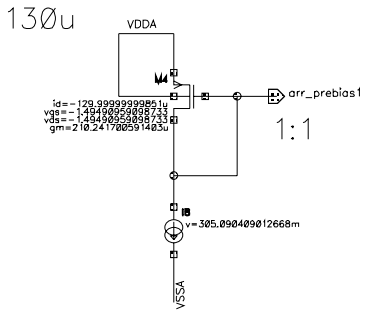
Pixel SF



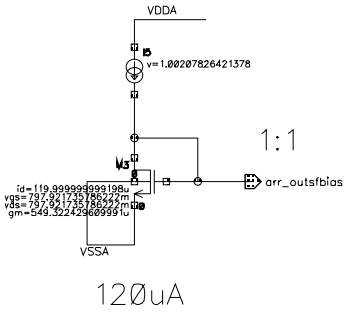
VDDA

VSSA

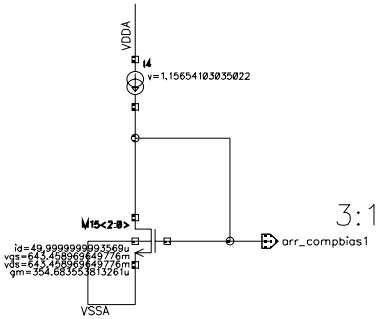
Preamp

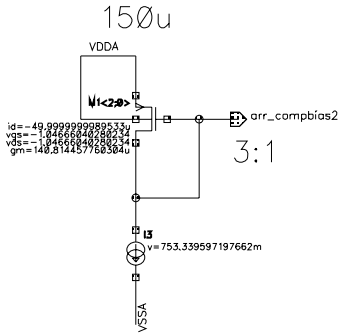


Out SF



Comparator Bias

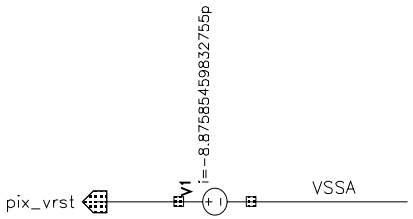




RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	pixbias_prsmpIRT_sim
Last QA Review	
Last Changed	Oct 18 15:09:53 2006

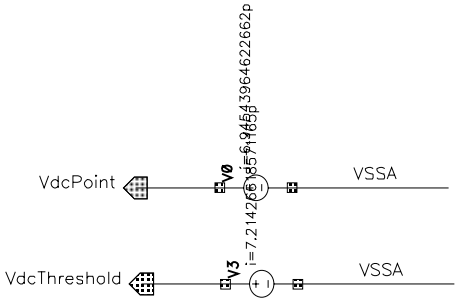
VSSA

Pixel reset point ~1v
for hard reset

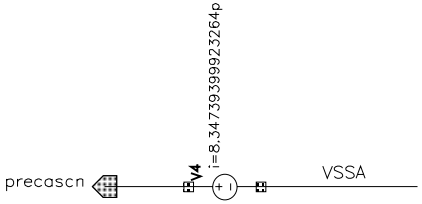


Vdcpoint = 1.Øv nom.

VdcThreshold = Vdcpoint – Vth (35mV nom)



Preamp cascode
voltage 1.5V nom.



RAL Microelectronics Group	
Project	Tera–Pixel APS for CALICE
Library Name	calice_feasability
Block Name	pixbias_voltages_RT
Last QA Review	
Last Changed	Oct 18 15:31:09 2006