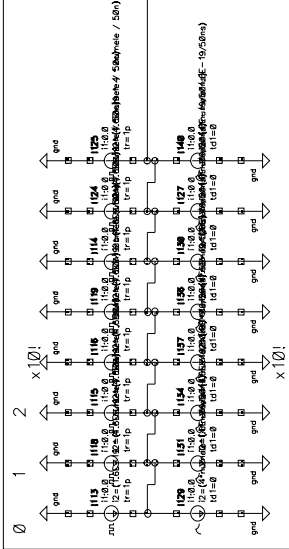
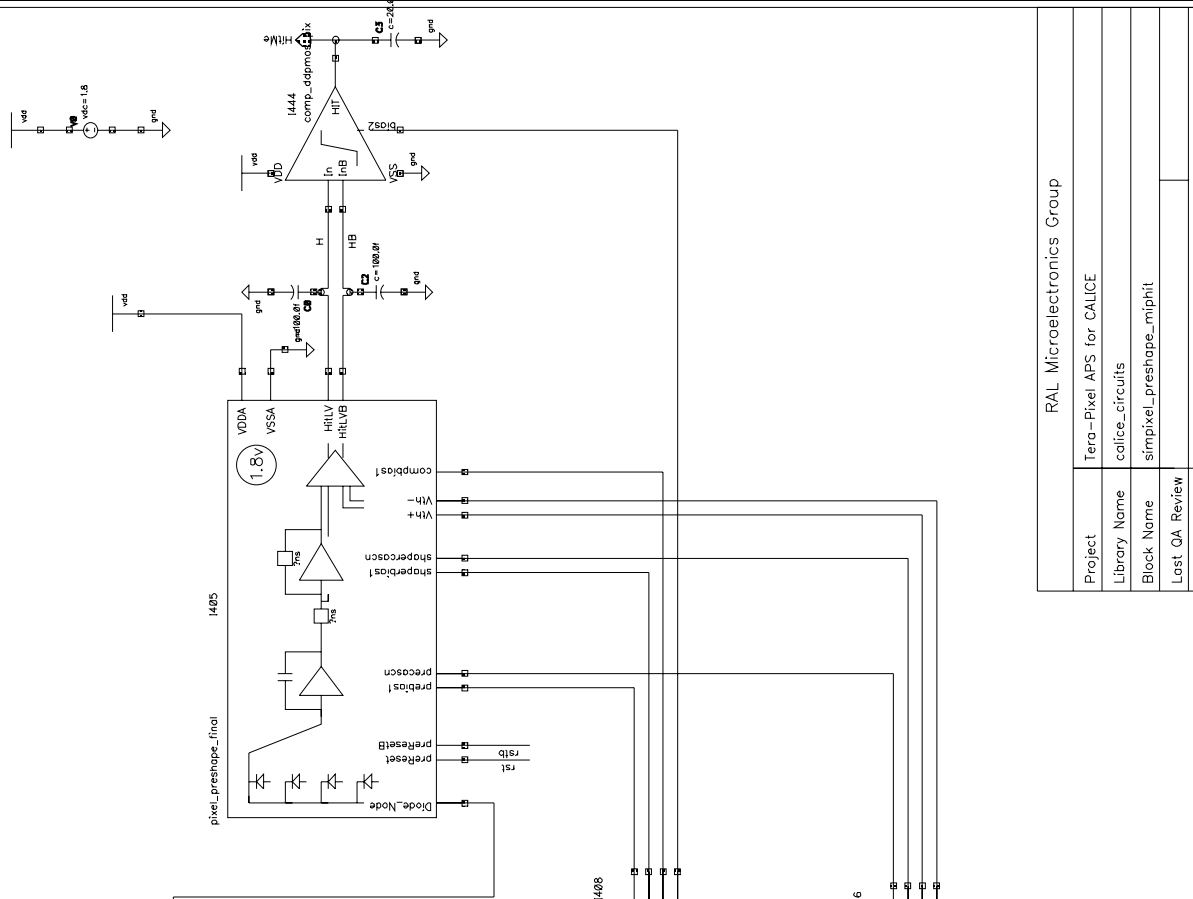


pulse train (8) with one large (10MIP) signal (4th pulse)

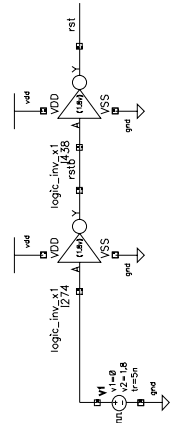


set variable "hittime" to specify time of first hit  
 set variable "hitperiod" to specify interval between subsequent hits

pulse train (8)  
 numele\*4



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	simplex1_preshape_miphit
Last QA Review	
Last Changed	Nov 6 17:33:29 2006

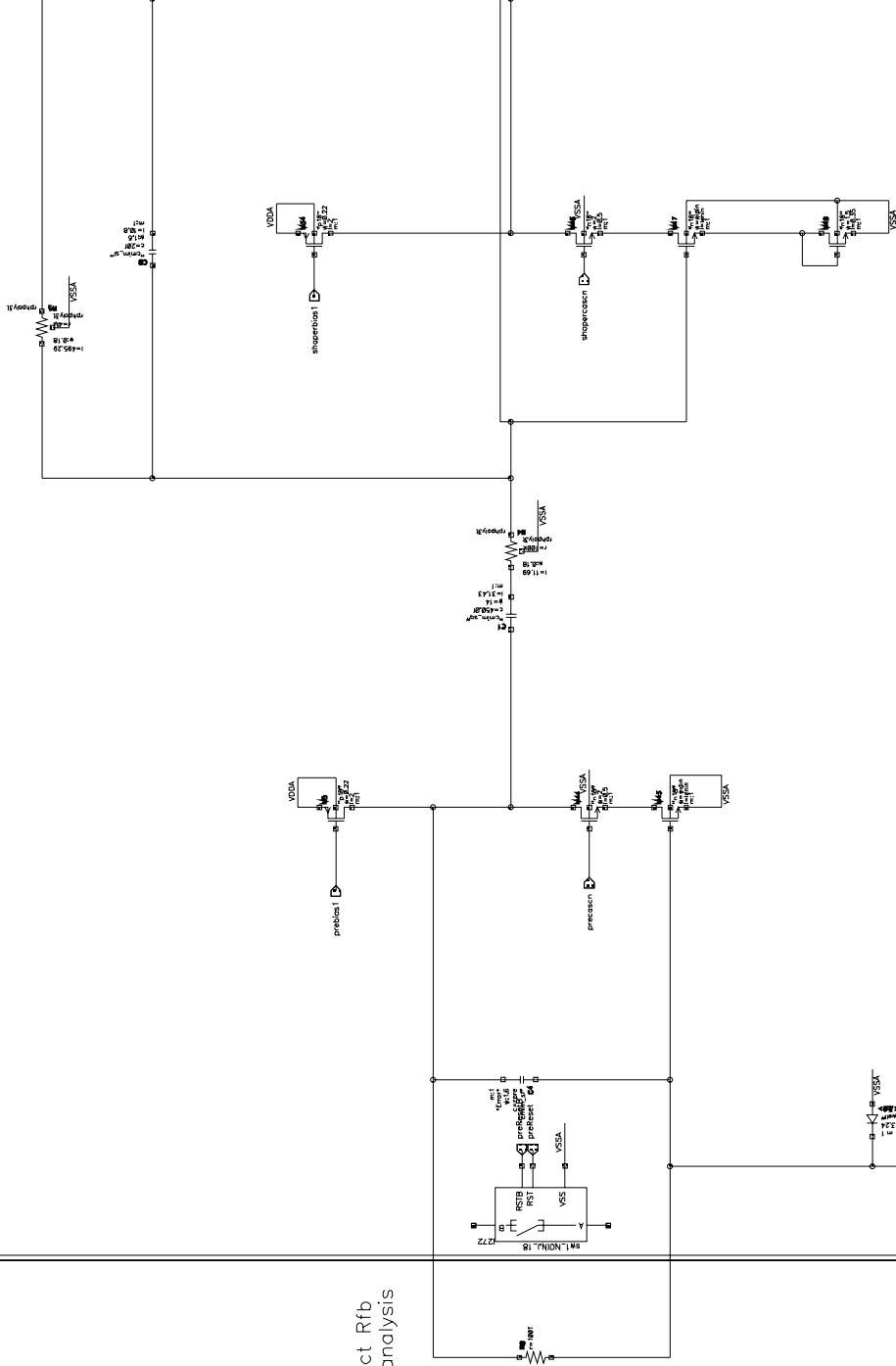


# Charge Preamp

# Comparator [NMOS-Half]

VDDA

VSSA



100mV differential "hit" signal wired across to row logic

NB: Connect Rfb for noise analysis

$i(\text{prebias1}) = 1.5\mu\text{A nom.}$

$i(\text{shaperbias1}) = 1.5\mu\text{A nom.}$

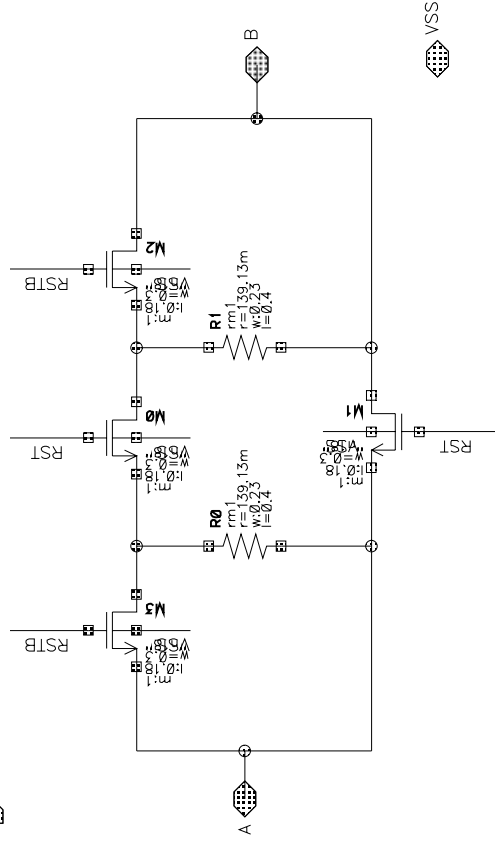
$i(\text{compbias1}) = 250\text{nA nom.}$

$\text{precascn} = 1.5\text{v}$

$\text{shapercascn} = 1.5\text{v}$

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixel_freshape_final
Last CA Review	
Last Changed	Nov. 6 17:33:15, 2006

RST  
RSTB



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Project Tera-Pixel APS for CALICE

Library Name calice\_circuits

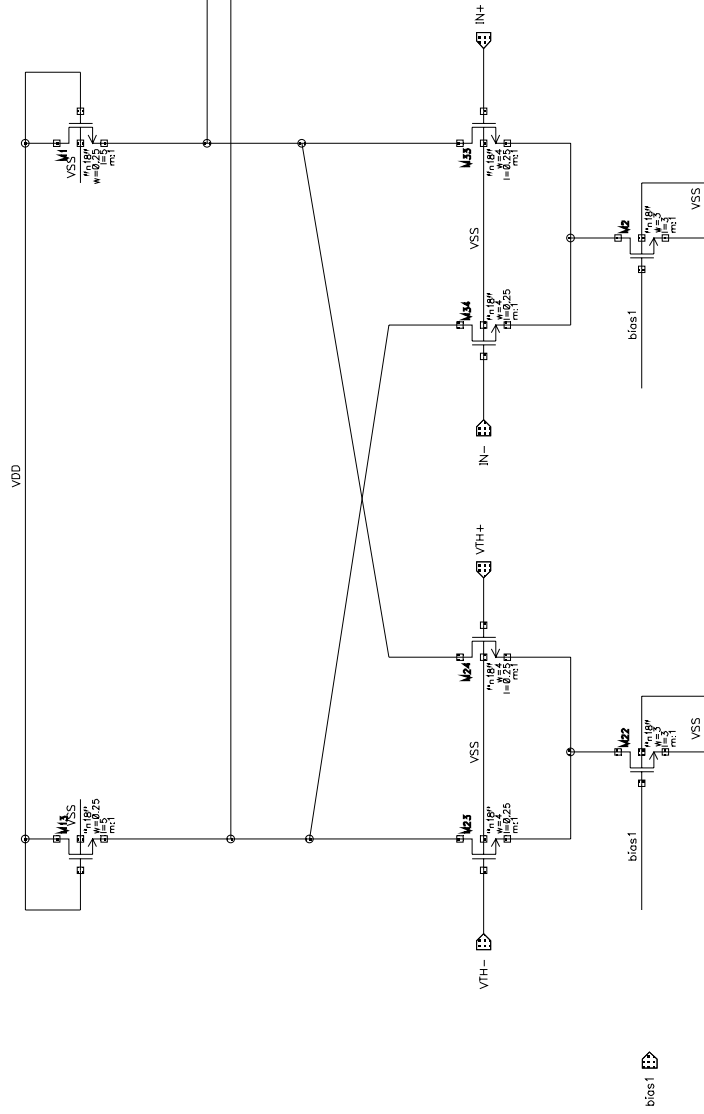
Block Name sw1\_NOINJ\_18

Last QA Review

Last Changed Oct 13 10:05:15 2006

VSS

VDD



differential (10s of mV)  
 hit signal wired across  
 to\_pmos comparator at r  
 logic

250nA

250nA

RAL Microelectronics Group

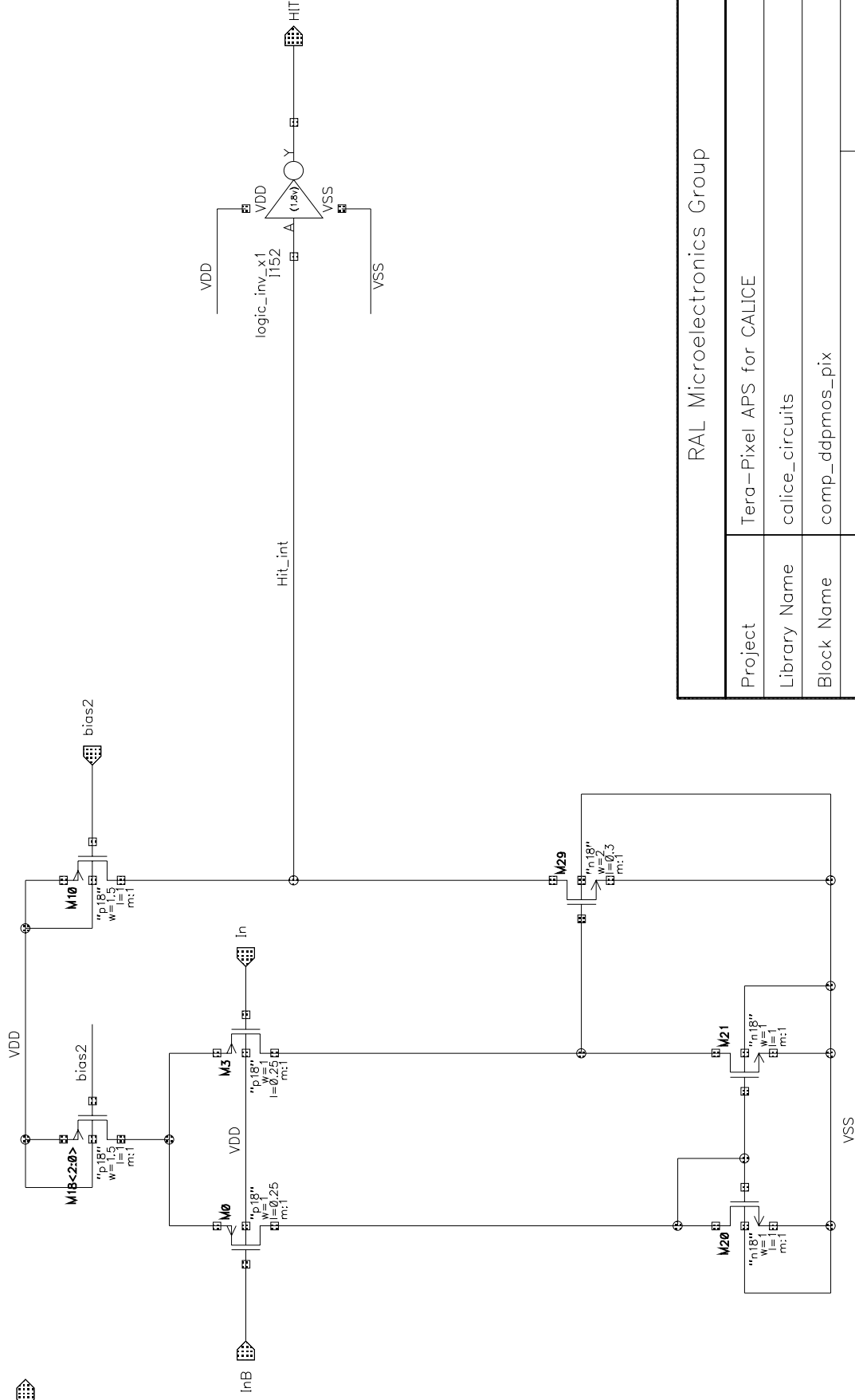
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	comp_ddmos_pix
Last QA Review	
Last Changed	Oct 17 09:27:22 2006

<<<<< AT ROW LOGIC >>>>>

VDD

VSS

500nA 250nA



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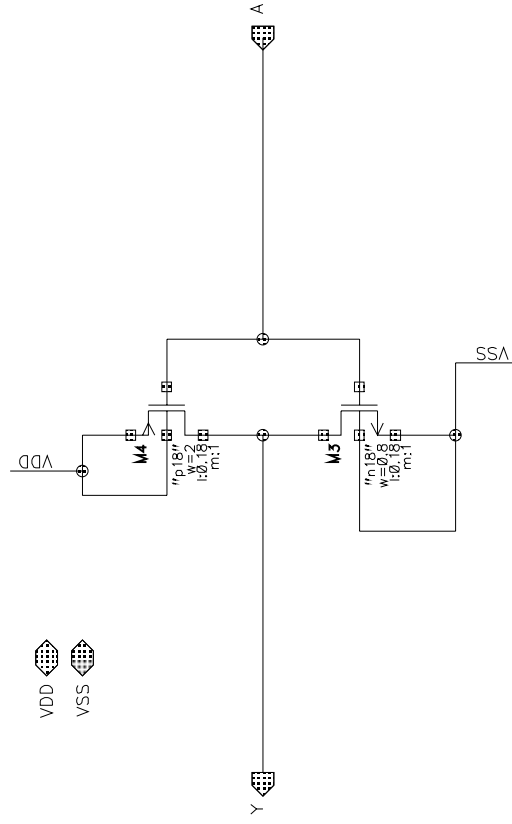
Project Tera-Pixel APS for CALICE

Library Name calice\_circuits

Block Name comp\_ddpmos\_pix

Last QA Review

Last Changed Oct 16 18:10:12 2006

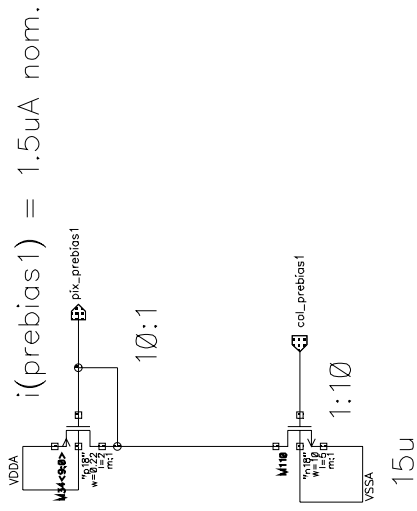


RAL Microelectronics Group

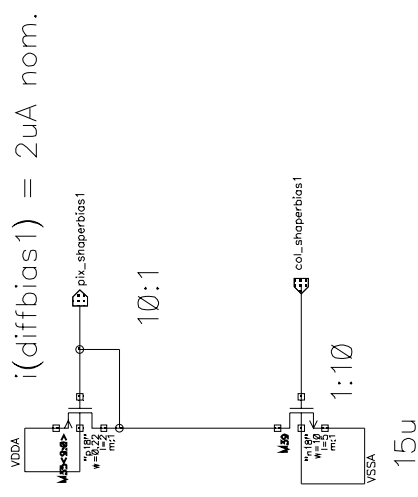
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Sep 28 11:46:11 2006

# Preamp Bias

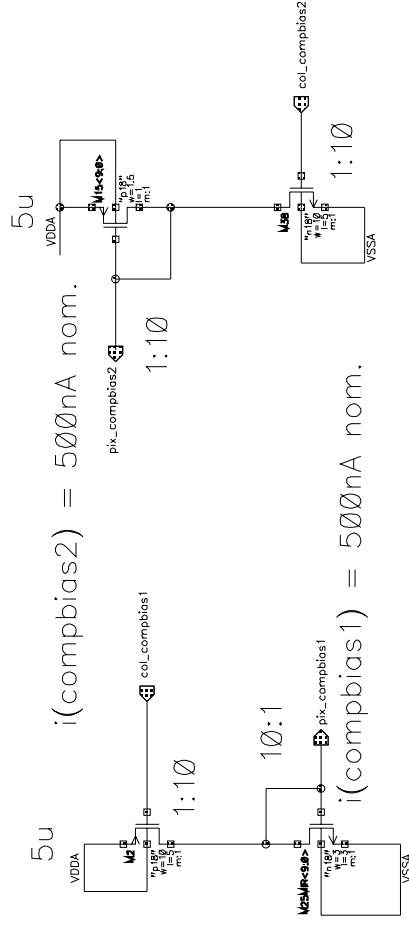
VDDA  
VSSA



# Shaper Bias



# Comparator Bias



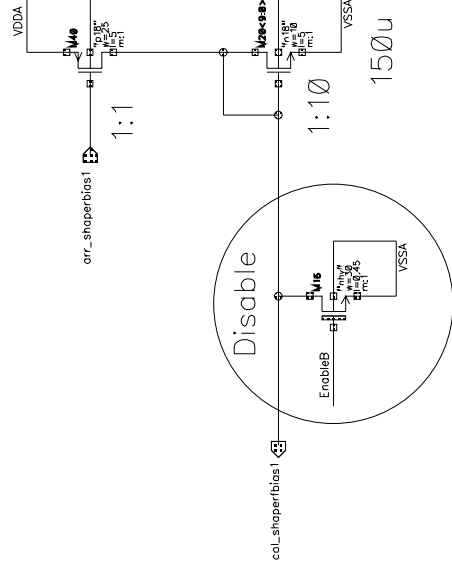
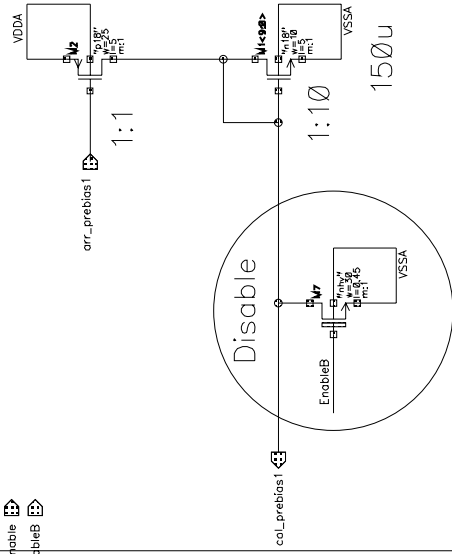
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixbias_prishcm_col_final
Last QA Review	
Last Changed	Oct 27 14:03:52 2006

# COLUMN CIRCUITS

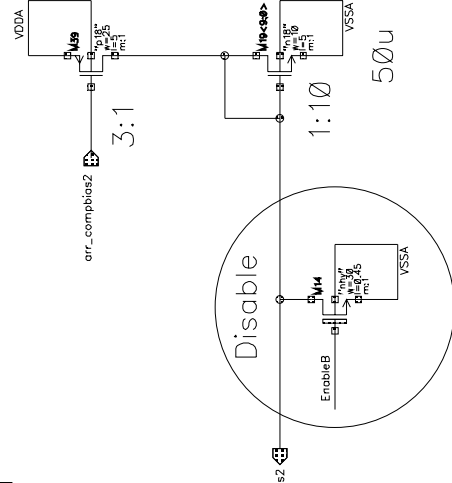
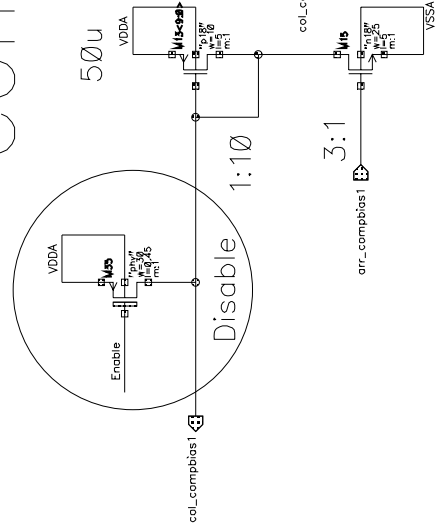
# Preamp Bias

# Shaper Bias

VDDA  
 VSSA  
 Enable  
 EnableB



# Comparator



# ARRAY CIRCUITS

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixbias_prshcm_arr_final
Last QA Review	
Last Changed	Oct 27 14:17:16 2006

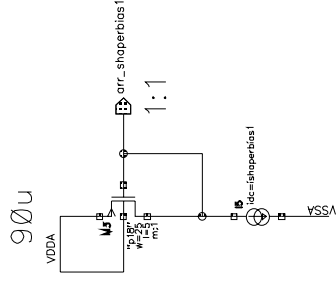
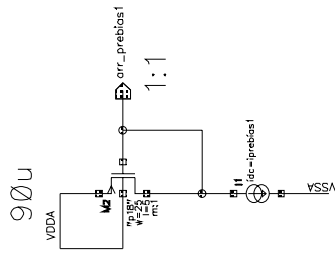


# Preamp

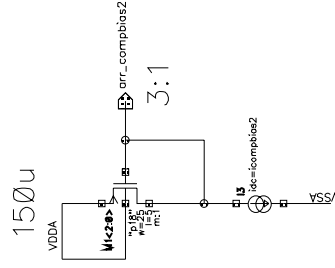
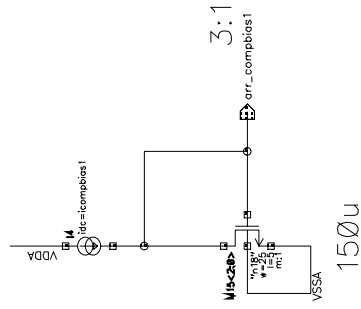
# Shaper Bias

VDDA

VSSA



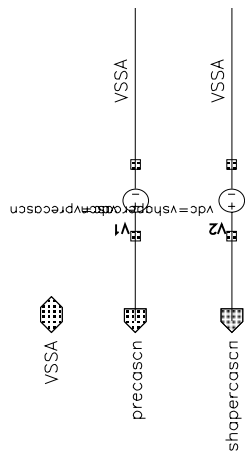
# Comparator Bias



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixbias_prshcm_sim_final
Last QA Review	
Last Changed	Oct 27 14:25:26 2006

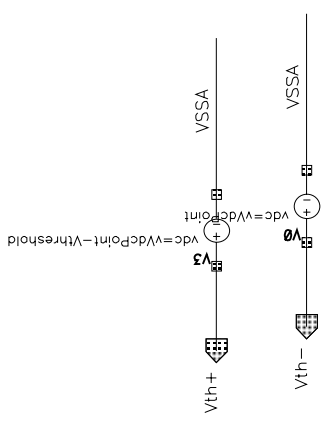
preamp cascode

shaper cascode



$$V_{th+} = V_{dcpoint} + V_{th}$$

$$V_{th-} = V_{dcpoint} - 1.0v \text{ nom.}$$



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixbias_voltages_final
Last QA Review	
Last Changed	Oct 27 14:12:14 2006