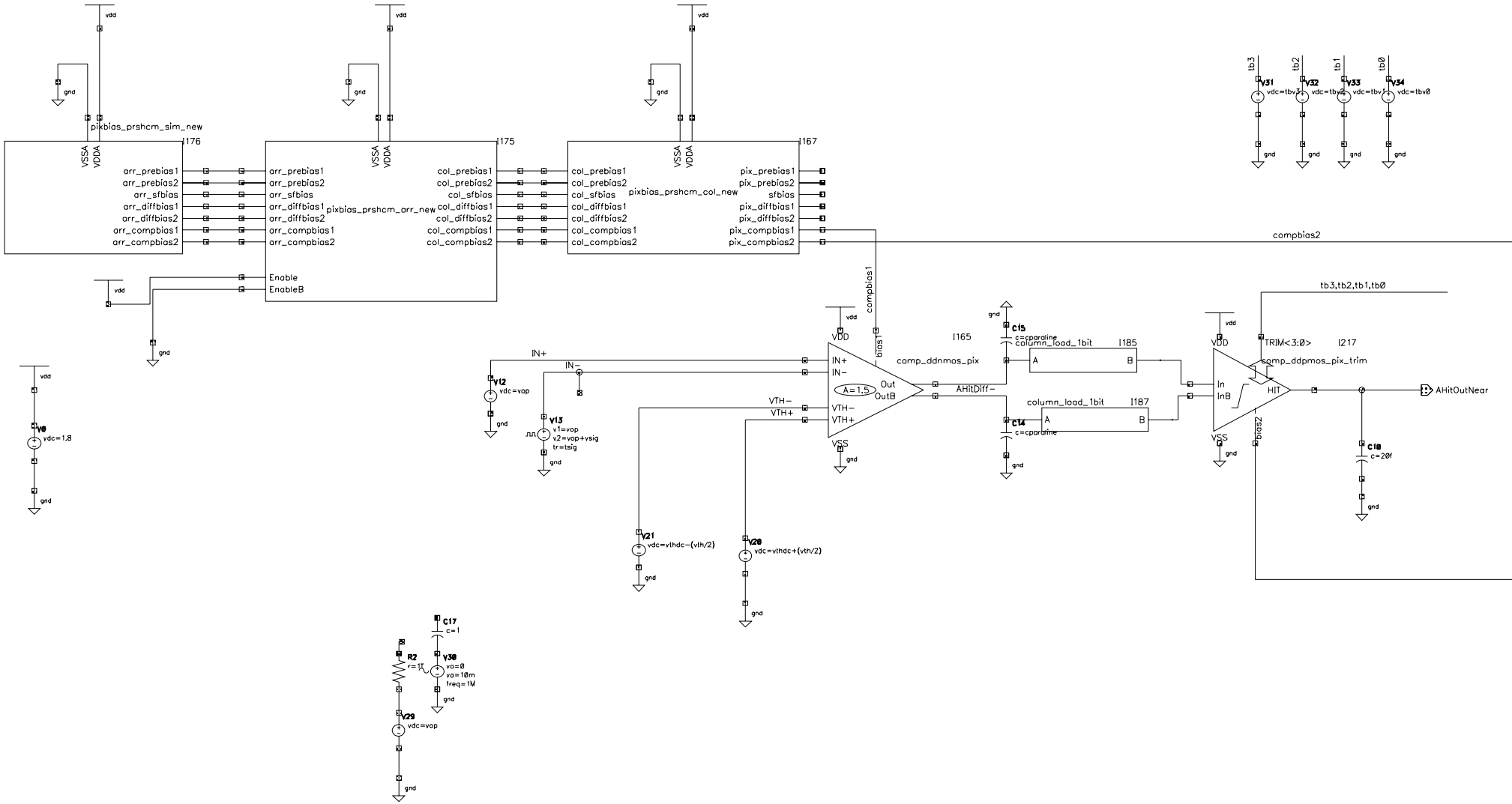
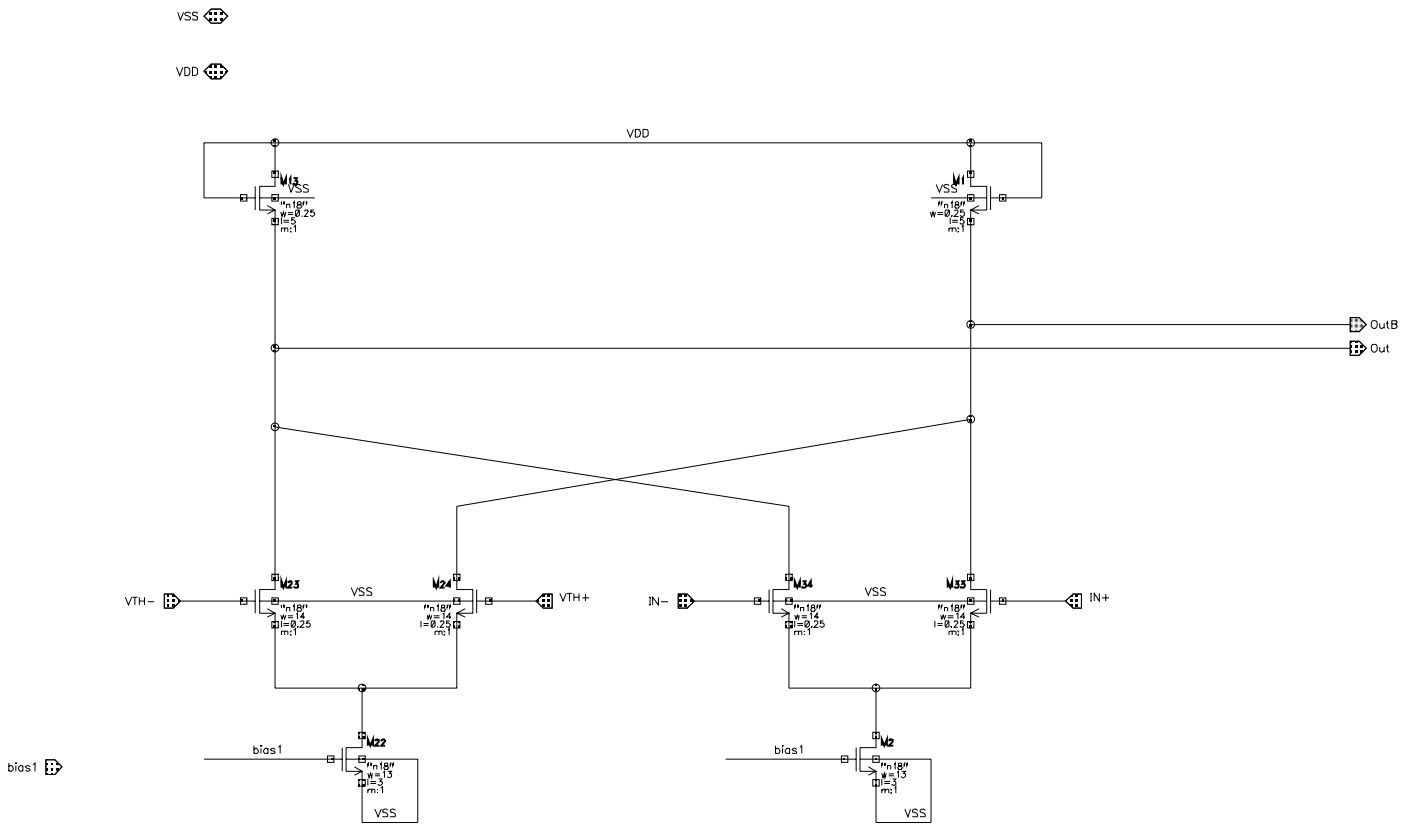


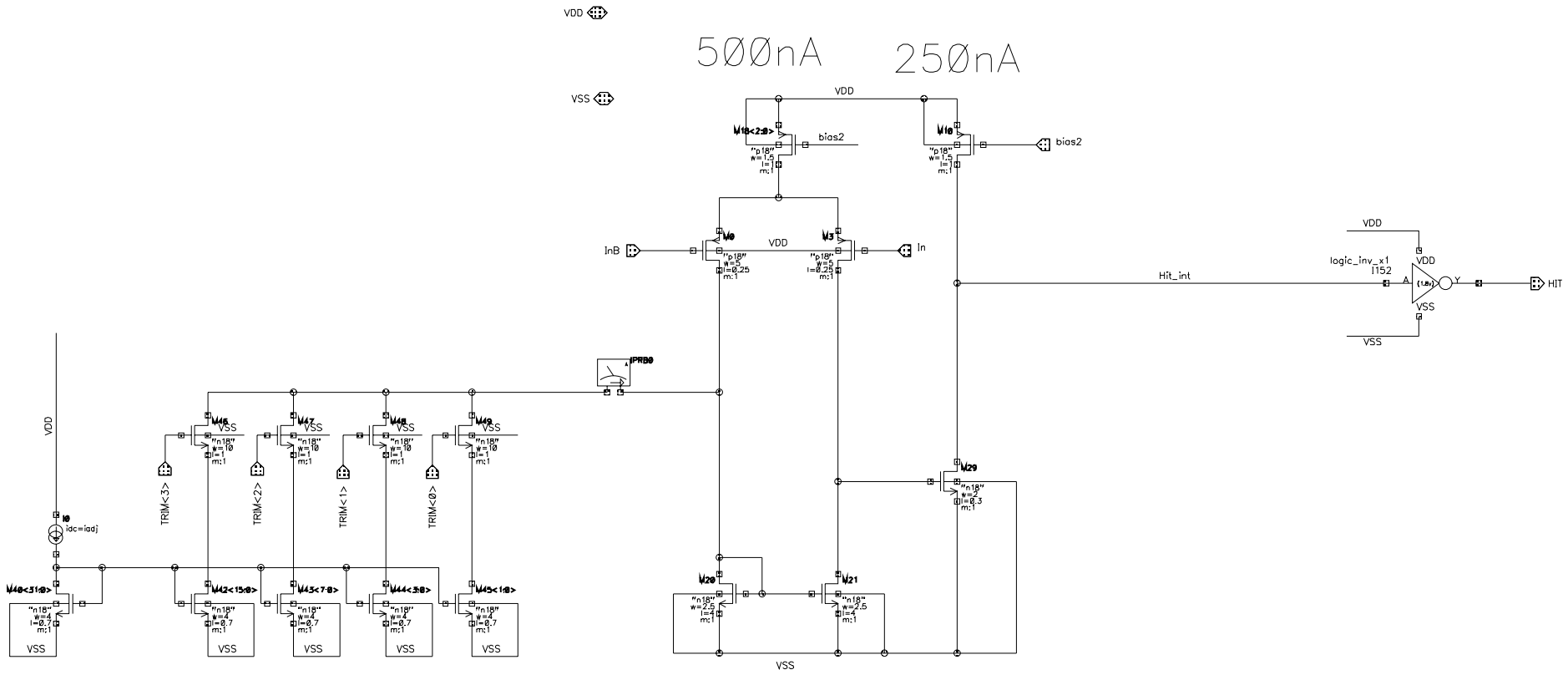
RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	sim_comp_doublediff3
Last QA Review	
Last Changed	Nov 30 10:17:18 2006



differential (10s of mV)
hit signal wired across
to pmos comparator at rov
logic

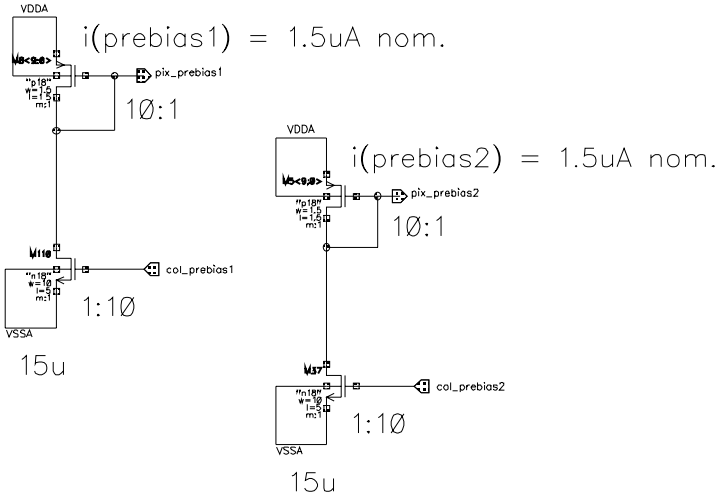
RAL Microelectronics Group	
Project	Tera−Pixel APS for CALICE
Library Name	calice_circuits
Block Name	comp_ddnmos_pix
Last QA Review	
Last Changed	Nov 24 11:27:15 2006

<<<<< AT ROW LOGIC >>>>>



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	comp_ddpmos_pix_trim
Last QA Review	
Last Changed	Nov 28 16:06:25 2006

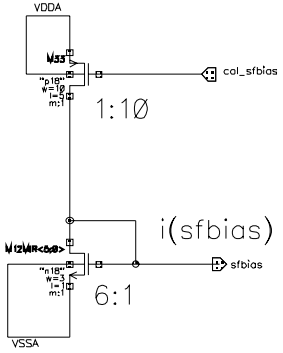
Preamp Bias



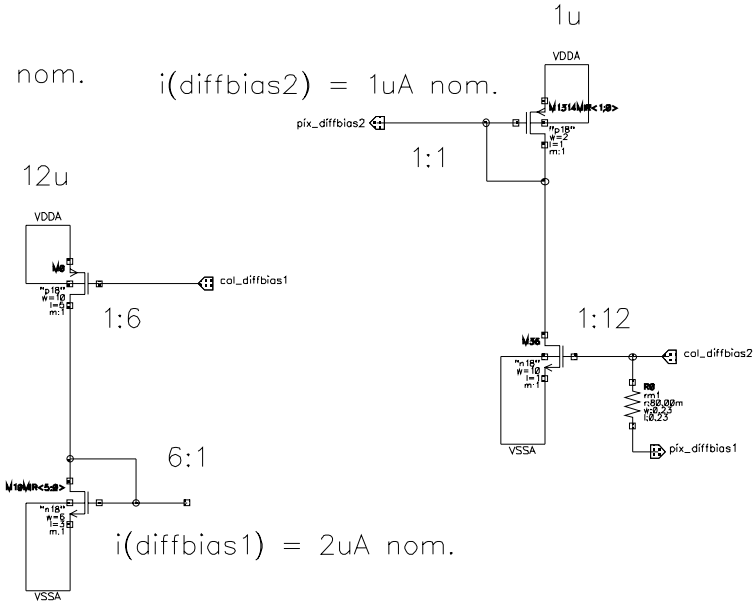
VDDA

VSSA

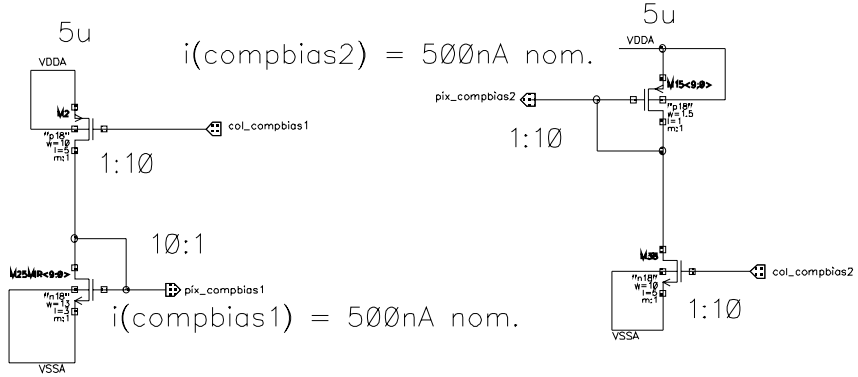
SF



Diff Shaper Bias

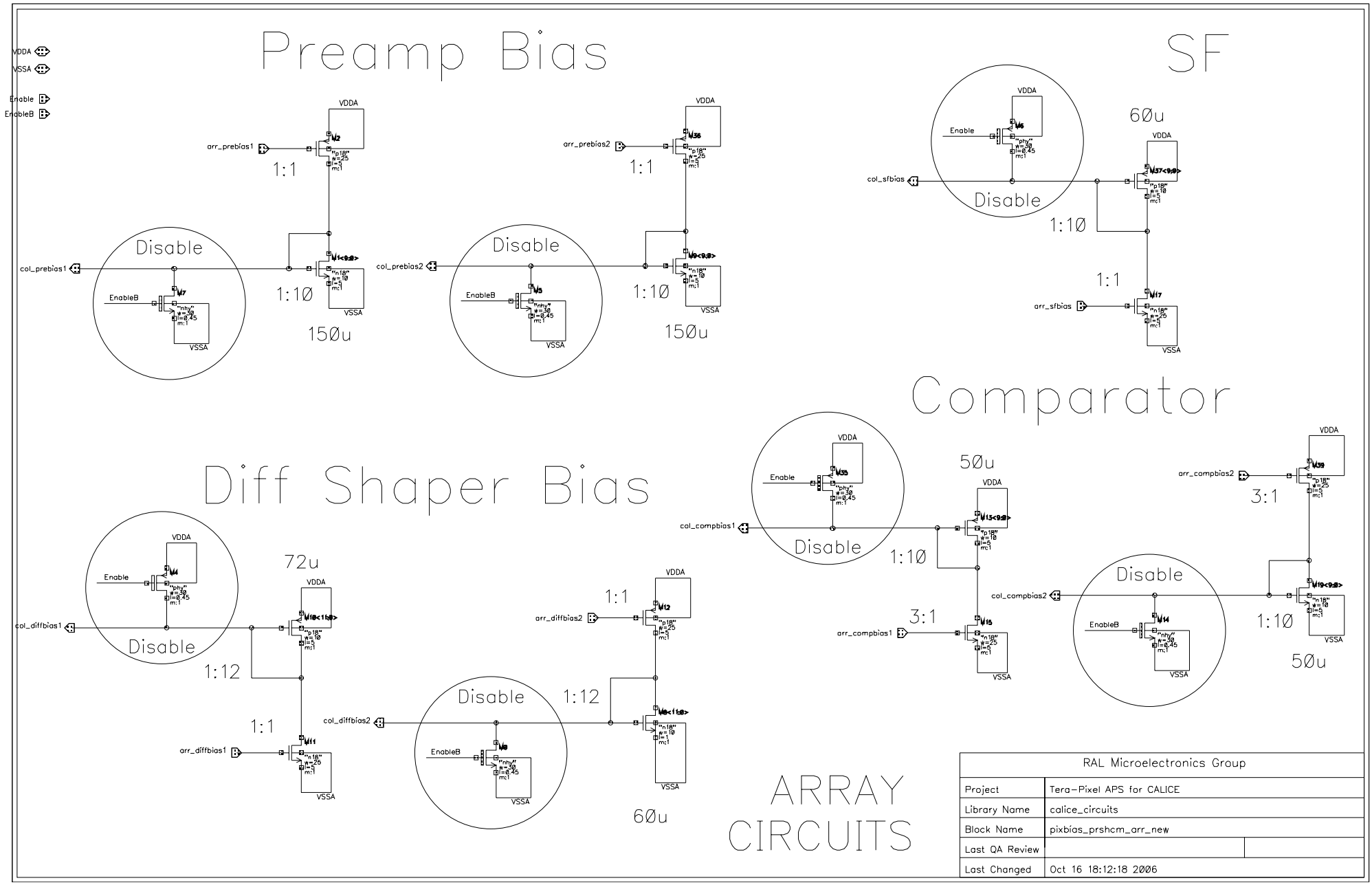


Comparator Bias



COLUMN CIRCUITS

RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixbias_prshcm_col_new
Last QA Review	
Last Changed	Nov 24 10:15:43 2006

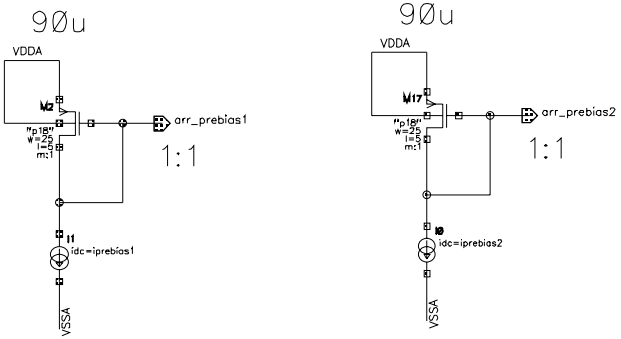


RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixbias_prshcm_arr_new
Last QA Review	
Last Changed	Oct 16 18:12:18 2006

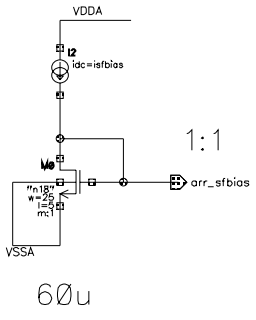
Preamp

VDDA

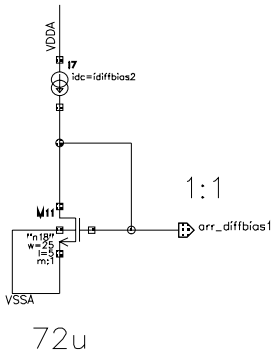
VSSA

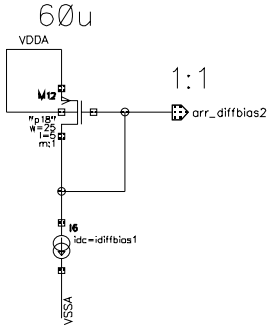


SF

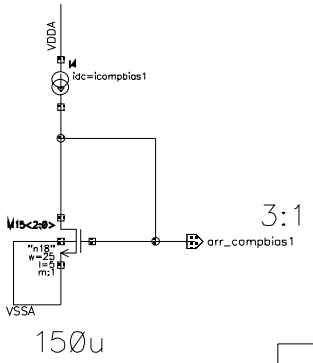


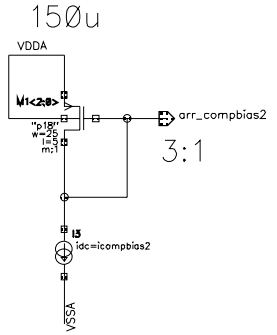
Diff Shaper Bias



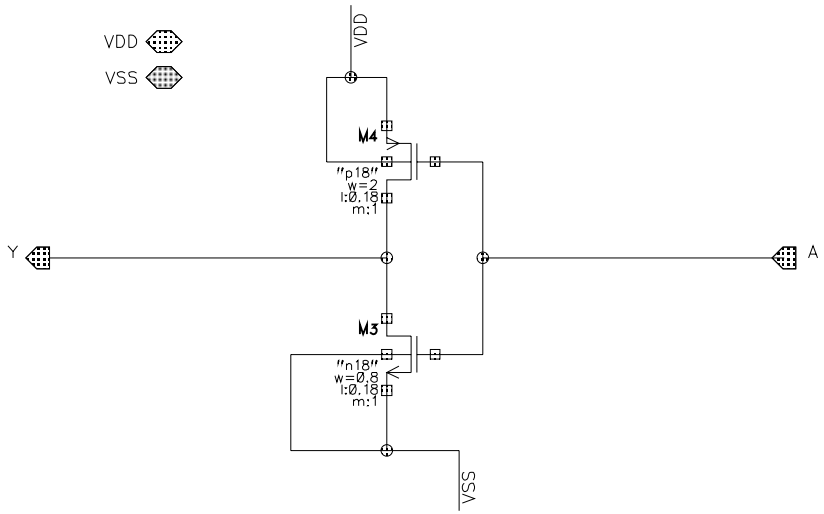


Comparator Bias

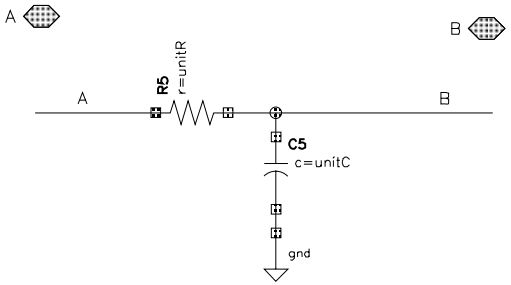




RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	pixbias_prshcm_sim_new
Last QA Review	
Last Changed	Oct 16 18:12:59 2006



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_feasability
Block Name	logic_inv_x1
Last QA Review	
Last Changed	Sep 28 11:46:11 2006



RAL Microelectronics Group	
Project	Tera-Pixel APS for CALICE
Library Name	calice_circuits
Block Name	column_load_1bit
Last QA Review	
Last Changed	Sep 28 14:10:30 2006