CALICE-UK Report to the STFC Oversight Committee

May 31, 2007

1 Introduction

The CALICE collaboration is a worldwide effort to study calorimetry for the International Linear Collider (ILC). The collaboration is described in more detail in Section 2 below.

UK involvement in CALICE started in 2002. The PPRP granted seedcorn funds for five groups in December of that year to join the collaboration. In February 2005, seven UK groups then returned to the PPRP for further funding to complete the ongoing programme of beam tests as well as start several longer-term R&D programmes, which were funded to March 2009.

The UK CALICE groups were also part of the successful EUDET infrastructure bid to the EU, which was approved in January 2006. This gives the UK funding to produce a DAQ system for reading out future calorimeter prototypes also being produced within the EUDET framework.

The individual workpackages are described in more detail in Sections 3 to 7. The Gantt charts, milestones, financial and risk tables are supplied separately and some related points are discussed in Section 8.

2 General status of CALICE

The CALICE collaboration is undertaking a major programme of R&D into calorimetry for the ILC, directed towards the design of an ILC calorimeter optimised for both performance and cost. It now has over 200 members from 41 institutes worldwide and is by far the largest group studying calorimetry for the ILC. New groups continue to join CALICE and since the last OsC meeting, three new countries (Canada, India and Spain) have had institutes become members.

It is the only collaboration within the ILC community studying both electromagnetic (ECAL) and hadronic (HCAL) calorimeters in an integrated way. The collaboration serves as an umbrella organisation for longer-term ILC calorimeter projects where developments can be tested together.

There are four ILC detector "concept groups", of which three are of a significant size. These three are also the ones which have calorimeters based on particle flow (PFA) concepts, the approach supported by CALICE. The aims of the concept groups are supposed to be to evaluate and compare the physics potential in the context of a full detector of the various ideas coming from the (separate) R&D groups. Although nominally worldwide groups, the three major ones tend to be dominated by single regions; LDC[1] is mainly European, SiD[2] is mainly based in the US and GLD[3] is mainly Asian. LDC and GLD have recently decided to cooperate more closely and it is widely assumed they will merge at some point in the future, although at present they still operate separately. An R&D collaboration like CALICE tries to have a strong contribution

[1] http://www.ilcldc.org/

[2] http://www-sid.slac.stanford.edu/

[3] http://ilcphys.kek.jp/gld/

to all three major concept groups, although since it originated from the TESLA TDR design, the strongest ties are with the LDC group.

There are two main R&D directions within CALICE; the "physics prototypes" and the "technical prototypes". These have very different aims. The physics prototypes are being used to acquire large data samples in beam tests so that the calorimeter simulations can be tuned to agree. This will allow the design and optimisation of ILC detectors based on similar technologies with a high degree of confidence in the simulation. The technical prototypes are designed to be a first attempt at building semi-realistic "ILC-like" calorimeter modules. These are intended to give crucial information on the real integration issues and constraints of building such a calorimeter.

2.1 Physics prototype programme

The collaboration will test physics prototypes of two ECAL technologies along with at least two types of HCAL technology in electron and hadron beams over the next 18 months. The CALICE programme also covers simulation studies incorporating the results of these tests into the ILC detector simulation programs.

The most advanced of the CALICE ECAL physics prototypes is a silicon-tungsten sampling calorimeter and consists of 30 layers of silicon wafers interspersed between tungsten sheets. Each wafer layer contains a 3×3 array of silicon wafers, each containing 36 $1 \times 1\,\mathrm{cm}^2$ diode pads. There are around 10,000 channels in total occupying a volume of approximately $(18\,\mathrm{cm})^3$. The ECAL is mainly a collaboration between the French and UK groups, with the former responsible for the mechanics and silicon detectors and the latter for the readout electronics. The ECAL assembly has been paced by the silicon wafer production and there were problems with wafer production throughout 2005 and 2006. However, the total required number of functioning wafers are now in hand. Around 80% of these have now been assembled into detector planes and the rest are expected to be completed by July 2007.

The second ECAL physics prototype is a scintillator-tungsten sampling calorimeter, called the ScECAL. It consists of 27 layers of scintillator strips, with each layer covering an $18 \times 18\,\mathrm{cm}^2$ area. The scintillator strips are $1 \times 4.5\,\mathrm{cm}^2$ in their transverse dimensions and each layer contains a 4×18 array of strips, for a total of around 2,000 channels. This calorimeter is mainly built by the Japanese institutes, although it uses the same on-detector electronics as the AHCAL (see below) and the UK readout electronics. This reuse of existing equipment and expertise illustrates well the power of a large collaboration like CALICE. A test stack of 1/4 size (the full depth of 27 layers, but only a $9 \times 9\,\mathrm{cm}^2$ area in each layer) was assembled and tested in a beam at DESY in March 2007. The rest of the full physics prototype is under construction and will be completed in January 2008.

The first HCAL is the analogue HCAL (AHCAL), a sampling calorimeter with 38 layers of steel absorber sheets instrumented with scintillator tiles. Each layer has a $96 \times 96\,\mathrm{cm}^2$ area and the total volume is approximately $(1\,\mathrm{m})^3$. The tiles are of varying sizes, with the highest granularity central region using $3 \times 3\,\mathrm{cm}^2$ tiles, increasing to $12 \times 12\,\mathrm{cm}^2$ for the outermost tiles. As the name implies, the readout is analogue, with the off-detector UK electronics being common to the ECAL. The AHCAL has around 8,000 channels in total. It is a collaboration of many small European institutions but is led by a large DESY group. The assembly has been mainly paced by the manufacturing rate of the silicon photomultipliers used to read out the tiles. These are now all in hand and the AHCAL will be fully assembled in May 2007. The AHCAL is complemented by a "tail-catcher" (TCMT) consisting of 96 cm of iron instrumented with 16 layers of 5 mm $\times$ 5 cm scintillator strips, which tag shower leakage and detect muons. This detector was completed in 2006.

Secondly, the digital HCAL (DHCAL) is a binary readout sampling calorimeter. The sen-

sitive layers will be mainly resistive plate chambers (RPC) although for some of the tests, one or more layers may be replaced with gas electron multiplier (GEM) or micro-megas detectors. In all cases, the pads will be $1 \times 1\,\mathrm{cm}^2$, giving around 350,000 channels, each reading one bit. The DHCAL has been mainly a US and Russian collaboration, although within the last six months, the effort has been expanded by groups from France and Spain. As one of the main aims of the beam tests is to compare the performance of these HCAL options, the same absorber structure and tail catcher as for the AHCAL will be used, so as to eliminate any spurious differences which might otherwise arise. Hence, the DHCAL is also around $(1\,\mathrm{m})^3$ in volume. The DHCAL funding is mainly required for the readout electronics. Applications for funding are pending in the US, France and Spain. Assuming funding is secured, the DHCAL should then be completed by the middle of 2008.

All these detectors will be run in various combinations, described in Section 3. The data from all are collected in a common format to allow a common analysis structure for all detectors. The UK online DAQ system and software is used for all such beam tests.

2.2 Technical prototype programme

The technical prototype programme is growing rapidly and has expanded significantly over the period since the last OsC meeting. The aim of this effort is to understand the real-world issues of building a calorimeter for the ILC. Hence, the technical prototypes are being designed to be a "best guess" of how such a calorimeter module might look in terms of mechanical structure, cooling, sensitive layers, on-detector electronics and off-detector readout. These "ILC-like" calorimeter modules will be tested in beam when complete. However, unlike for the physics prototypes, the aim would not be to accumulate a high statistics sample for comparison with simulation, but to assess the functionality (signal/noise, leakage, timing resolution, etc.) of the modules. As such, they do not need to be fully populated. This effort started with the EUDET work, which aims to build a technical prototype of the silicon-tungsten ECAL and the AHCAL. The expansion of the DHCAL effort to include European groups has enabled them to start working on an DHCAL technical prototype also. There are no firm plans for a scintillator-tungsten ECAL technical prototype at this stage.

The ECAL technical prototype will be mechanically the size of a LDC current design detector ECAL module. This is specifically 1/40 of the total barrel calorimeter, being approximately $1 \times 1.5\,\mathrm{m}^2$ in area and 30 layers deep. It will be partially equipped with silicon wafers; 1/7 of the module will have full depth and one complete layer of the 30 will be fully populated. The mechanical structure will have the size and cooling structures expected in a real detector and the UK will contribute to this design. The on-detector readout will use ASICs embedded in the detector which are able to operate triggerless and can buffer data with no deadtime during an ILC beam spill. The data are then read out between spills and the chip can be powered down to reduce the heat load before the next spill. The off-detector readout, the UK contribution, will use the UK DAQ design to provide a prototype DAQ system which would in principle be capable of operating at the ILC. This will give invaluable experience in the real applications of the UK ideas. The module is scheduled to be completed in 2008 and exposed to beams from early 2009 onwards. It will serve as a test bed for the various projects within CALICE; in particular, layers will be able to be replaced by ones containing the UK MAPS sensors, allowing a controlled comparison between them in a very similar environment.

In a similar way, the AHCAL technical prototype will represent a fraction of 1/32 of the LDC barrel HCAL. It will correspond to a half-octant of a half-barrel with an area of approximately $1 \times 2\,\mathrm{m}^2$ and a depth of 40 layers. It is scheduled to be completed on the same timescale as the ECAL. Like the ECAL, it will be equipped with second-generation on-detector ASICs with ILC-like specifications. The DHCAL technical prototype plans as less well-advanced. as this

effort only started recently. It will be 1/36 of an SiD barrel module (1/12 of a CMS-style barrel ring, with the total consisting of three such rings) although the ASIC and other on-detector electronics have not yet been defined. The UK is not contributing directly to either of these prototypes in terms of the detectors themselves. However, the UK DAQ will be used for readout of the AHCAL module and it is highly probable the DHCAL readout electronics will be designed to integrate into the UK DAQ also.

2.3 CALICE-UK Perspective

The ILC political situation worldwide is in a state of rapid flux. The medium term UK aim is to contribute strongly to the detector designs, having established ourselves in the community. The timescale for this was originally set by the TDRs, scheduled for 2009/10, which were to be based on the detector concept groups, with true collaborations forming after this. However, there is now a move for the concept groups to produce LoIs in around a year, following which two would be chosen and these would lead to two collaborations by late 2008, which is significantly earlier than previously planned. These collaborations would then produce "lightweight" Engineering Design Reports (EDR) by 2010 as it is thought that two costed and buildable detector designs must be available by the earliest possible date that ILC funding could be secured. However, since a lot of the worldwide R&D will not be complete on this timescale, the EDRs will allow alternative solutions for the detector technologies and true TDRs will come two or three years later.

The task for the UK groups between now and 2010 is to be able to contribute strongly to the detector collaborations as they form such that we have a significant role in the EDRs. This will give us a long-term position within the ILC community. This has to start by stepping up our interactions with the concept groups and this will be a short-term goal over the next year. Through CALICE, there are already reasonable contacts with LDC and this will also give us some influence in GLD as they become closer. We have recently started talking to SiD and a UK speaker gave a MAPS overview talk at the recent SiD meeting in April[4]. The aim is to expand these contacts over the next year.

We see the above as taking place through two paths. Firstly, the UK is contributing strongly to the analysis of the data from the physics prototypes. This means the UK will have a strong role in the simulation tuning and subsequent application of the simulation to the detector optimisation work. The UK is leading the PFA work and is contributing to physics benchmark studies for detector designs. All this work is within WP1 and 5 and will position us for the short-term detector collaboration studies when the collaborations form.

Longer-term, the UK technical contributions to the EDRs will be through our R&D work in DAQ, MAPS and mechanical studies; this is covered in WP2, 3 and 4, respectively. As described in the previous OsC submissions, we would aim to have at least one of the DAQ or MAPS designs accepted as part of the EDRs, and preferably both. The mechanical design studies are part of the generic ECAL mechanical plans and so will almost definitely be part of any ECAL EDR contribution.

3 WP1: Beam Test Programme

This workpackage covers the ongoing beam test programme, the UK effort to support it, and the analysis of the data collected. The work of WP1 will give a large dataset of interactions which can be used to tune and verify the realism of the various simulation models on the market. This is to ensure we have a reliable simulation for all the studies needed for WP5. This workpackage has the highest degree of interaction with, and dependence on, non-UK groups.

[4] `http://www.hep.ph.imperial.ac.uk/calice/maps/conferences/sidtalk100407.pdf`

A large volume of data was recorded at test beams in DESY in May 2006, followed by CERN in August-October 2006. Since then, attention has focussed on analysis and understanding of these data. The UK has a strong leadership rôle in this endeavour; in autumn 2006 N.K. Watson and D.R. Ward were invited jointly to coordinate the analysis work. Our focus has been on having an extensive array of preliminary results for presentation at the principal annual ILC workshop, LCWS07 in DESY at the start of June 2007. A few highlights of this work can be presented here.

3.1 Task 1.1: Support for beam tests

The UK hardware and firmware for the readout electronics was completed in time for the CERN run in 2006. Work since then has been to repair boards damaged by handling and general wear and tear through their use in the beam areas. Currently, the boards have less than 1% bad channels. The calorimeters do not require every channel to be cabled so for the coming beam tests at CERN and FNAL, only fully functional channels will be used.

The software was also mainly complete for the 2006 CERN run. The main work since has been to support the new detectors. The quarter-size ScECAL run in March 2007 required some changes, mainly to allow automatic switching in the offline code between the two ECALs, and these were done by the Imperial group. The online software ran very smoothly through the ScECAL run and around 50M events were taken. The semi-online monitoring program, a Cambridge responsibility, was upgraded for ScECAL use. This included the event display; an example of an event is shown in Fig. 1.

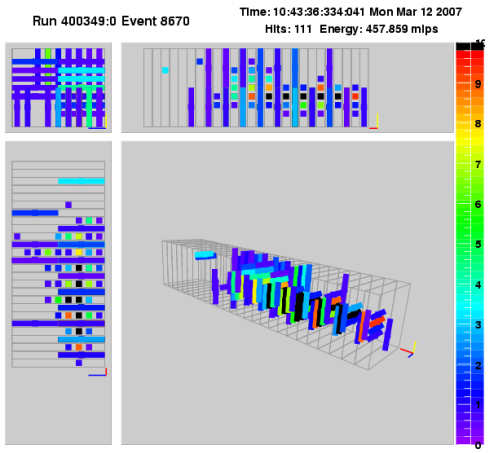

Figure 1: *Semi-online event display from the ScECAL run, showing the response to a 3 GeV electron.*

Future work will be needed to integrate the DHCALs into the DAQ online software. This has been ongoing for some time and should be completed by June as the European DHCAL groups will run one plane in the DESY beam at that time. In addition, the US DHCAL group will do a "slice test" of small RPCs and GEMs in the beam at FNAL in June and July. In principle, this should complete ID5 on the Gantt chart. However, as these are small subsections of the full detectors, further work will almost definitely be needed later.

The biggest task, of integrating the full $(1\text{m})^3$ US DHCAL at FNAL, will be around one year from now. This will include the FNAL beam line tracking, triggering and particle-identification devices, all of which will need to be incorporated into the CALICE readout. All these tasks will again be supported by the Imperial and Cambridge groups.

Because of the delay in the FNAL beam tests, the DAQ tasks of ID4 and ID5 will not be completed until well into 2008.

3.2 Task 1.2: DESY test beam

As reported to the last OsC meeting, the main round of ECAL beam tests at DESY took place in May 2006. At that time, 24 layers of silicon detectors were installed (placed in layers 1-22 and 25-26 of the calorimeter), each covering an area of $12\times18\,\mathrm{cm}^2$. For the electron beam energies available at DESY, up to 6 GeV, this provided sufficient instrumented depth to contain the showers. Data were recorded covering the energy range 1-6 GeV, at several beam impact points on the calorimeter, and at angles 0°, 10°, 20°, 30° and 45°. In all around 10M beam triggers were recorded. Preliminary analysis of these data was reported to the last OsC meeting. Full analysis needed to wait for muon data recorded at CERN in October 2006 in order to obtain calibrations. The analysis of these data is discussed below along with the CERN analysis, because the intention is to publish a coherent description and understanding of the data over the combined DESY-CERN energy range.

3.3 Task 1.3: CERN test beam

Installation of the ECAL, AHCAL and TCMT at CERN took place successfully around the end of June 2006. Three two-week periods of data taking were scheduled. The first was lost owing to PS machine problems. The other two were successful, and more than 30M triggers were recorded including electron and hadron beams.

Throughout these tests, the ECAL was fully equipped in depth with 30 layers of sensors, each covering an area of $12\times18\,\mathrm{cm}^2$. The ECAL had all but 9 of its 6480 sensors working. This configuration is adequate to contain electromagnetic showers. At the time of the August run, the AHCAL was equipped with 16 layers of scintillator tiles (giving a total of around 3500 channels), while 23 layers (out of a planned 38) were installed for the October run, by which time the TCMT was also complete.

Electron beam data were recorded with energies in the range 6 to 45 GeV, and at angles 0, 20°, 30° and 45°. Typical event samples were 100-500k triggers, providing useful electron samples of at least 100k events in almost all cases. The electron tests of the ECAL can therefore be regarded as having been successfully completed.

In addition, a sizeable volume of pion data was recorded, as well as muon data for calibration purposes. The data from October are useful for hadronic physics analysis, though the performance will not reflect that of the complete prototype because the AHCAL was not fully instrumented. Also, the rotating table on which the AHCAL is intended to rest was not commissioned, so data were only recorded using normal incidence beams at a fixed position. AHCAL data were recorded both with and without the ECAL.

The UK groups provided a strong presence in the test beam running at DESY and CERN, with emphasis on the DAQ and short-term monitoring and data checking. Monitoring software written at Cambridge was used to provide near-online histograms and an event display. These were produced using an offline job running on the data files was they weere being written during the ongoing run, thereby providing very rapid feedback. This was of great value in providing feedback during the running period. Support of this software has continued and it will soon be used for the first DHCAL module tests at FNAL.

The major task of understanding the combined data and comparing with simulations began in earnest after the October run. A reconstruction processing of the CERN and DESY data was carried out on the Grid in November 2006. The intention is to provide data processed using common calibrations for all members of the Collaboration to use. Much of the work since has been devoted to understanding calibrations and the electronic response effects. Further reconstructed samples have been generated since then, including improved ECAL calibrations, a preliminary version of the AHCAL calibrations, and track reconstruction in the drift chambers.

The UK groups have been involved in many areas of data analysis. In broad terms, up to now the ECAL analysis has been shared between the UK and France, the AHCAL analysis is led by DESY, and the TCMT analysis by Northern Illinois University. The UK activity is summarised below:

- The overall coordination of all CALICE analysis is provided by members of the Cambridge and Birmingham groups.
- A member of the RHUL group has been responsible for modelling the beam line in the Monte Carlo simulation.
- Track reconstruction in the drift chambers at CERN and DESY has been entirely a UK responsibility, with participation from RHUL, Imperial and Cambridge.
- The Cambridge group is working on energy response of the ECAL, linearity and resolution, and transverse shower shape and response near inter-wafer gaps.
- The UCL and Birmingham groups have been studying the longitudinal shower profile in the ECAL.
- Imperial has been working on position and angular resolution of the ECAL, exploiting their work on tracking.
- Imperial has also led the work on digitisation issues such as noise and cross-talk and their implementation in the simulation.

A sizeable note ($\sim$ 50 pp) summarising the ECAL electron analysis is being assembled (coordinated in Cambridge). This will comprise the results to be presented at the LCWS'07 Linear Collider workshop in DESY in June 2007. This will eventually evolve into a publication, when the analysis is stable and complete. All results should be regarded as preliminary, and are not even approved by the Collaboration at the time of writing. We show a couple of typical results here. In Fig. 2, we compare the hit energies seen in data and Monte Carlo for 12 GeV non-showering pions (showing the 1 MIP peak) and for 30 GeV electrons (emphasising the good modelling of the tails up to 350 MIPs). However, in the latter case, there are small discrepancies around the MIP peak (not shown) indicating that there are features of the data or simulation which need further work. In Fig. 3 we show the measured energy resolution for electrons, with Monte Carlo for comparison. Good agreement is seen. In Fig. 4 we show longitudinal shower profiles for several electron energies from 1.5 to 30 GeV, demonstrating the expected logarithmic increase of shower depth with energy. Finally, in Fig. 5 we show the shower position resolution, based on correlating the upstream track with the shower barycentre. Similar notes on the AHCAL and combined analyses are also being prepared before LCWS'07.

Since the successful runs at CERN in 2006 were performed with an incomplete HCAL, and the CERN beam line was available in 2007, we decided to apply for additional running time in 2007, to complement the data taken in 2006. We have been granted six weeks of beam time, with runs in July and August. This will allow (mainly hadron) data to be taken with the fully instrumented AHCAL depth, at a variety of angles of incidence. Comparison with 2006 will provide valuable information about the long term stability of the prototypes.

3.4 Task 1.4: FNAL test beam

Significant improvements are being made to the test beam at FNAL, especially in regard to low energy hadrons (of special importance for Monte Carlo validation). These will be available when the CALICE ECAL, AHCAL and TCMT move their test beam activities to FNAL. The

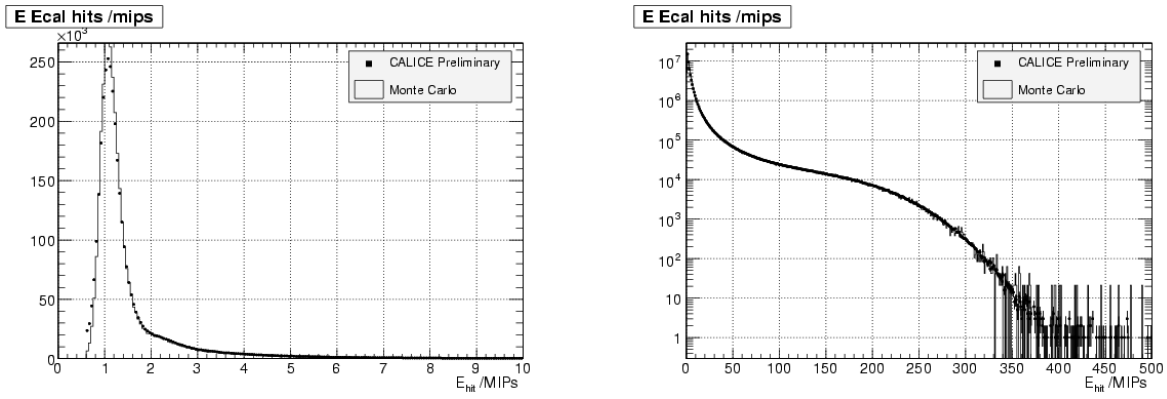

Figure 2: *Distribution of ECAL hit energies for a 12 GeV π^- beam (left) and for a 30 GeV e^- beam (right). Data are shown as points; simulation as the open histogram.*

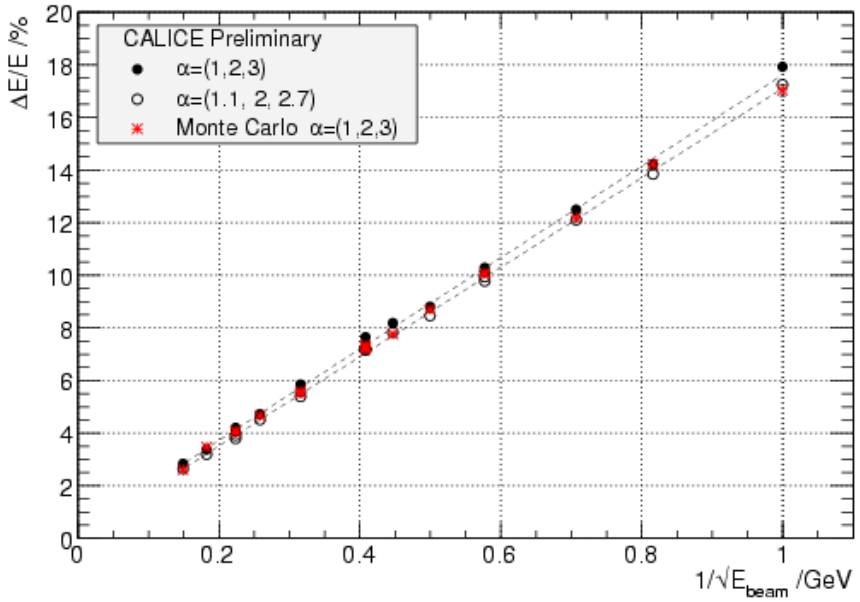

Figure 3: *Fractional energy resolution of the ECAL, plotted as a function of $1/\sqrt{E}$. The plot summarises electron beam data from DESY and CERN taken at normal incidence, with energies 1-45 GeV. Two possible weightings of the different calorimeter stacks are compared. A Monte Carlo simulation is also shown.*

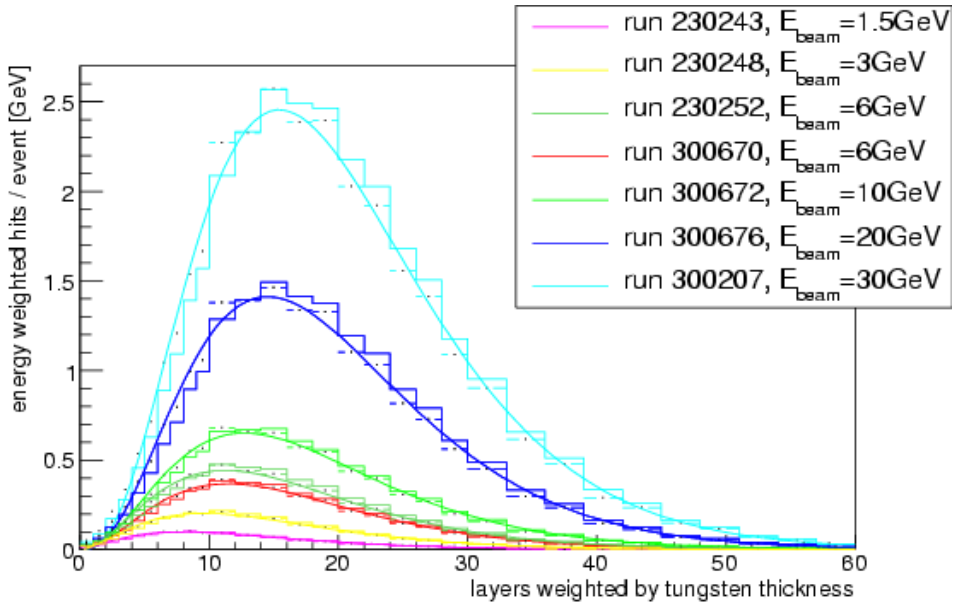

Figure 4: *Longitudinal shower profile from runs at CERN and at DESY with several energies measured in the CALICE ECAL. The data are represented by points with statistical uncertainties and the GEANT4 Monte Carlo simulation by the histogram. Parametrisations of the shower profiles by the form* $\gamma(t) = c\,t^{\alpha}\exp(-\beta t)$*, where* t *is the calorimeter depth in radiation lengths, are also shown.*

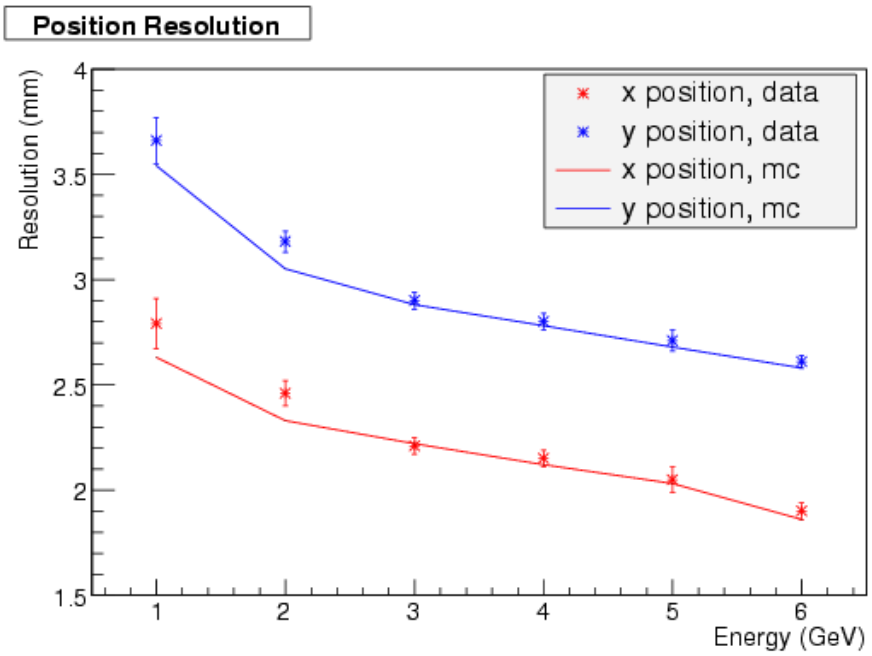

Figure 5: *Resolution in position as a function of the beam energy. The data are shown as points with error bars. The simulation expectation is shown by the continuous line.*

exact timing of the runs in 2007 is not fixed although it is planned that the ECAL, AHCAL and TCMT will move to FNAL in November 2007 and take data there for several months. This will provide lower energy hadrons than available at CERN and will cross check the FNAL and CERN beam results. Running the AHCAL at FNAL will also assist in the comparison between the AHCAL data and the DHCAL data.

The full-size ScECAL will be complete early in 2008 and it will then be run combined with the AHCAL and TCMT. This should give a dataset with which to directly compare the two ECALs. Since all CALICE data are available to all collaboration members, then the UK will be able to analyse the two datasets.

The final combination will be the ECAL, DHCAL and TCMT. This will start when the DHCAL is complete, around mid 2008. This critical dataset will allow the comparison of the AHCAL and DHCAL in a very similar environment. The main dataset will have all DHCAL layers instrumented with RPCs although it is possible that several layers may be replaced by GEMs later in the run.

3.5 Milestones

3.5.1 Milestone ID14: "Complete analysis of DESY data"

This will not be met on schedule and is estimated to be completed in Oct 2007. Great progress has been made in the analysis, but inevitably unexpected features show up in an R&D programme which need attention. An example is a signal-induced pedestal shift (a depression of the pedestals in a wafer containing a high signal), which has recently come to light and is not yet fully understood. The decision to terminate the analysis and publish the results is not one for the Calice-UK groups alone – the analysis effort is rightly being shared between the UK and other groups, and the decision to publish is for the Collaboration as a whole. Nevertheless, we believe that the results outlined here and presented at LCWS demonstrate that good progress is being made.

3.5.2 Milestone ID19: "Successful end of 2006 CERN test beam run"

Since the last report to the OSC, this milestone has been achieved. As reported above, the detectors performed well, and a large volume of data was collected. The electron data are essentially sufficient for the ECAL analysis. The hadron data were taken only at normal incidence, and with an incomplete AHCAL.

3.5.3 Milestone ID20: "Successful end of 2007 CERN test beam run"

Due to the AHCAL being incomplete during the 2006 CERN beam test, we are returning to CERN in Jul-Aug 2007 for further data taking. We shall take advantage of this to record some additional electron data as well, which will be interesting as a test of long term stability of the system. This milestone was set before the CERN schedule was known but is expected to be completed one month later, in Aug 2007.

3.5.4 Milestone ID24: "Submit paper on electron results"

The same comments as for ID14 above hold here. This milestone is estimated to be completed in Dec 2007.

3.5.5 Milestone ID27: "Present interim results at LCWS'07"

This will certainly be achieved. At the time of writing, four internal Calice notes describing results from the CERN test beam are going through their approval procedure. Five talks will be given at LCWS presenting this material.

3.5.6 Milestone ID29: "Complete internal report on hadron data"

This will be based on the 2007 CERN beam test data and is likely to be achieved on schedule, in Dec 2007.

4 WP2: DAQ

4.1 EUDET work

As well as meeting the goals of the grant awarded by PPARC, this workpackage needs to achieve the work programme set out in the EUDET project. This will put the UK at the forefront of DAQ activities for the calorimeter (if not wider) and place us in a position to build the DAQ for the final detector when it is constructed. The effort in EUDET concentrates on providing a technical prototype by the beginning of 2009 at which point we should have a working DAQ system to readout this detector.

In Fig. 6, the proposed DAQ stream is shown for the EUDET prototype calorimeters. At the end of the detector slab, the data will be aggregated and transported off the detector via calorimeter-specific electronics, called a DIF (Detector InterFace). The data will then pass to a Link/Data Aggregator (LDA) which is a generic piece of electronics used by all calorimeter systems, which will serve multiple DIFs. A high-speed optical link will then transfer the data to the off-detector receiver (ODR). The detector-specific DIF for the ECAL will be built by UK groups with the AHCAL and DHCAL DIFs to be built by the institutes, with our input, building the respective detectors. The rest of the DAQ chain will be provided by the UK groups. We are currently defining the LDA-DIF interface which is crucial for all detector builders. Work has also started at Imperial, Manchester, RHUL and UCL on the full DAQ software.

4.2 Task 2.1: Readout of prototype VFE ASICs

The production by French groups of the ASIC chip for the ECAL is delayed, and it is now expected to be fabricated around the end of 2007. The French groups are concentrating on a chip to be used by a DHCAL physics prototype. This chip provides many new features compared to that in the current ECAL physics prototype and is a useful step towards the final ASIC. It has a similar DAQ interface to that expected for the next ECAL chip. Therefore the Imperial group is performing tests on this chip to feedback into the next rounds of design. However, since the readout is digital, this will not allow many of the studies of Task 2.1, such as pedestal and noise stability, to be performed.

The ECAL chip will now only be available at about the time the second round of ECAL production was originally scheduled. Hence, all the Gantt chart items for 2007 ASICs (specifically ID4-6 and the milestone ID7) are now redundant. The project will effectively restart in 2008 with ID8. Work has been done to develop the test DAQ (which will also be used for the MAPS) and so ID3 is well advanced, but will only be complete once the ECAL chips become available.

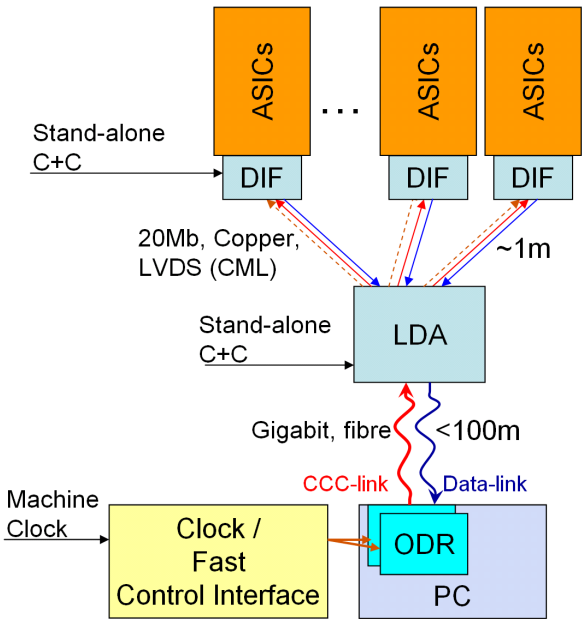

Figure 6: *DAQ stream for EUDET prototype modules*

4.3 Task 2.2: Study of data paths over 1.5 m slab

The hardware for the the model slab, Test Panel 0, is complete and commissioned (sub-tasks ID15 and ID16 and milestone ID17). This is shown in Fig. 7 where a front-end electronics board is coupled to an intermediate board which is then coupled to one of the 24 cm test PCBs. The test PCB has the characteristics of the current design for the the EUDET (and final) ECAL. Tests are ongoing (sub-task ID18) with the one PCB slab, but will also be extended to seven PCBs connected together (Test Panel 1), thereby simulating the full-length EUDET slab. The PCB is populated with FPGAs, each of which mimics two ASIC chips. This panel will allow mechanical and thermal tests to be performed such as methods of bonding two PCBs together and power dissipation. However, the main thrust for the DAQ are: signal and distribution options, ultimate speed, output standards, etc. and these options have been included in the model slab to optimise its performance. The results of these tests will feed directly into the design and build of the EUDET module. Work on the front-end board for the EUDET ECAL prototype will benefit directly from this and will be led by the Cambridge group.

4.4 Task 2.3: Connection from on- to the off-detector receiver

The work on 1 Gbit ethernet tests is complete, fulfilling sub-tasks ID36-ID39 and milestone ID40, and is written up in conference proceedings.[5] We will finalise the 1 Gbit work using the existing testbed to measure network performance through ethernet switches between the FPGA and multiple receiving hosts. It is also essential to understand the mechanisms resulting in the observed packet loss as detailed in the conference report. Preliminary investigations point to problems within the networking stack of the receiving computer. Once these tests are complete we will move on to the 10 Gbit work, fabricating a small 10 Gbit daughter card for the existing FPGA development board and repeating the tests with the full 10 Gbit infrastructure.

[5] D. Bailey, R. Hughes-Jones and M. Kelly, "Using FPGAs to generate Gigabit ethernet data transfers and studies of network performance of DAQ protocols", 15th IEEE NPSS Real Time Conference 2007, FNAL, April-May, 2007.

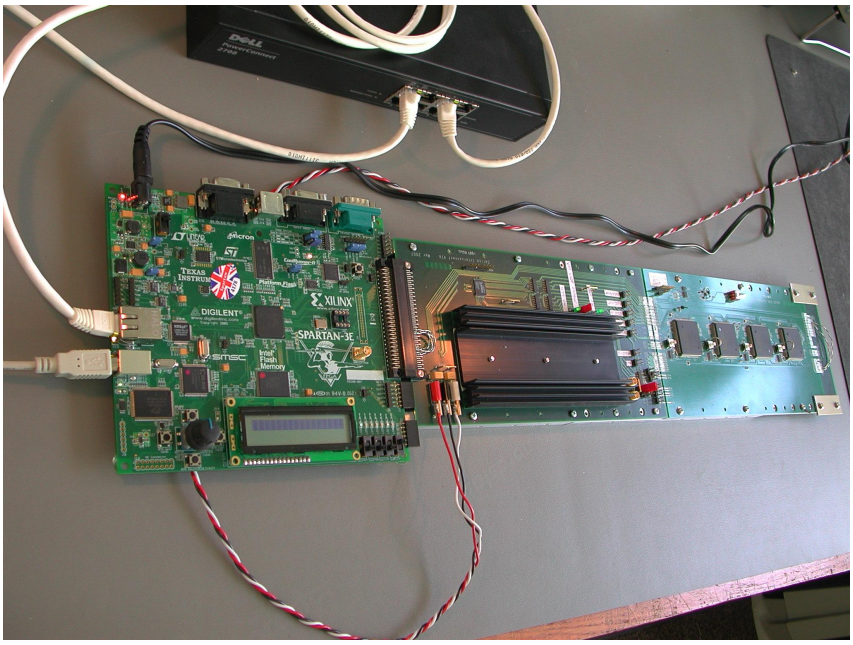

Figure 7: *Picture of model slab showing PCB and readout electronics*

The part of this task dedicated to optical switching has started within the UCL group. Several companies were contacted about their products, with a decision made to purchase a 16 × 16 port optical switch, shown in Fig. 8, from Polatis Inc.[6], Cambridge (UK). The Polatis switch uses multimode (single-mode is also available) fibres and has faster switching than the competitors. This completes sub-task ID55 and milestone ID56, with building a network test rig, ID57, underway.

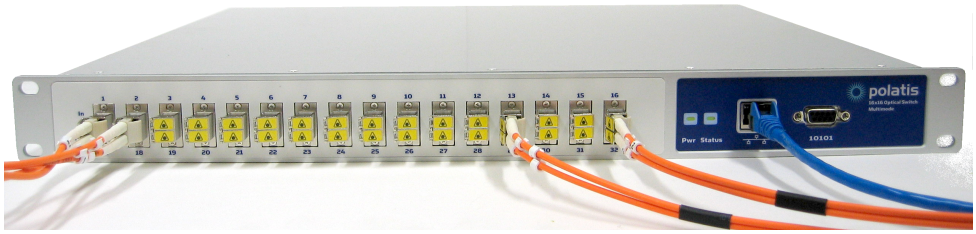

Figure 8: *Optical switch from Polatis Inc.*

4.5 Task 2.4: Transport of configuration, clock and control data

Studies have been completed (sub-tasks ID66 and ID68 and milestone ID67 [7] [8]) on the impact of radiation on the electronics at the end of the slab in the detector volume. Of concern is the rate of single event upsets (SEUs) in the FPGAs, which will require the FPGA to be reconfigured. This is clearly FPGA dependent and the FPGA to be used in the final ILC calorimeter is unknown. However, a study has been performed to determine the rate of SEUs for current FPGAs. The

[6] www.polatis.com
[7] http://www.hep.ph.ic.ac.uk/calice/generalMeetings/070327imperial/bartsch.pdf
[8] http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=1535

rate of particles from physics events impinging on the slab electronics was estimated using Monte Carlo simulation. The neutron, proton and pion energy spectra were then converted into a rate for SEUs for FPGAs for which test measurements had been made. The rate varied considerably from about one SEU every 40 days to one every day for the whole ECAL electronics. From this study, we can conclude that this is a feature which needs to be addressed, but does not require the electronics to be reset on a bunch-train timescale. However, testing for these errors requires a good understanding of the hardware to be tested. A generic design has been proposed making use of the FPGA itself as both device under test and error detector and logger. This relies heavily on duplicated logic and multiple comparisons of output. Suggestions regarding testing the ever increasing array of on-chip resources (e.g. Ethernet MACs, gigabit serialisers) have been made. This highlights that test setups will need to take specific FPGA architectures into account when building hardware. This completes sub-task ID69 and milestone ID70, with all of the results from ID66-ID70 to be presented in a LC note.

A clock and control system has been specified (completing sub-task ID74) that covers all the requirements foreseen from the CALICE collaboration, see Fig. 6. Additionally much tighter tolerances have been placed on e.g. jitter such that the system is also suitable for vertex detector use. The design is modular, flexible and scalable, making use of three tiers of hardware to allow early prototyping without the need for the full system. Signals are distributed using a single serial link to each sub-system. Design effort (sub-tasks ID75 and ID76) is now being focussed on finding the correct hardware and firmware to pass fixed latency commands and good clocks.

Remote configuration of hardware (sub-task ID71) is also being considered as part of this design, but ensuring clock and command signal integrity, as well as efforts to provide detector groups with a prototype system has pushed this to the last of the elements to be addressed. As much of Task 2.4 on clock, control and configuration data is closely linked to the EUDET work, this has meant some sub-tasks are a bit behind schedule but will follow on from the EUDET work.

4.6 Task 2.5: Prototype off-detector receiver

This task is on schedule, with sub-tasks ID85-ID90 complete, including the recently acheived milestone, ID90. The firmware and test software are stored in a central repository for use by each of the University labs which bought one of the cards. An example of some of the ongoing tests is shown in Fig. 9 where transfer rates over the PCI Express bus have been measured for different situations. The outcome of this study was that the high rate (Fig. 9a) when the data was held in memory was compromised by the I/O actions necessary for storage on disk (Fig. 9b). Optimal file systems and storage arrays are being consider to alleviate this. This and other tests form part of the sub-task ID91, which is on schedule, and feeds into sub-task ID92, which has already started.

4.7 Milestones

4.7.1 Milestone ID7: "Successful readout of 2007 ASICs"

This milestone is redundant and has been retired.

4.7.2 Milestone ID17: "Test bench 0 hardware ready and commissioned"

As described above, this milestone was completed since the last OsC meeting four months later than planned, in May 2007. As this work provides a model of the prototype, several iterations with our French collaborators were necessary to incorporate all the necessary functionality for testing.

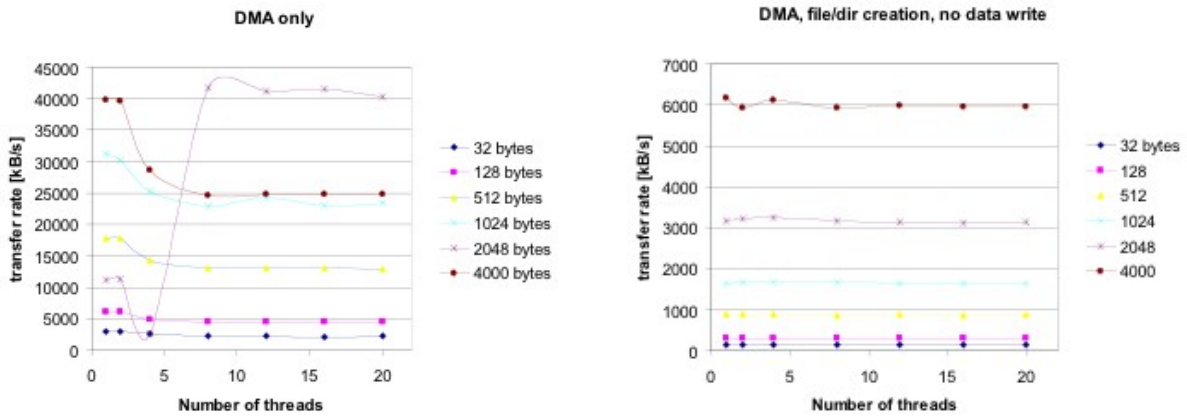

Figure 9: *Performance tests of PCI card to host throughput: (left) when data is held in memory and (right) when files and directories are created and closed.*

4.7.3 Milestone ID20: "Concepts established for 1.5 m data path"

This is expected to be achieved on schedule in Jul 2007. Much of the preparation work, writing test software and firmware was ongoing whilst the test slab was being built, hence this milestone should still be on time.

4.7.4 Milestone ID40: "Report on FPGA ethernet work"

As described above, this milestone was completed since the last OsC meeting three months later than planned, in Apr 2007. This was later than planned as the report for convenience sake was taken as the IEEE conference proceedings which was later than the initial milestone completion date.

4.7.5 Milestone ID50: "Component selection"

This is expected to be achieved on schedule in Sep 2007.

4.7.6 Milestone ID56: "Acquire optical switch"

As described above, this milestone was completed since the last OsC meeting two months later than planned, in May 2007, although the order went through in February. This therefore did not affect the tasks to come afterwards.

4.7.7 Milestone ID67: "Present simulation results"

As described above, this milestone was completed since the last OsC meeting four months later than planned, in Apr 2007. The delay was due to the change in staff with the initial RA leaving.

4.7.8 Milestone ID70: "Make proposal for robust/fliexible test system"

This is expected to be achieved on schedule in Jun 2007. The results are complete and the proposal is being written in the form of an LC Note.

4.7.9 Milestone ID73: "Demonstrate remote FPGA reset and reconfigure"

This milestone will be delayed by three months as it became less of a priority compared to the EUDET work. This will then follow the timeline of the next milestone ID77.

4.7.10 Milestone ID77: "Demonstrate system lock from data interface"

This is expected to be achieved on schedule in Sep 2007.

4.7.11 Milestone ID90: "Initial prototype complete"

As described above, this milestone was achieved since the last OsC meeting. This is the most important task for EUDET and hence has international pressures so it is essential to keep this on time.

4.7.12 Milestone ID94: "Initial system complete"

This is expected to be achieved on schedule in Dec 2007.

5 WP3: MAPS Development

The MAPS project has continued to make good progress since the last OsC meeting. The project has had regular meetings throughout this period[9]. The first round sensor was submitted for fabrication by the RAL Microelectronics group in April 2007 and is due back in July. This fulfils ID7 in the WP3 Gantt chart. This is a delay of approximately two months compared to the original schedule, due to the development of the "deep p-well process" as discussed in the last OsC meeting.

5.1 Sensor fabrication

The project design phase for this first sensor had a mid-term Interim Design Review (IDR1) in December 2006/January 2007 and the design phase was completed following the Final Design Review (FDR1) in February/March 2007. These reviews both correspond to scheduled milestones (ID5 and ID6, respectively) on the Gantt chart. These review are part of the ISO9001 process used in the RAL Microelectronics Division. The reviews both included two external reviewers and documented the schematics, circuit simulation and (for the FDR1) the layout of the sensor. Most of the documentation is publically available for the IDR1[10] and the FDR1[11]; the exception is the schematics which are protected by RAL IP. The outcome of the reviews was a detailed list of modifications, checks and suggested improvements, all of which were implemented before the sensor was submitted for fabrication. A diagram of the final pixel and sensor layout is shown in Fig. 10.

5.2 Sensor simulations

Sensor simulations performed in the RAL PPD group provide an estimate of the signal size and noise. The former depends strongly on the position of the particle within the sensor with a particle crossing the pixel near the corner being the case with the lowest charge collected. The important issue is that all positions give a collected charge above the pixel threshold, so that they register as a hit. Fig. 11 shows the dependence of the collected charge in terms of

[9] http::/www.hep.ph.imperial.ac.uk/calice/mapsMeetings/meetings.html
[10] http::/www.hep.ph.imperial.ac.uk/calice/maps/pdr/idr1.html
[11] http::/www.hep.ph.imperial.ac.uk/calice/maps/pdr/fdr1.html

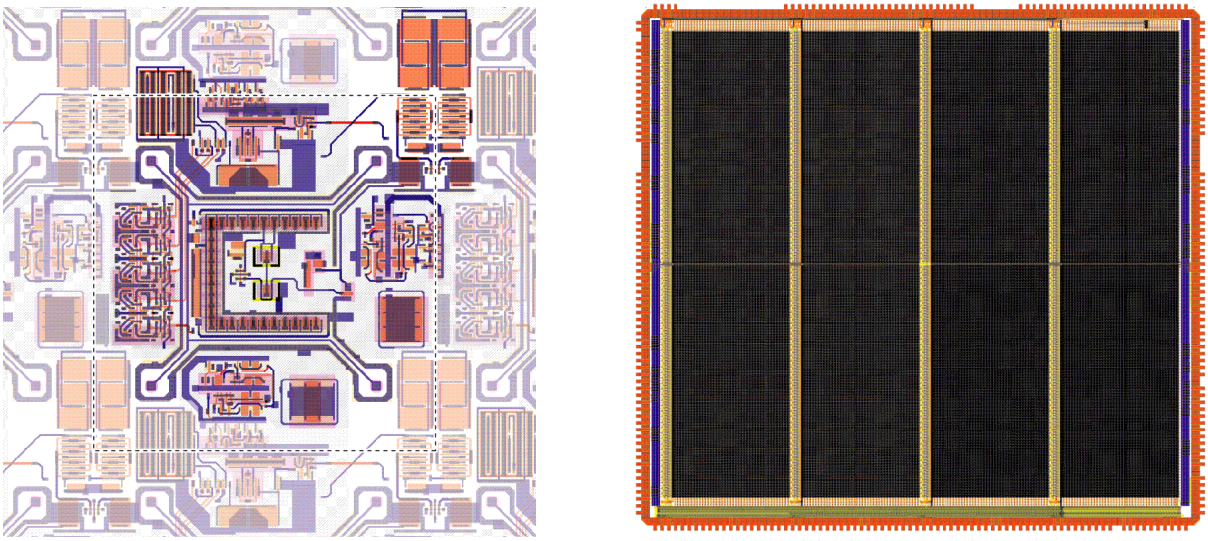

Figure 10: *(Left) First round MAPS pixel layout. The highlighted components illustrate those belonging to one pixel. The dashed line shows the* $50 \times 50\,\mu$m *pixel boundary. (Right) The total MAPS sensor layout. The vertical lines are the areas containing the data memories.*

signal/noise as a function of distance from the corner of the pixel, for three collection diode sizes. The highest signal/noise is seen to occur for a $1.8\,\mu$m diode size and this was the value used in the sensor being fabricated. The signal/noise is seen to be above 10 for all positions with this diode size, which is sufficient for a threshold set at around half the signal value.

5.3 Physics simulations

The physics studies to understand the expected MAPS performance in a full ILC detector are continuing. A full simulation of the charge diffusion, noise and discriminator has been written and interfaced to GEANT4. This work was done by the Birmingham and Imperial groups. A significant improvement of the electromagnetic (EM) resolution was recently obtained with a new concept of "pixel clustering". The charged tracks in an EM shower are spaced far enough apart, even in the dense core of the shower, that the rate of hits in the same or even neighbouring pixels is very low. Hence, a cluster of several neighbouring pixels has a very high probability of being due a single particle, either because it crossed the boundary between pixels or because of charge diffusion into the neighbouring pixels. This means naive counting of pixels has a significant statistical error contribution from such fluctuations as a single MIP going through one layer can give anything from one to nine pixels hit. However, by grouping the pixels into clusters and counting each cluster, rather than each pixel, as one MIP, a better estimate of the number of MIPs, and hence energy of the shower, can be obtained. This is illustrated in Fig. 12 where the various contributions to the resolution are shown. The basic result is that following clustering, the resolution is dominated by the physical fluctuations of the EM shower and the sampling fraction of the silicon and tungsten. Hence, the resolution is very insensitive to the charge diffusion, noise and threshold and the value obtained is now very close to the ideal resolution that would be obtained using the exact ("truth") energy deposits.

5.4 Sensor testing

When the first sensor is returned early in July, it needs to be tested. The DAQ system to read the sensor out is under preparation and is task ID10. A PCB to hold the sensor is being designed at

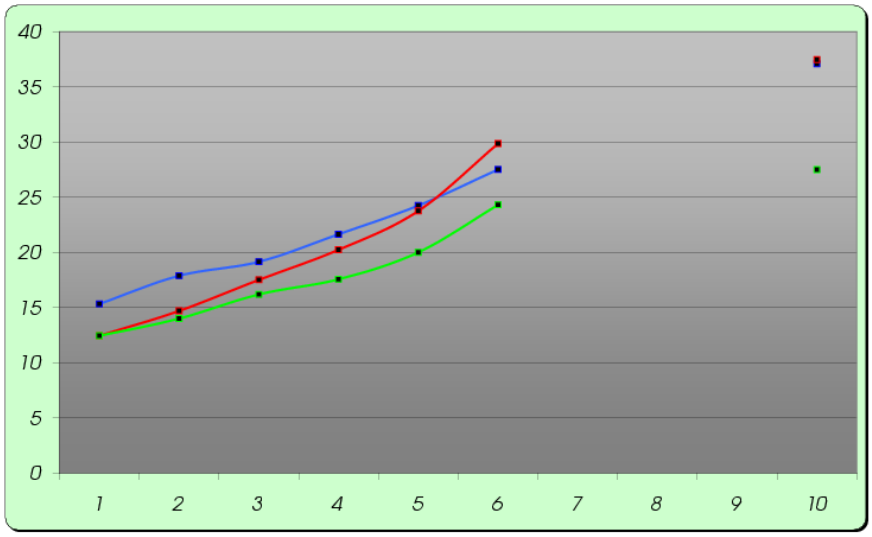

Figure 11: *MAPS sensor simulation of a MIP charge deposited at various distances from the pixel corner. The x axis value 1 corresponds to the corner, while higher values are closer to the centre. The green line is for a diode size of 0.9 μm, blue for 1.8 μm and red for 3.6 μm.*

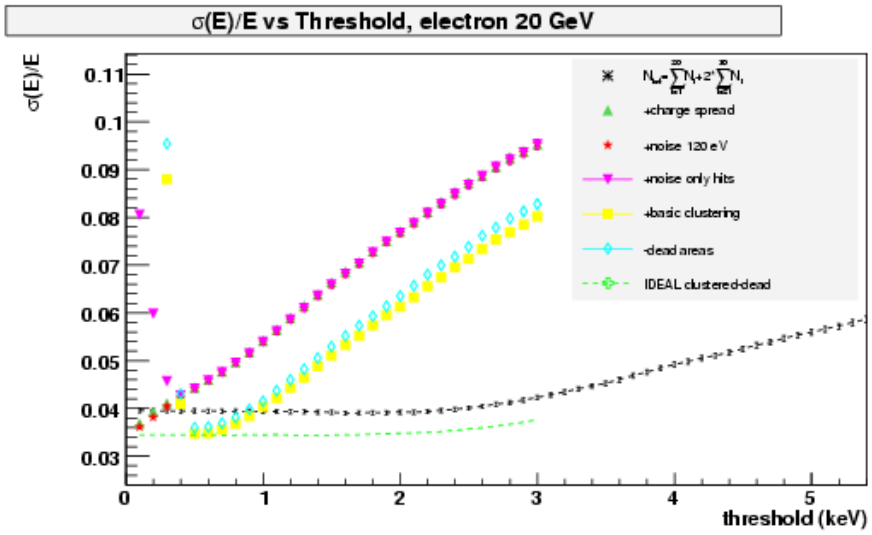

Figure 12: *Contributions to the resolution as a function of threshold. The eventual resolution expected is shown by the light blue points, which indicate a threshold of around 600 eV is optimal. With an assumed noise of 100 eV, this should also give good noise suppression. The resolution should be compared with the light green points, which show the resolution obtained before any digitisation effects are included.*

Birmingham; a review of the schematics was held recently[12]; and the layout review will happen in June. The control and readout will occur through the "USB_DAQ" board, previously designed for the I-IMAS project at Imperial. The test systems for the sensor are also under preparation. In particular, a laser system is being commissioned in RAL PPD to illuminate the sensor with spot sizes of around $2\,\mu$m, which will allow the sensor simulations to be checked in detail. The tests, including cosmics and sources, are scheduled to continue until mid-2008. If successful, then during this period, four sensors mechanically assembled in a stack will be exposed to the DESY electron beam for a first look at their response to an EM shower. These tests are likely to happen around the end of 2007 or early in 2008. A beam test using the first sensor production was not included in the original schedule but is an attempt to compensate for the deep p-well delay. By getting some experience from the first round sensor, then we hope the longer beam test of the second sensor, scheduled for the end of 2008, will be more effective and hence done in the shorter time now available.

5.5 Milestones

All milestones for WP3 are late by two to three months due to the development of the deep p-well process.

5.5.1 Milestone ID5: "First sensor interim design review"

This was three months delayed and was completed in Jan 2007, since the last OsC meeting. The review was done in two parts, the first on 19/12/06 and the second on 25/01/07, as there was too much material considered for one session.

5.5.2 Milestone ID6: "First sensor design review"

This was three months delayed and was completed in Mar 2007, since the last OsC meeting. Again, due to the quantity of material under consideration, the review was done in two parts, on 28/02/07 and 30/03/07.

5.5.3 Milestone ID7: "First sensor design to foundry"

This was three months delayed and was completed in Apr 2007, since the last OsC meeting. The sensor was submitted on 23/04/07, around three weeks after the design review to allow time to implement the review recommendations and perform the suggested cross-checks.

5.5.4 Milestone ID9: "First sensor fabrication complete"

This is expected to be two months delayed and so should be completed in Jul 2007. The fabrication has been entirely in the hands of the foundry since the design submission.

5.5.5 Milestone ID14: "Second sensor design review"

This is expected to be three months delayed and so should be completed in Dec 2007. The date is set by the need to acquire enough results from the first sensor so as to begin to know how to modify the design for the second sensor.

[12] `http::/www.hep.ph.imperial.ac.uk/calice/maps/daq/sensorpcb/reviews.html`

5.5.6 Milestone ID15: "Second sensor design review"

This is expected to be three months delayed and so should be completed in Mar 2008. This is based on the estimated time to know all results from the first sensor relevant to the redesign and to have implemented all changes.

6 WP4: Thermal and Mechanical Studies

WP4 is a smaller project which is using existing expertise in the Manchester group, arising from their work in ATLAS, to study thermal and mechanical aspects for the ECAL mechanical structure. While the UK is not leading the ECAL mechanical design, this work gives us a foothold in this area which we may choose to exploit at a later date.

6.1 Task 4.1: Bonding and glue studies

The long term tests to assess glue reliability are ongoing and will be completed by the LCWS workshop where a final assessment will be made.

A series of PCBs were constructed to carry out tests of the resistance of the glue. Figure 13 shows the conceptual layout of the test boards.

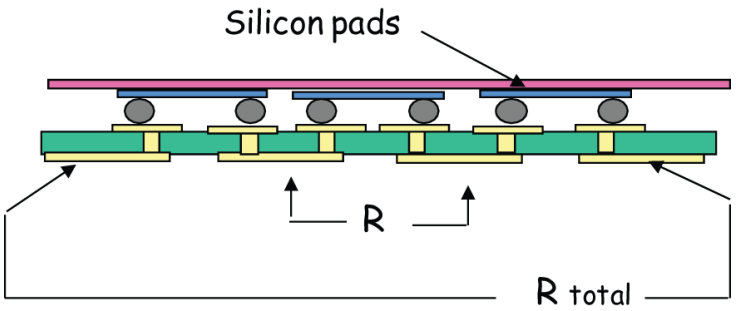

Figure 13: *Snake test schematic*

Pads on the rear of the board are probed to measure the resistance of individual glue dot joints or the total resistance of the snake. The boards are shown in figure 14.

Figure 15 shows a closeup of one of the testing boards with some small glue spots applied. Kapton spacers are used to ensure that each glue spot has the same thickness after the silicon is attached on top.

Measurements of the resistance of the glue snakes have been made in the environmental chamber at Manchester. A typical measurement is shown in figure 16. The data are for a 72-dot snake, continually powered for 500 hours and cycled from 20°C to 70°C with the temperature changing at 1° per minute. There is a clear trend as the glue resistance slowly drops over the first 100 hours and then settles down to around 1Ω per dot. Also visible are the resistance changes due to the temperature cycling. There is no evidence of joint failure.

An interesting effect has been observed in "virgin" glue joints - i.e. joints that have cured for several days without application of a bias voltage. On first application of a voltage, the IV curve can show high resistance at low voltage (typically less than 500mV) followed by chaotic transitions to lower resistance states as the voltage is increased. This behaviour is shown in figure 17. There is a final transition to low resistance (around 1 Ω) when the bias voltage is typically a few volts. Once this state has been achieved it appears to be semi-permanent. Figure 18 shows the corresponding resistance as a function of applied voltage.

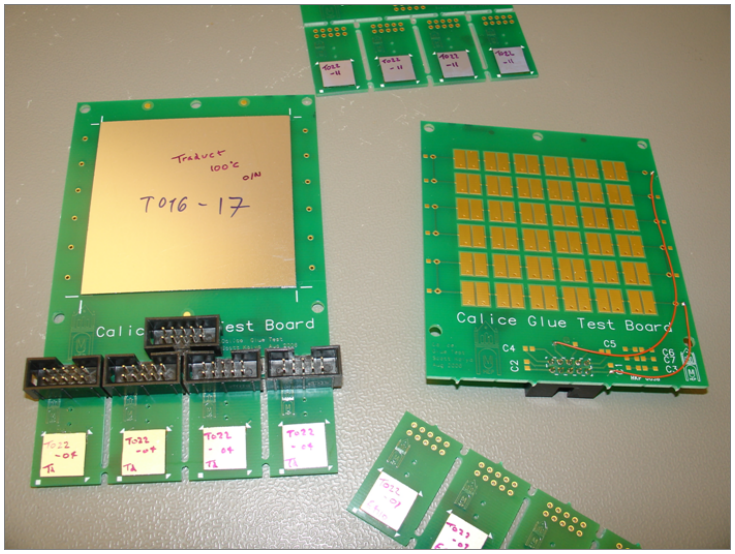

Figure 14: *Snake test PCBs*

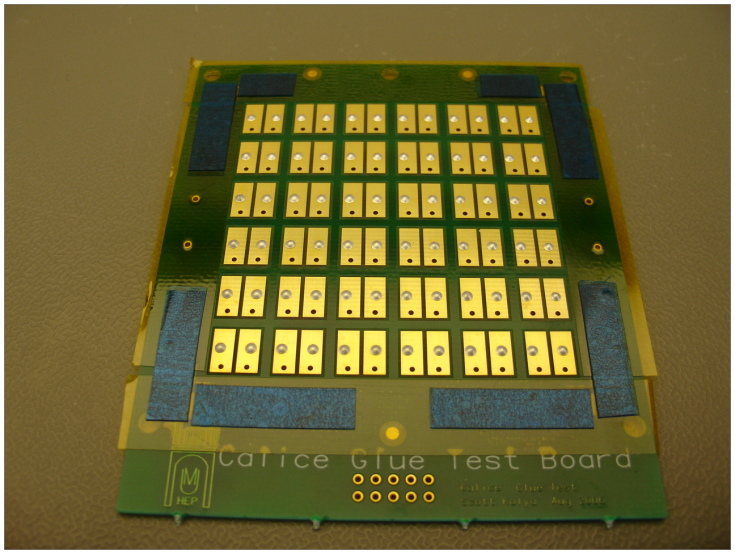

Figure 15: *Snake test PCB with glue applied. Kapton spacers can bee seen at the bottom of the board*

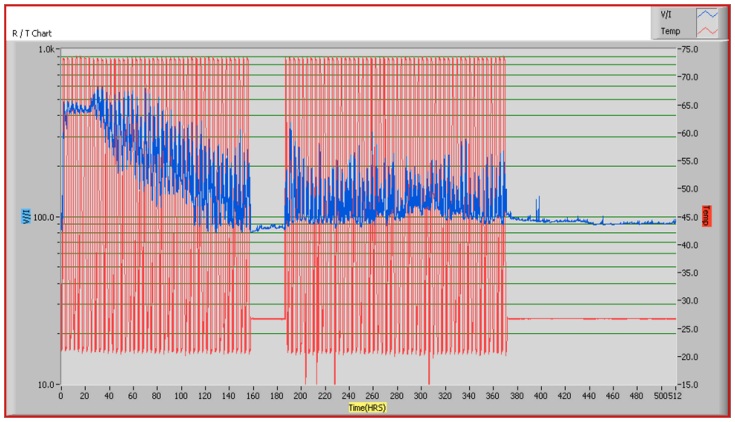

Figure 16: *Resistance measurement of a 72-dot snake*

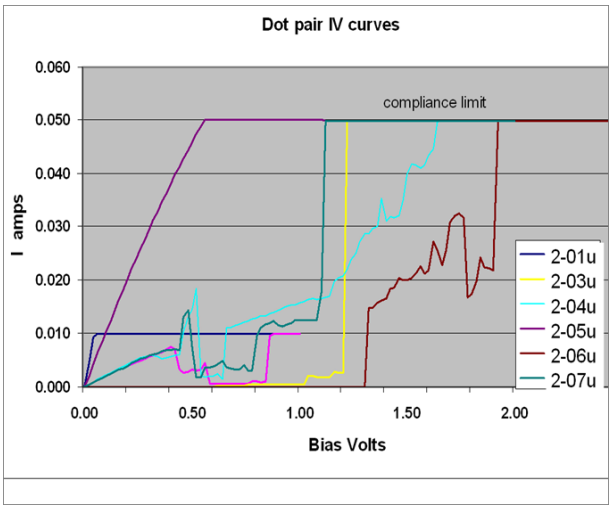

Figure 17: *IV curves of "virgin" glue joints showing the transition to low resistance.*

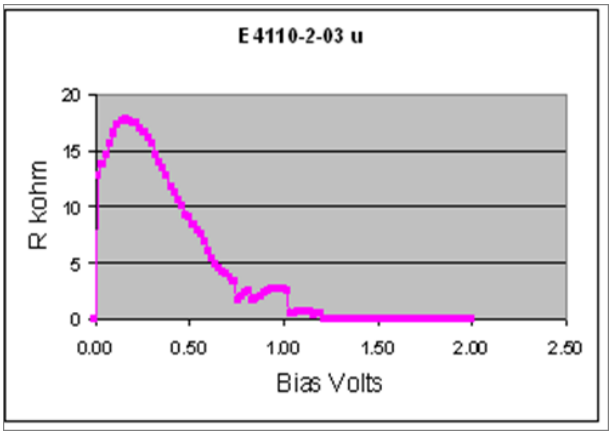

Figure 18: *Resistance of "virgin" glue joint as the applied voltage is increased*

The mechanism for this is unclear, but is probably a complex mix of punch-through of nanometer-scale oxide interface films and mechanical breakdown due to localised heating. There is some evidence that oxide films can reestablish themselves if the glue is left unbiased for months in air, but the low-resistance state can be returned simply by applying a few volts. It would be sensible to put systems in place in the final detector design to allow this voltage application if the detector is likely to be powered-down for significant periods of time, perhaps in a push-pull scenario when the detector is off-beam.

6.2 Task 4.2: Thermal studies

After reporting to the collaboration in 2006, this task is currently on hold.

6.3 Task 4.3: ECAL assembly

This task is due to begin after LCWS, replacing our primary activity on glue tests. We are identifying key areas where the UK can contribute in collaboration with our colleagues in France, and expect to finalise our plans at LCWS.

6.4 Milestones

6.4.1 Milestone ID7: "Report on glue ageing results"

This will be achieved with the presentation of the results of the glue studies at LCWS in May.

7 WP5: Physics and simulation studies

Good progress has been made since the last report. The one milestone expected was achieved, with benchmark results from within the group being shown at a European ILC Software Workshop at LAL[13] in May, jointly organised by Thomson from Cambridge. Further results of both physiscs studies and algorithm development will be shown at the LCWS'07 Workshop, 30-May–04-June 2007.

The progress already made in each of the areas of the project is summarised below.

7.1 Task 5.1: Energy Flow algorithms

The PandoraPFA package developed by Thomson and first released Aug. 2007 has been used by larger numbers of people, including several within the UK both in their physics benchmark studies and also for initial tests within the MAPS project. This package was highlighted in the recent ILC software workshop at LAL, and is seen to be the "state of the art" particle flow algorithm at present in terms of performance, of those algorithms under active development.

The current status of PandoraPFA will be presented[14] at LCWS'07, demonstrating continued good progress with ID9. The physics benchmarking of the algorithm (ID10) is ongoing, thus far greater emphasis has been placed on demonstrating performance using metrics such as jet energy resolution rather than complete analyses (e.g. efficiency for separation of signal from background, mass resolutions, etc.).

The two physics analyses developed to date by CALICE-UK members will be presented at LCWS'07, as expected by ID11, see Section 7.5.1.

[13] `http://events.lal.in2p3.fr/conferences/ILCSoftware`

[14] Status of Particle Flow Reconstruction with PandoraPFA, M.A.Thomson,
`http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=262&sessionId=76&confId=1296`

7.2 Task 5.2: Global detector design

Progress has been made towards optimisation[15] of the global detector design, and now starting to address this for two detector concepts (LDC and GLD), as planned by ID17. To date this has made use of measurable quantities which are readily accessible such as jet energy resolution, and starts to consider segmentation, radius, magnetic field. The extent to which CALICE UK members can contribute to the other major detector concept will become clearer in the forthcoming period, during which the emphasis on the 'concepts" will increase as they (perhaps prematurely) move towards proto-detector collaborations.

To achieve optimisation of the detector concepts using metrics based on complete physics analyses requires a significant amount of effort and more people will have to become involved in this activity in the next period.

7.3 Task 5.3: Workpackage support

Simulations of physics signal processes and machine backgrounds (using GUINEAPIG) have been carried out in support of WP2 and WP3. No significant work has been performed on studying mechanical imperfections (ID22-23) so far. The area of most concentrated effort recently has been in the physics and digitisation simulations of MAPS for WP3, where a complete simulation chain is now in place, including parametrisation of the actual charge flow within the silicon, modelling of noise and application of thresholds. See Section 5 for details. Also since the last report, initial developments of clustering of pixels (within a single layer) and of clustering of energy deposits between layers have taken place. Studies of beam-induced backgrounds using the GUINEAPIG model for the full range of ILC machine parameter options have also been made as part of an investigation of acceptable reset times and occupancies.

7.4 Task 5.4: Physics studies

Physics studies using the ZHH and WW/ZZ processes have continued and latest results are to be presented at LCWS07, see Section 7.5.1. An extensive study was made using the ZHH analysis of the relative performance of PandoraPFA and the combination of the "TrackWiseClustering" and "Wolf" particle flow algorithm, and this was documented as an LC-Note[16] in Feb. 2007.

No significant progress has been made in terms of resolving differences between the software packages which dominate the analysis in different regions, in particular regarding access to geometry information defined in one detector simulation when reconstructing events in a different regional framework. (This is noted as a difficulty, although it is not a specific UK responsibility.)

7.5 Milestones

7.5.1 Milestone ID11: "Presentation of physics benchmark results at LCWS07"

This is achieved with two talks[17], [18] by CALICE-UK members at LCWS'07 at the end May.

[15] Detector parameter optimization for jet measurement, M.A.Thomson
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=201&sessionId=48&confId=1296

[16] M.Faucci-Giannelli, M.Green, F.Salvatore, LC-PHSM-2007-003,
http://www-flc.desy.de/lcnotes/notes/LC-PHSM-2007-003.pdf

[17] Full simulation study of WW Scattering in the LDC00Sc Detector Model, W.Yan,
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=236&sessionId=76&confId=1296

[18] Update of ZHH Studies, M.Faucci-Giannelli,
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=241&sessionId=76&confId=1296

7.5.2 Milestone ID24: "First results from mechanical imperfections study"

This is expected to be achieved on schedule in Dec 2007.

7.5.3 Milestone ID36: "Alternative benchmark analysis available"

This is expected to be achieved on schedule in Sep 2007. There are already two physics analyses developed by CALICE-UK members (see ID11, above), with others in preparation.

8 Financial and managerial issues

The Gantt charts, financial tables, risk proforma and milestone tables are supplied separately. The work-package managers and the project manager hold bi-monthly meetings (normally by phone) at which these tables and other managerial matters are discussed.

8.1 The financial tables

The tables presented at this meeting give the financial status as of the close of the 2007/8 financial year. Column 2 gives the actual spend to that date and column 3 the spend as projected to that date in the original approval. The penultimate column is the difference between these two columns and thus gives the underspend or overspend to date. Column 5, being the sum of columns 2 and 4, gives the estimate of spend to the end of the project. Column 6, being the sum of the amount originally projected to be spent to date and the future intended spend profile, is not meaningful. The final column is our current estimate of the variance in spend at the end of the project. The working allowance is not included in the total.

As noted at the last meeting, delayed appointments of PDRAs at Birmingham and Imperial transfer spend towards the end of the project, leading to small actual underspends and projected overspends. In the last OsC report we said that we had no relaible salary information from RAL but that we beleived that there had been a significand overspend. We now have that information from RAL which shows that, contrary to our fears, similar delayed starts on WP3 in both PPD and TD have led to actual underpends of about £38k in both divisions.

The variations in the RHUL and UCL effort reflect the transfer that has allowed an earlier start and later finish of a PDRA at RHUL from STFC funds, with the UCL PDRA transferred to the EUDET grant. The final nine months of effort at RHUL from April 2009 (approximately £38k) has been included in FY08/9.

The equipment, consumables and travel expenditure has been obtained from the RAL FRS system.

The underspend on travel of about £38k is principally a result of delays to the FNAL beam test programme and so these funds will now be required in this and the next financial year.

The additional development cost of the MAPS deep p-well process of about £15k, discussed in section 5, is shown in the equipment line of WP3 and leads to a projected equipment overspend of the whole project of £15k.

The current equipment underspend of about £40k on WP2 is due mainly to networking equipment for Task 2.3 and PCI cards for Task 2.5 being purchased later. For Task 2.3, the re-profiling of the schedule means that the 10 Gbit equipment will be bought in FY07/08 not in FY06/07 as originally intended. Note, that the optical switch will also be bought completely in FY07/08, bringing this spending forward. The PCI cards in Task 2.5 were bought off-the-shelf and did not require hardware development. Therefore, there were no development costs and buying in bulk was not necessary. Further cards will be purchased for bench-tests and the upcoming prototypes 07/08 and 08/09.

8.2 The Gantt charts

The Gantt charts are unchanged since the last OsC meeting apart from updating the progress bars and checking off milestones. Progress against the Gantt charts is discussed for each work-package in the main body of this report.

8.3 The risk table

As requested at the last meeting we have added a new column giving the cost if the risk is realized. Only two have any cost. WP1.3 could have additional travel costs of up to £30k if further beam tests are needed because of delays, e.g. in prototype construction, and this risk now appears to have been realized. However, the travel funds which will actually be needed to support the beam tests at FNAL in 2008 are not yet known and will not be until the schedule is fully defined. Hence, we treat the £30k as the upper limit until this time. We anticipate that this cost will fall eventually on the working allowance or on savings elsewhere. The second risk with an associated cost is WP3.1, where we could require an additional foundry round if a MAPS run fails.

A new risk, WP4.1 has been identified and added. Other changes since the last meeting are highlighted.

8.4 The milestones tables

These are provided for the first time in the requested format. In these tables we use the word "achieved" to mean that the milestone was complete as scheduled and "completed" to mean that it is complete but delayed compared with the original schedule. Any changes to the schedule of any milestones are shown in bold.

9 Summary

During the time since the last OsC meeting, CALICE has continued to make good progress. Preliminary results from the 2006 beam test data are being presented at LCWS and preparations for the 2007 CERN run are almost complete.

For CALICE-UK, all workpackages have continued to make progress since the last meeting. They are all on, or reasonably close to, schedule and no milestones have been missed by more than four months.

WP3 is running somewhat overbudget due to the unforeseen deep p-well development but the other WPs are financially within or below the budget. Overall, the total is close to budget and well within any ceiling set by the working allowance.

Some tasks have had to be modified in the light of developments from outside the UK but no significant problems have been identified yet.