

## Milestone Tables

<b>Table 1. Milestones for the period Jan 2008 – Jul 2008</b>		
WP1.24 Submit paper on electron results	Mar 2008	<b>Complete May 2008</b>
WP1.29 Complete internal report on hadron data	Mar 2008	<b>Complete May 2008</b>
WP2.16 Test panel 1 complete	Jan 2008	<b>Complete Apr 2008</b>
WP2.45 Demonstrate optically switched network	Jan 2008	<b>Achieved</b>
WP2.83 Initial system complete	Jan 2008	<b>Achieved</b>
WP2.51 LDA-DIF link operational at electrical level	Mar 2008	<b>Achieved</b>
WP2.20 DIF completed	May 2008	<b>Aug 2008</b>
WP2.64 Demonstrate trigger and C + C interface	Jun 2008	<b>Sep 2008</b>
WP3.15 Second sensor preliminary design review	Jan 2008	<b>Complete May 2008</b>
WP3.16 Second sensor interim design review	Apr 2008	<b>Deleted</b>
WP3.17 Second sensor design review	Jun 2008	<b>Achieved</b>
WP3.18 Second sensor design to foundry	Jul 2008	<b>Achieved</b>
WP4.6 End of module – 3D design complete	Apr 2008	<b>Deleted</b>
WP4.11 Module assembly – initial wafers expected	Apr 2008	<b>Achieved</b>
WP5.28 Simulation of MAPS test beam	Mar 2008	<b>???</b>
WP5.38 Report on hadronic modelling studies with test beam	Jun 2008	<b>???</b>

<b>Table 2. Milestones for the period Aug 2008 – Dec 2008</b>	
WP1.33 Successful completion of FNAL test beam run	Dec 2008
WP2.69 Demonstrate work-ability from single trigger	Oct 2008
WP2.53 Working LDA with C&C and ODR	Dec 2008
WP2.92 Complete basic DAQ and run control	Dec 2008
WP3.20 Second fabrication complete	Oct 2008

**Table 3 – Overall milestone list as updated July 2008**

	As at Dec 2007	As at July 2008 Changes in bold	Delay due to		Affects critical path?	See note
			UK?	Other Collaborators?		
WP1.9 Successful end of DESY test beam run	May 2005	Achieved				
WP1.19 Successful end of 2006 CERN test beam run	Oct 2006	Achieved				
WP1.27 Present interim results at LCWS07	May 2007	Achieved				
WP1.14 Complete analysis of DESY data	Jun 2007	Complete Oct 2007				
WP1.20 Successful end of 2007 CERN test beam run	Jul 2007	Complete Aug 2007	N		N	
WP1.24 Submit paper on electron results	Mar 2008	<b>Complete May 2008</b>	Y	Y		
WP1.29 Complete internal report on hadron data	Mar 2008	<b>Complete May 2008</b>	Y	Y		
WP1.33 Successful completion of FNAL test beam run	Dec 2008	Dec 2008	N	Y		
WP1.37 Submit paper on hadron results	Sep 2009	Sep 2009				
WP2.75 Buy PCI cards	May 2006	Achieved				
WP2.27 FPGA 1Gb Ethernet MAC firmware complete	Jul 2006	Achieved				
WP2.57 Present simulation results	Dec 2006	Complete Apr 2007				
WP2.9 Test bench 0 hardware ready and commissioned	Jan 2007	Complete May 2007				
WP2.30 Report on FPGA Ethernet work	Jan 2007	Complete Apr 2007				
WP2.41 Acquire optical switch	Mar 2007	Complete May 2007	Y	N	N	
WP2.79 Initial prototype complete	Mar 2007	Achieved				
WP2.60 Make proposal for robust/flexible system	Jun 2007	Achieved				
WP2.72 Demonstrate remote FPGA reset and reconfigure	Jun 2007	<b>Deleted</b>				
WP2.12 Concepts established for 1.5m data path	Jul 2007	Achieved				
WP2.89 DAQ software choice	Oct 2007	Achieved				
WP2.14 Test bench 1 hardware	Nov 2007	Achieved				

ready and complete						
WP2.16 Test panel 1 complete	Jan 2008	<b>Complete Apr 2008</b>				
WP2.45 Demonstrate optically switched network	Jan 2008	<b>Achieved</b>				
WP2.83 Initial system complete	Jan 2008	<b>Achieved</b>				
WP2.51 LDA-DIF link operational at electrical level	Mar 2008	<b>Achieved</b>				
WP2.20 DIF completed	May 2008	<b>Aug 2008</b>				
WP2.64 Demonstrate trigger and C + C interface	Jun 2008	<b>Sep 2008</b>				
WP2.38 Report on 10Gb performance	Aug 2008	<b>Deleted</b>				
WP2.69 Demonstrate work-ability from single trigger	<b>Oct 2008</b>	<b>Oct 2008</b>				
WP2.53 Working LDA with C&C and ODR	Dec 2008	Dec 2008				
WP2.92 Complete basic DAQ and run control	Dec 2008	Dec 2008				
WP2.23 ECAL DIF available for test beams	Mar 2009	Mar 2009				
WP2.49 Delivery of busy system	Mar 2009	Mar 2009				
WP2.72 Demonstrate remote FPGA reset and reconfigure	Mar 2009	Mar 2009				
WP3.3 Preliminary design review	Apr 2006	Achieved				
WP3.5 First sensor interim design review	Oct 2006	Complete Jan 2007				
WP3.6 First sensor design review	Dec 2006	Complete Mar 2007	Y	N	Y	1
WP3.7 First sensor design to foundry	Jan 2007	Complete Apr 2007	Y	N	Y	1
WP3.9 First sensor fabrication complete	May 2007	Complete Jul 2007	Y	N	Y	1
WP3.15 Second sensor preliminary design review	Jan 2008	<b>Complete May 2008</b>				
WP3.16 Second sensor interim design review	Apr 2008	<b>Deleted</b>	Y	N	Y	1
WP3.17 Second sensor design review	Jun 2008	<b>Achieved</b>	Y	N	Y	1
WP3.18 Second sensor design to foundry	Jul 2008	<b>Achieved</b>	Y	N	Y	1
WP3.20 Second fabrication complete	Oct 2008	<b>Sep 2008</b>	Y	N	Y	1
WP3.25 Second sensor beam	Jun 2009	<b>Deleted</b>	Y	N	Y	1

tests start						
WP4.6 End of module – 3D design complete	Apr 2008	<b>Deleted</b>				
WP4.11 Module assembly – initial wafers expected	Apr 2008	<b>Achieved</b>				
WP5.14 Present initial result from single particle studies	Mar 2006	Achieved				
WP5.26 MAPS implemented in Mokka	May 2006	Achieved				
WP5.33 Status report at regional workshop	May 2006	Achieved				
WP5.4 Comparison of existing PFAs	Jun 2006	Achieved				
WP5.8 Release of V1 of algorithm	Aug 2006	Achieved				
WP5.34 Generic physics analysis implemented	Sep 2006	Achieved				
WP5.16 Present first physics benchmarks results at Valencia	Nov 2006	Deleted	Y	N	N	2
WP5.11 Presentation of physics benchmark results at LCWS07	Apr 2007	May 2007	N		N	3
WP5.36 Alternative benchmark analysis available	Sep 2007	Sep 2007				
WP5.24 First results from mechanical imperfections simulation	Dec 2007	Dec 2007				
WP5.28 Simulation of MAPS test beam	Mar 2008	Mar 2008				
WP5.38 Report on hadronic modelling studies with test beam	Jun 2008	Jun 2008				

Notes:

1. Simulation studies showed that additional design work of a deep p-well process by the foundry was required to achieve the target signal:noise ratio.
2. Initial results were presented earlier to collaboration meetings and we decided to wait until LCWS07 before presenting further results.
3. LCWS07 date fixed as May 2007 after we had set this benchmark.
4. Phase 1 of ASIC development skipped by our collaborators.