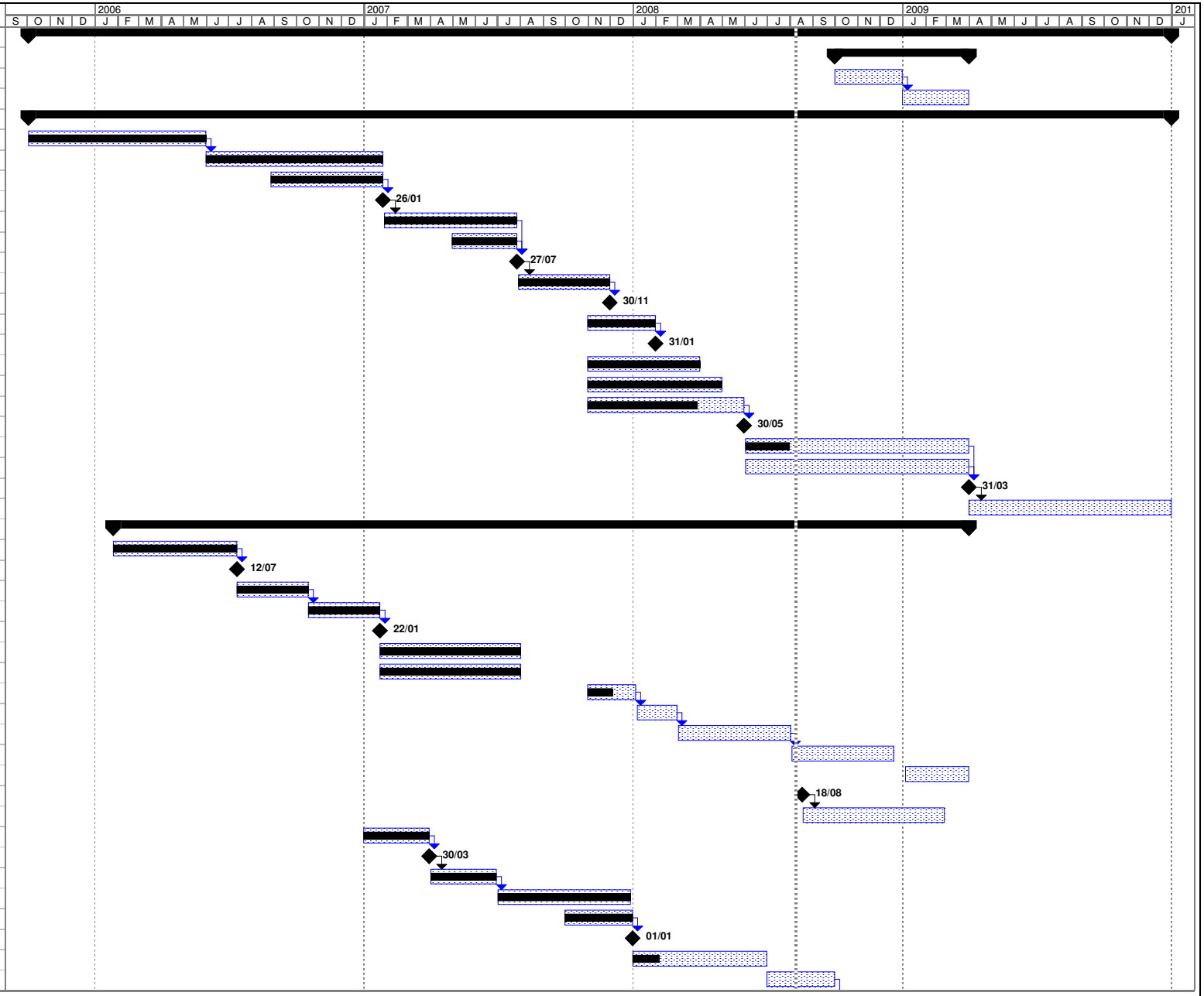
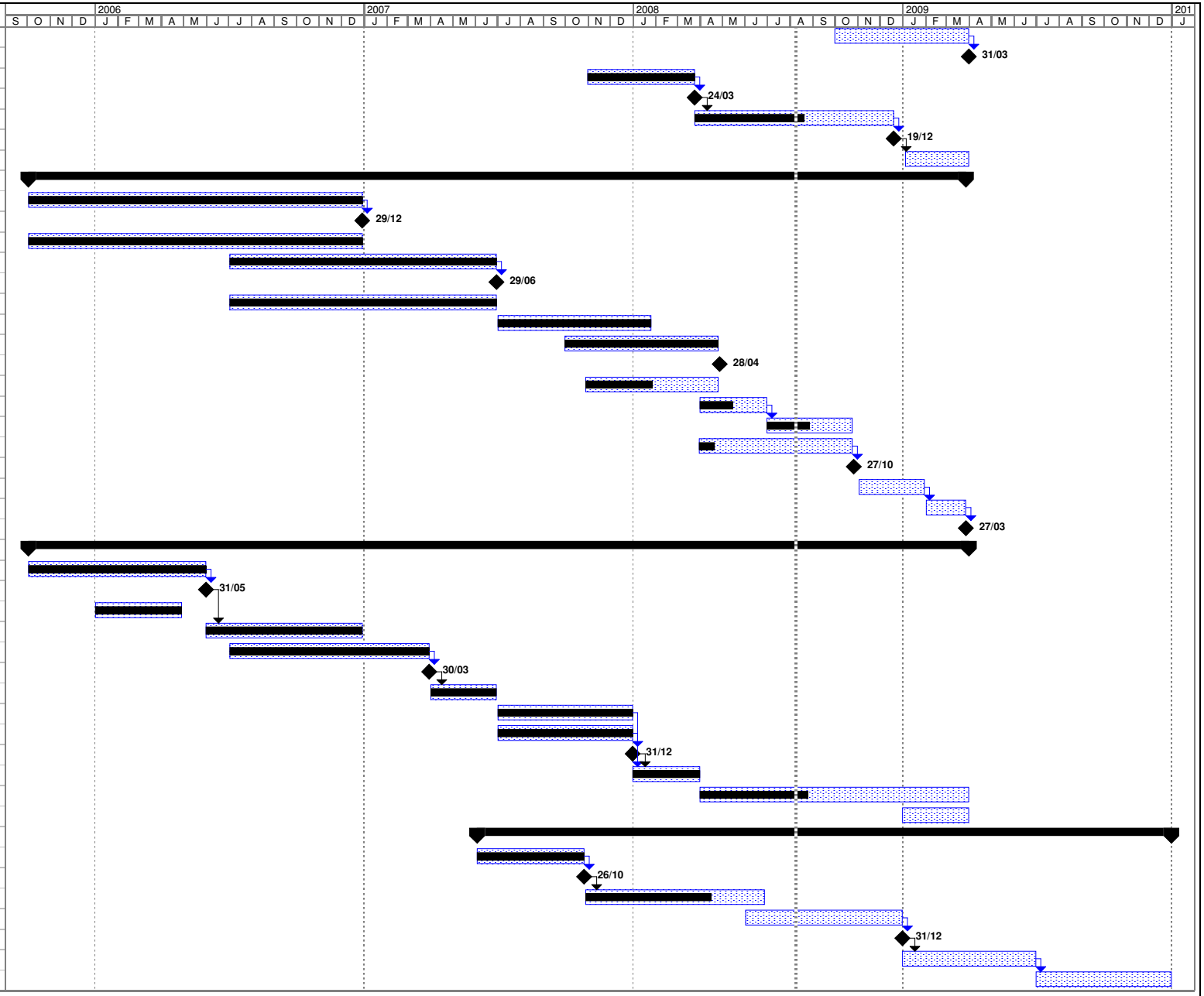
ID	Task Name
1	**CALICE WP2 - M. Wing (UCL)**
2	**Readout of prototype VFE ASICs**
3	*Firmware development for multi-chip tests*
4	*Multichip tests*
5	**Study of data paths over 1.5m slab**
6	Preliminary design study and preparation
7	Test Panel 0 design, fabrication and commissioning
8	FE board 0 design, fabrication and commissioning
9	Test bench 0 hardware ready and commissioned
10	Test bench 0 + host PC tests and measurements
11	Results analysis concepts definition for phase 1
12	Concepts established for 1.5m data path
13	Test panel 1 design and fabrication
14	Test bench 1 hardware ready and complete
15	Test panel 1 measurement programme
16	Test panel 1 complete
17	Define DIF-LDA protocol
18	DIF hardware design, fabrication and commissioning
19	DIF firmware - minimal version
20	DIF completed
21	Intermediate board hardware and commissioning
22	DIF firmware - final version
23	ECAL DIF available for test beams
24	System integration
25	**DAQ Networking**
26	FPGA to 1 Gig ethernet firmware development
27	FPGA 1 Gig Ethernet MAC firmware complete
28	1Gb data transfer tests
29	1Gb FPGA to multiple destination network tests
30	Report on FPGA ethernet work
31	Generic data source development
32	Re-package generic input data as ethernet
33	*Multi-port gigabit firmware development*
34	*Multi-port gigabit network tests*
35	*10Gb hardware development*
36	*10Gb tests*
37	*Network integration with electronics*
38	*Report on 10Gb performance*
39	*Networking tests with FPGA data source*
40	Survey of optical switches available
41	Acquire optical switch
42	Build network test rig using optical switch
43	Evaluate network performance
44	Re-evaluate performance with switching
45	Demonstrate optically switched network
46	Build busy signal
47	Develop trigger interface



Project: WP2
Date: Fri 08/08/08

Task | Progress | Summary | External Tasks | Deadline
Split | Milestone | Project Summary | External Milestone

ID		Task Name
48		Develop automatic switching system
49		Delivery of busy system
50	✓	LDA low-level firmware development
51	✓	LDA-DIF link operational at electrical level
52		LDA high-level firmware and integration
53		Working LDA with C&C and ODR
54		System integration
55		**Transport of configuration, clock and control data**
56	✓	Simulate radiation environment at FE
57	✓	Present simulation results
58	✓	Literature search for expected problems
59	✓	Design prototype board and test system
60	✓	Make proposal for robust/flexible test system
61	✓	Define clock and trigger requirements
62	✓	Design/prototype lock extraction system
63	✓	Evaluate use of commercial hardware fanout
64		Demonstrate trigger (and C + C) fanout
65		Design required interfaces
66		Demonstrate system lock from data interface
67		Evaluate jitter
68		Build large system
69		Demonstrate workability from single trigger source
70		*Design remote configuration hardware*
71		*Expand hardware to multiple units*
72		*Demonstrate remote FGPA reset and reconfigure*
73		**Prototype off-detector receiver**
74	✓	Investigated latest PCI technology
75	✓	Buy PCI cards
76	✓	High level system design
77	✓	Produce prototype firmware
78	✓	Write system software
79	✓	Initial prototype complete
80	✓	Tests of initial prototype
81	✓	Enhancements - s/w to h/w for speed improvements
82	✓	Enhancements - data to pseudo-file format
83	✓	Initial system complete
84	✓	Tests of initial system
85		Build and test full-scale system
86		Integrate into EUDET tets module
87		**DAQ software**
88	✓	Define overall DAQ structure
89	✓	DAQ software choice
90		Interface to hardware
91		Software and run control development
92		Complete basic DAQ and run control
93		System integration
94		Test beam support



Project: WP2
Date: Fri 08/08/08

Task | Progress | Summary | External Tasks | Deadline
Split | Milestone | Project Summary | External Milestone