Readout electronics for the CALICE ECAL and tile HCAL

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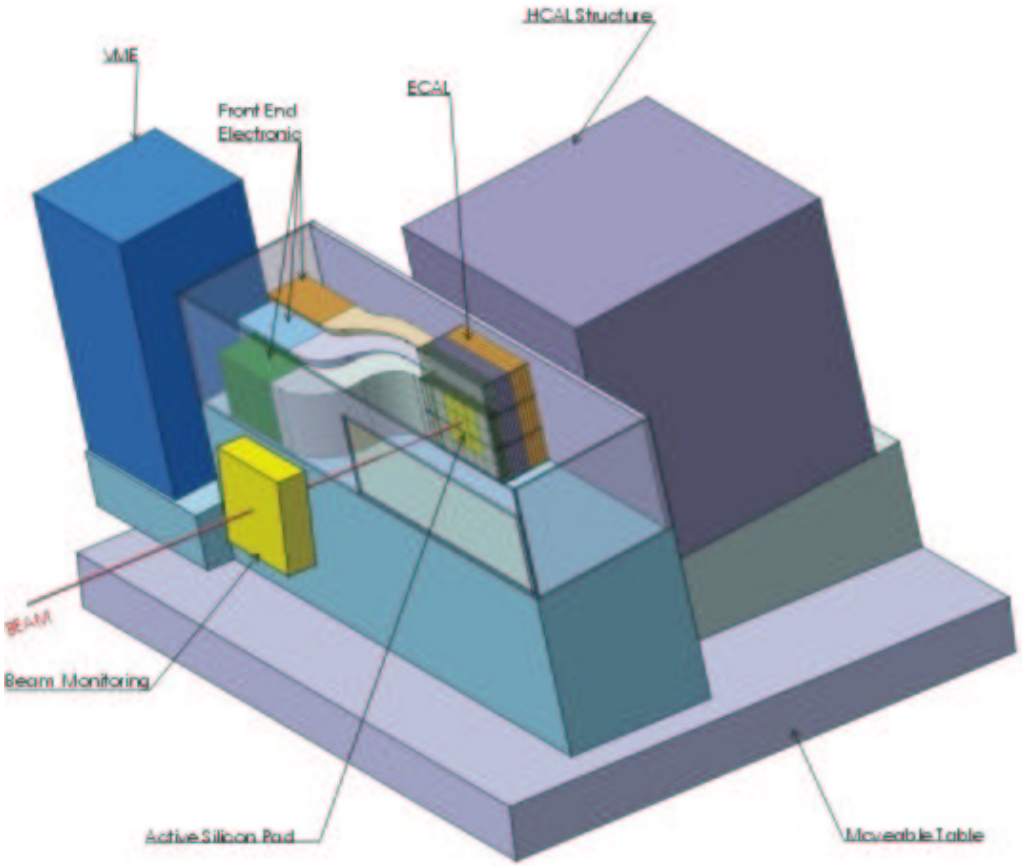
CALICE aims

Beam test with:

- Si/W ECAL
- Scintillating tile and/or digital HCAL

Data taking in 2004:

- $O(10^2)$ configurations (HCAL × beam energies × particle types × preshower × incident angle …)
- $O(10^6)$ events per configuration



ECAL readout electronics requirements

The UK is concentrating on the ECAL electronics. The requirements are:

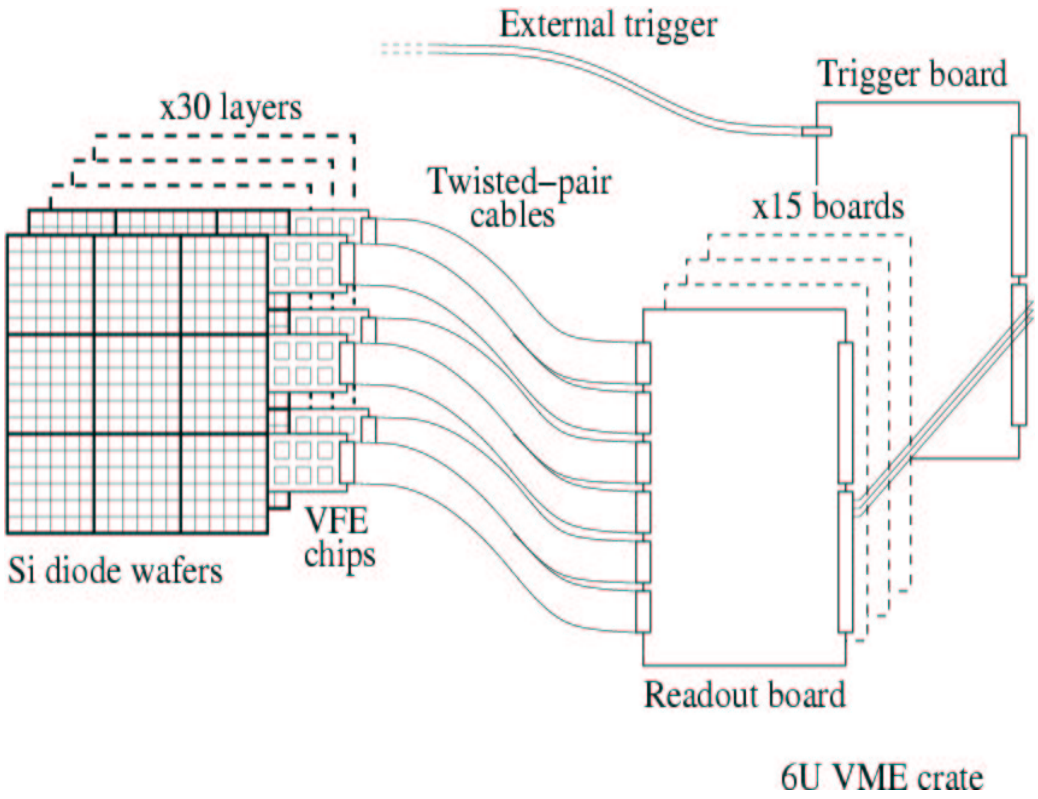
- Digitise data from all 9720 channels
  - Allow pedestal and noise measurements for all
- 14 bits dynamic range, 10 bits precision
  - Needed so digitisation noise does not limit precision
- 180 ns trigger latency, 10 ns trigger maximum jitter
  - Set by peaking time of CR-RC circuit in very-front-end chip
- O(100Hz) sustained event rate, O(1kHz) peak rate.
  - To acquire $O(10^8)$ events would take around one month of continuous data taking (more in reality).

Short timescale so system must be simple, flexible and robust

Overview of readout system

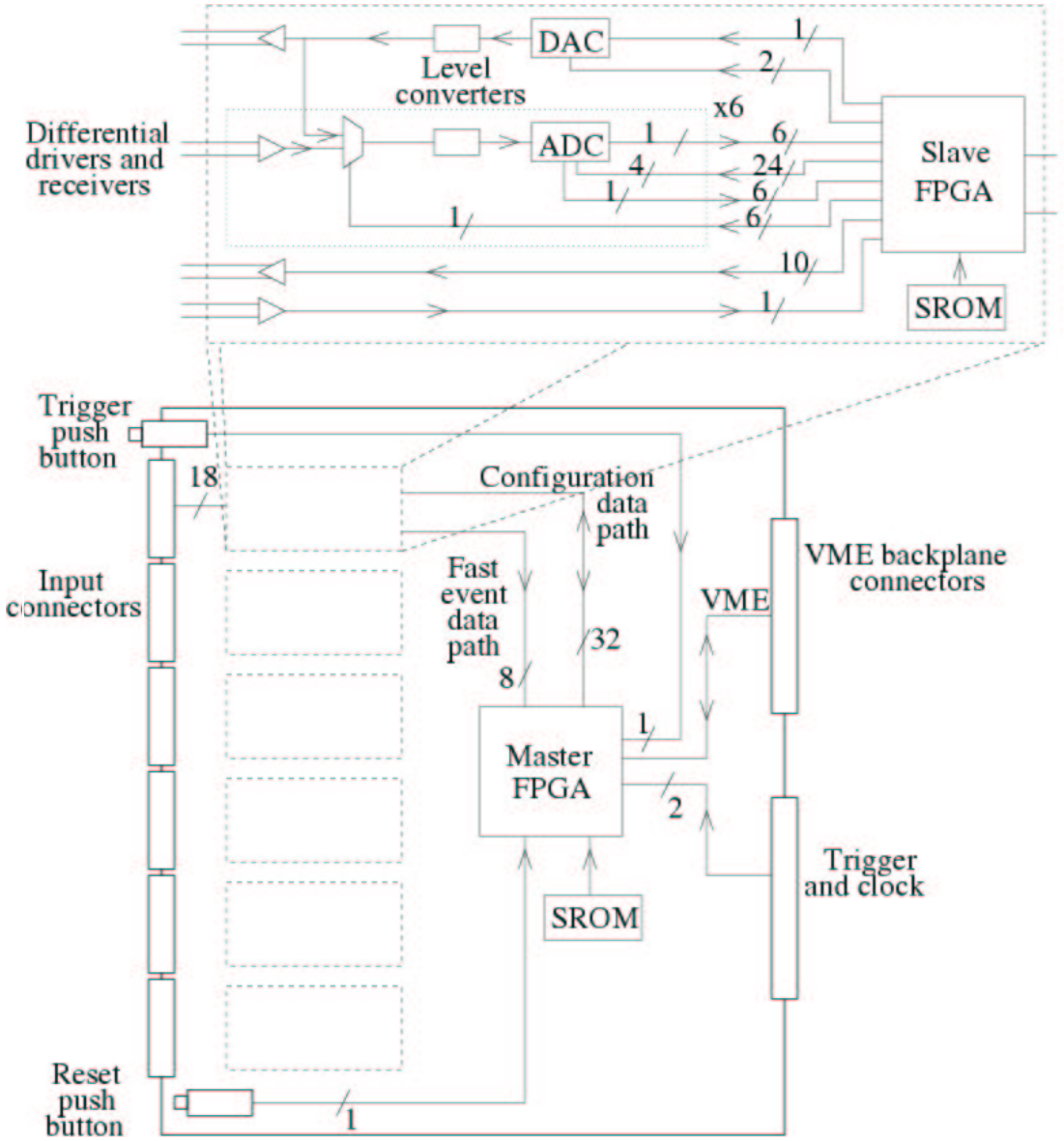
Need custom-built system as we found no available electronics which satisfied the requirements:

- A single VME crate
- 15 "readout boards"
  - Contains all front-end handling and digitisation electronics
  - Each handles two layers of ECAL = 648 channels
- 1 "trigger board"
  - Simple board to allow VME control
  - Trigger and clock distribution via customised VME backplane



Overview of readout board

- One master FPGA
  - Handles VME interface
  - Distributes clock and trigger
  - Distributes configuration data and collects event data
- Six slave FPGA's
  - One per cable, to handle cable control signals and ADC sampling
  - Each slave runs independently and contains identical firmware



Readout board features

- Very-front-end chip multiplexes 18 channels to one output line
  - 648 channels require 36 ADC's per readout board
- 16-bit, 500 kHz ADC's
  - Extra bits for robustness; allows some loss during range matching, etc.
  - Sample 18 channels plus overheads takes ≤ 50 μs or 5% of allowed 1ms event time at 1 kHz
  - Serial readout from ADC during sampling time; minimal extra delay
- Trigger distribution to very-front-end chips via programmable delay on 100 MHz clock
  - 10 ns steps; gives ≤ 0.15% offset from peak so compatible with 10 bits precision
- Built-in testability and flexibility
  - All signal and ADC timing configurable via VME
  - DAC output can loopback to ADC input
  - Configuration data can be played back through event data path

Data readout speeds

- VME access speed around 30 Mbytes/s
  - Readout board has no multiple event buffering capability
- For 1 kHz rate, need event sizes below 30 kBytes per event
  - Readout boards will do no zero suppression; 9270 channels gives 19 kBytes per event
  - HCAL's (both options) will be around 3 kBytes per event
  - Beam monitoring and trigger data less certain but will probably be around 1 kByte per event
- Total of 23 kBytes per event is tight but not impossible
  - Readout board VME interface will be optimised for speed; DMA transfers, asynchronous VME access, etc.
  - Consider using two VME crates in parallel; i.e. two VME-PCI bus converters to same PC. PCI bus rate is 80 MBytes/s so can double VME access speed. However, not clear if two bus converters will operate straightforwardly together in this mode.

Tile HCAL

Investigating use of ECAL readout boards for tile HCAL:

- 1500 channels, i.e. 15% of ECAL
  - 3 kBytes per event with no zero suppression
- 16-bit digitisation more than ample for requirements
- Very-front-end chip equivalent not yet specified
  - Peaking time, etc. not defined; configurable timing means differences from ECAL are easy to handle
  - Number of channels multiplexed per ADC not defined so number of extra readout boards needed unknown
  - Calibration circuit not defined
- ECAL and tile HCAL groups working together to come to a common solution for the cable I/O signals to the readout board
- Trigger distribution and DAQ simplified if common boards
  - But not possible for digital HCAL so need different solution there

Status and schedule

Proposal is not yet funded; being considered this fall

- Working on paper design up to that time
- No equipment funds needed before 2003

Schedule if approved:

- Finalise interfaces by October 2002
- Prototype design complete by January 2003
- Prototype fabricated by March 2003
- Prototype testing complete by June 2003
- Production redesign complete by July 2003
- Production fabrication complete by September 2003
- Production testing complete by January 2004