CALICE ECAL Readout Status

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For the CALICE-UK electronics group

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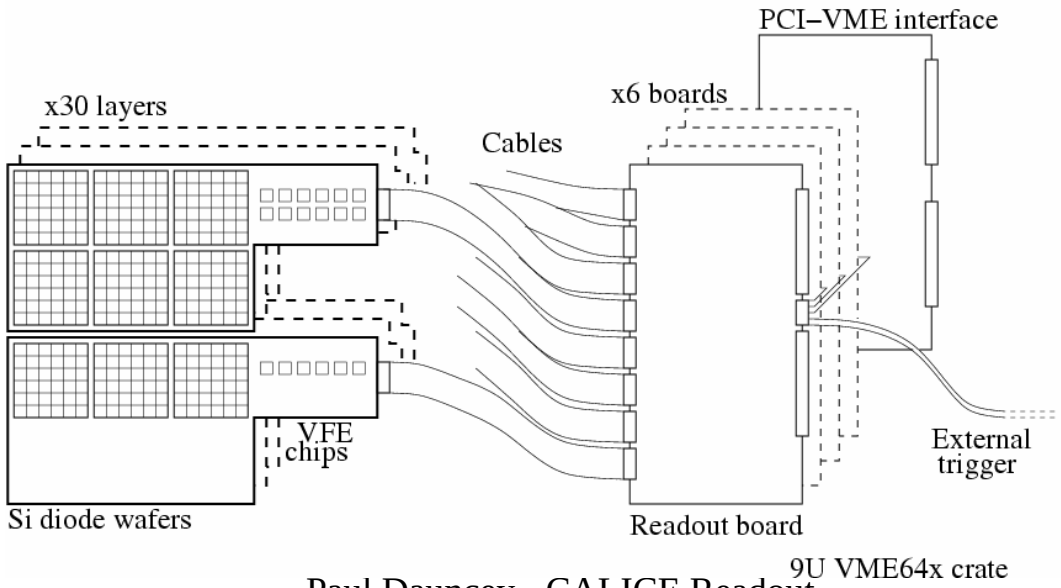
Readout electronics overview

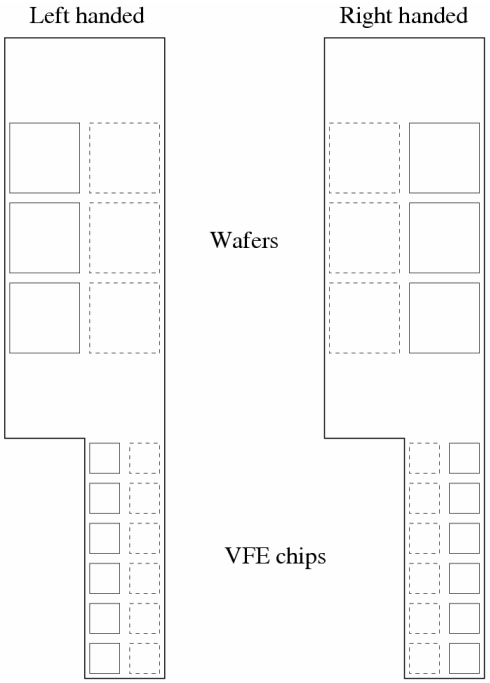
CALICE ECAL has 30 layers, 18×18 channels/layer, 9720 total

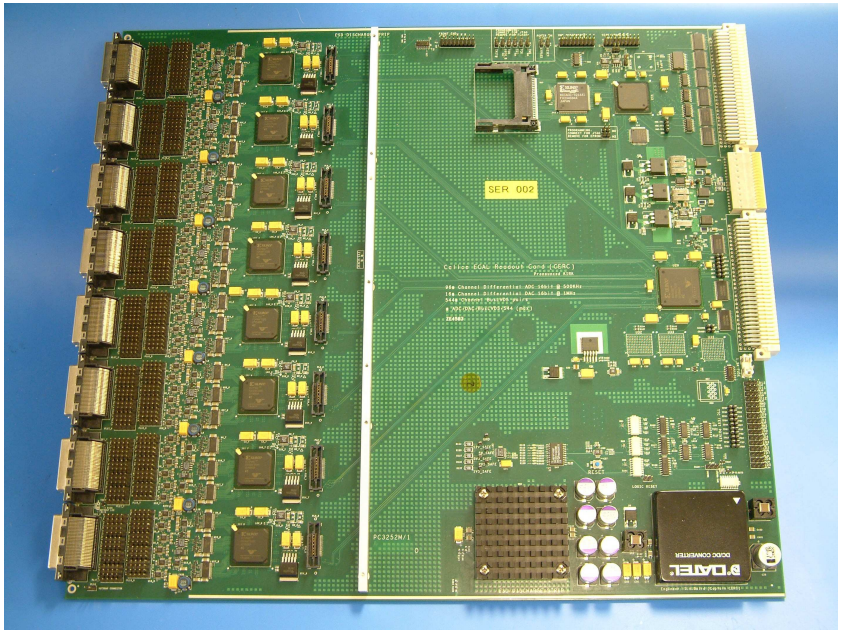
- Each gives analogue signal, 14-bit dynamic range required
- Very-front-end (VFE) ASIC (FLC_PHY from LAL-Orsay) multiplexes 18 channels to one output line
- VFE-PCB handles up to 12 VFEs (216 channels)
- Cables from VFE-PCBs go directly to UK VME readout boards, called Calice Ecal Readout Cards (CERCs)



Prototype verification tests

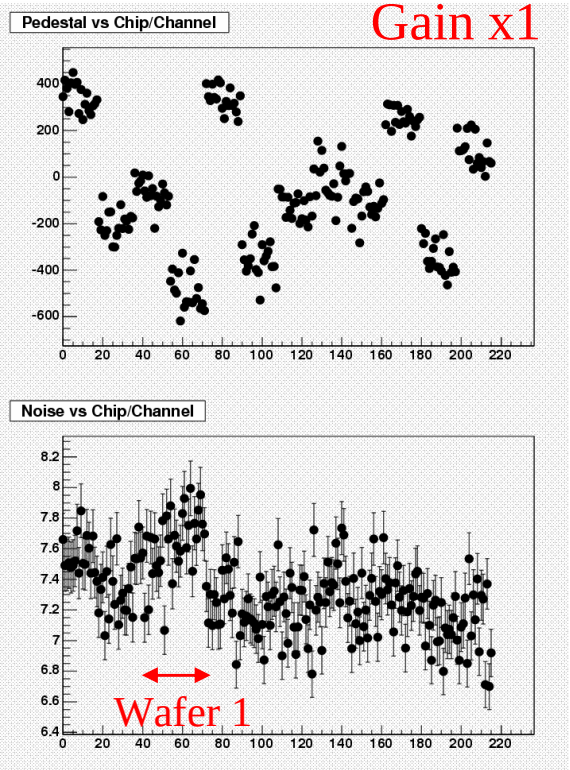
- Talk will show results of summer tests
  - To release designs of VFE and CERC for production
- Orsay VFE PCB V2_2 boards
  - Using VFE chip FLC_PHY3
  - Preproduction version
  - Three boards available
    - One each full, left-handed, right-handed
- CERC UK readout boards
  - Prototype version
  - Fully populated

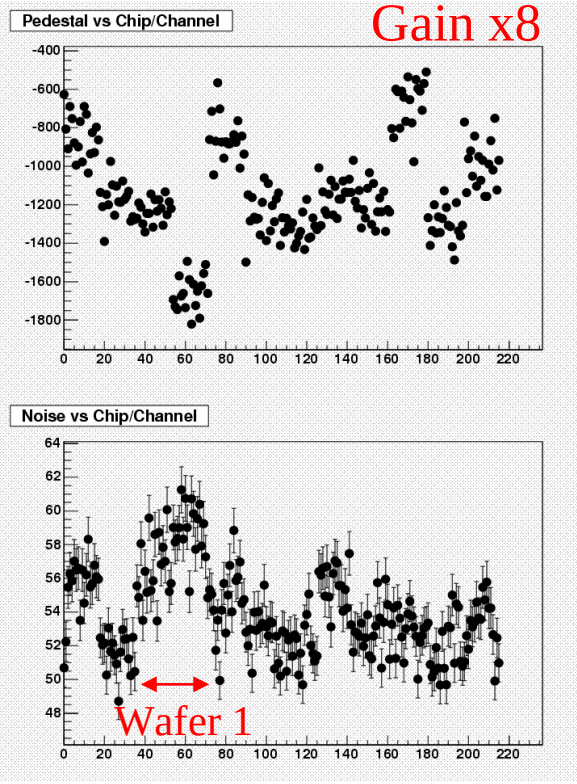




Noise tests

- Software selectable gain on VFE PCBs; ×1 or ×8
- Full PCB has 6 wafers mounted; wafer 1 does not deplete





Gain ×1 noise= 7.2 ADC counts, gain ×8 noise= 52 ADC counts

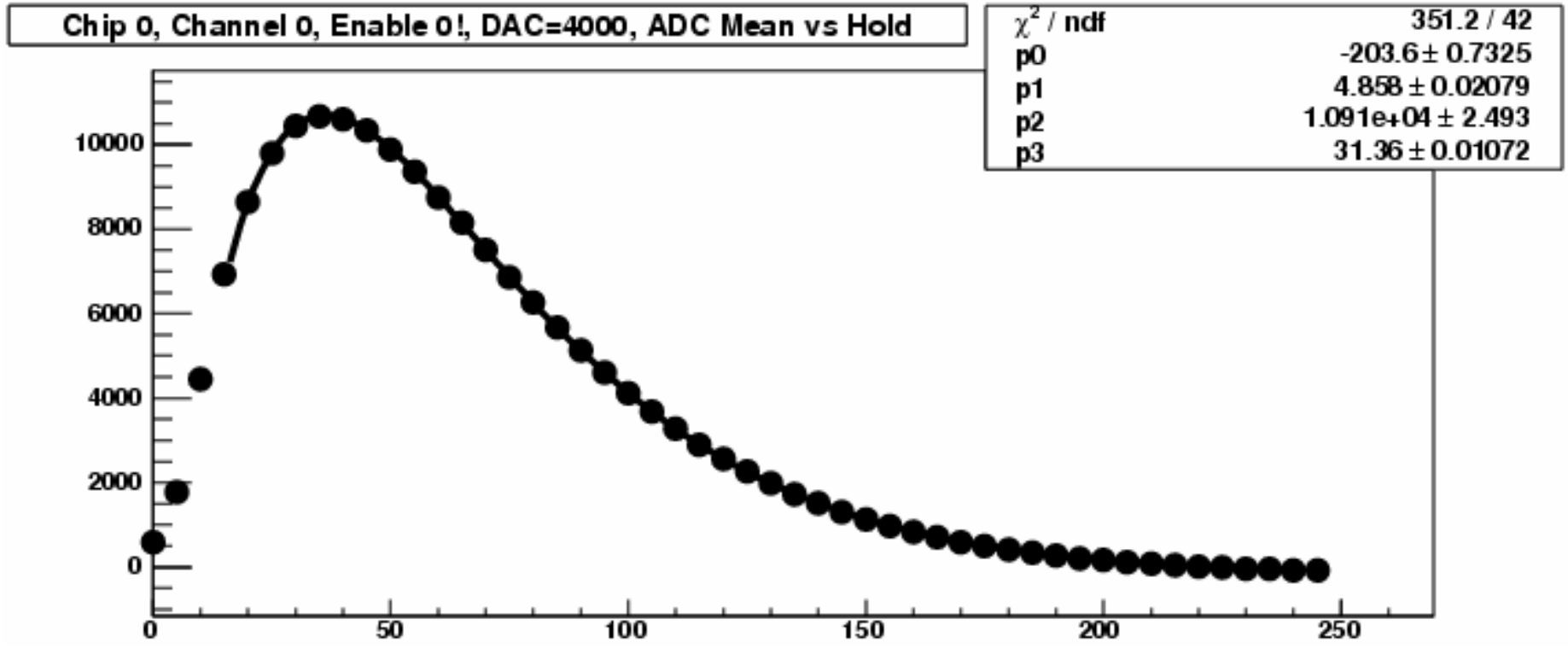
1 ADC count = 78μV. No obvious dead channels

Calibration with DAC

- Need to determining timing
  - Output signal is shaped by CR-RC circuit, shaping time ~200ns
  - Adjust timing so that sample-and-hold captures peak
  - Can change timing in software configuration; steps of 6.25ns
  - Scan sample-and-hold time and fit for peak
- With timing set correctly, scan DAC
  - From zero to channel saturation
  - 16-bit DAC, 1 DAC count = 20 μV
  - Determine mean and noise at each point
  - Fit for intercept and response
- Channels divided into 6 groups for DAC
  - Calibration can be enabled independently for each group
  - Look at response of non-enabled channels
  - Measure crosstalk

Timing determination

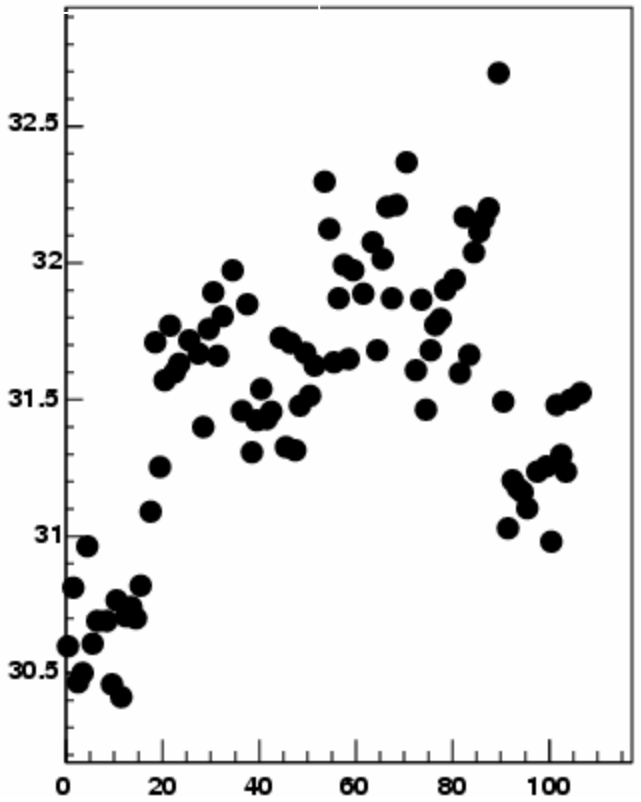
- Typical channel (first one on right-handed PCB), gain ×1
- Fit CR-RC xe^{1-x} shape to response (averaged over 19 events)
- Shaping time = p3 = 31.36 units × 6.25ns = 196 ns



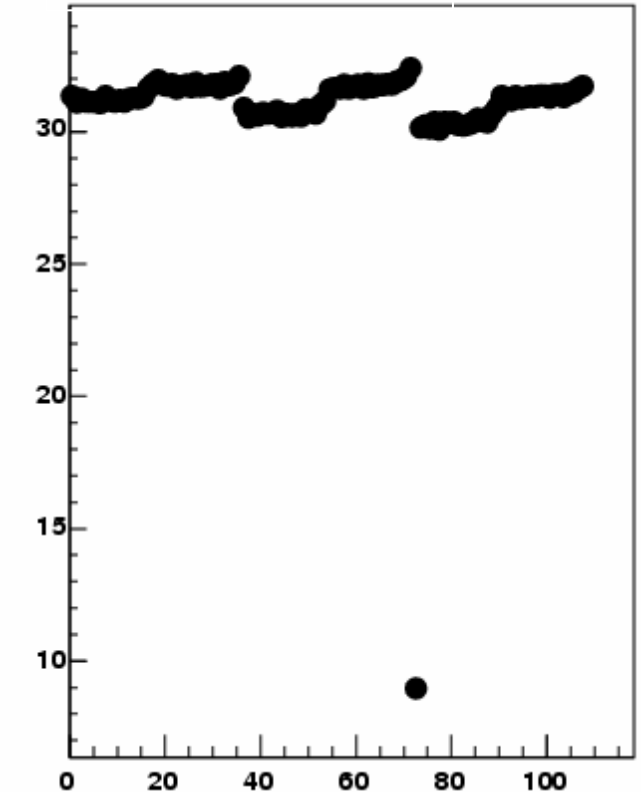
Timing determination (cont)

- Shaping times measured for left-handed and right-handed PCBs

Left-handed



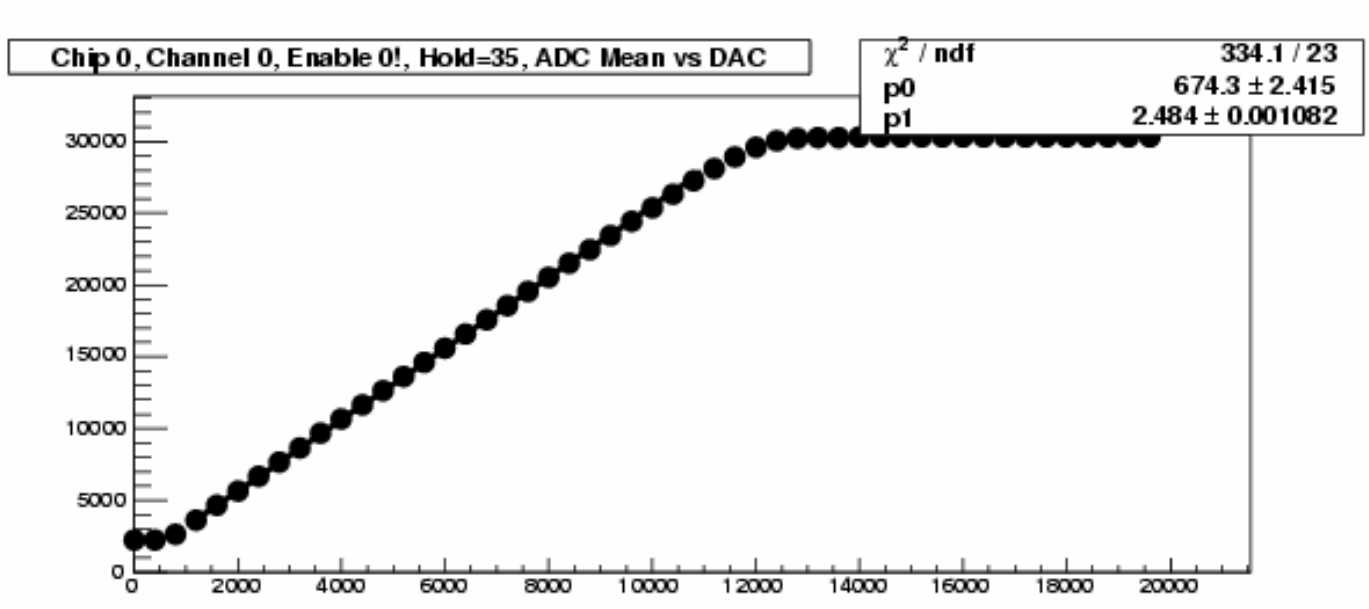
Right-handed



- Shaping times vary chip-to-chip; uniform to ±3%
- One unresponsive channel on right-handed PCB

DAC scan

- Typical channel (same as before), gain x1

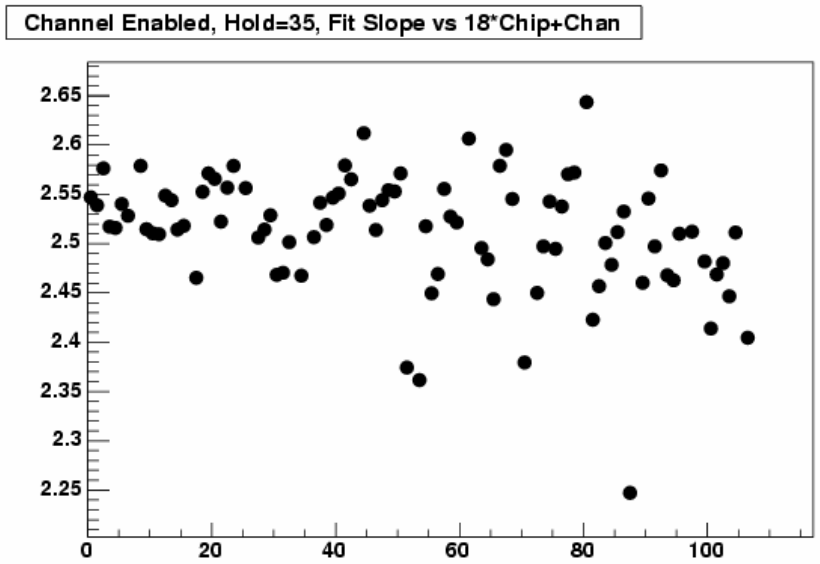


- Slope = 2.484 ADC counts/DAC count = 9.57V/V (expect 10)
- High end saturation from VFE-PCB preamplifier
  - Very close to top of ADC range (32k); well matched
- Low end saturation from CERC board; understood - due to DAC
  - Will be fixed in production version

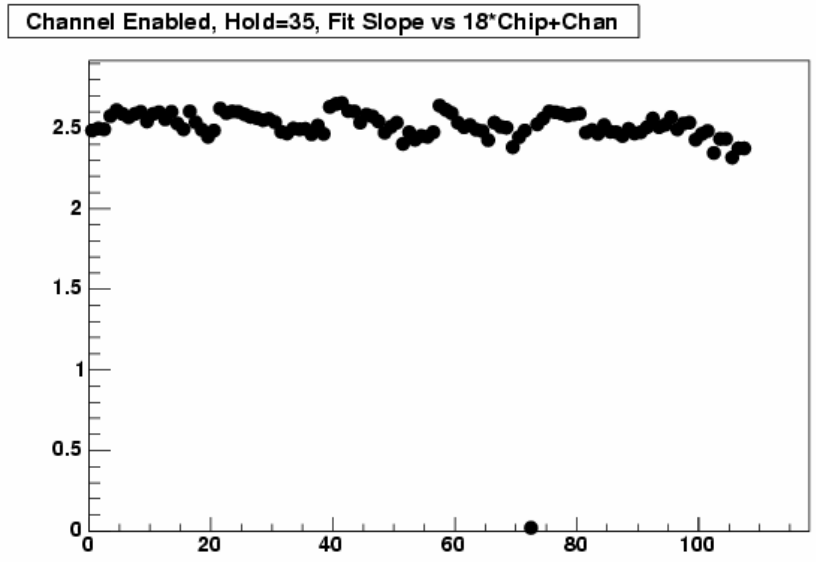
DAC scan (cont)

- Results for left-handed and right-handed PCBs

Left-handed



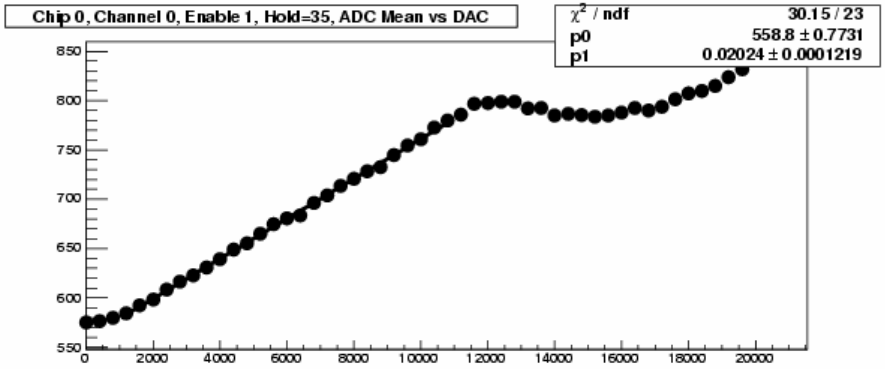
Right-handed

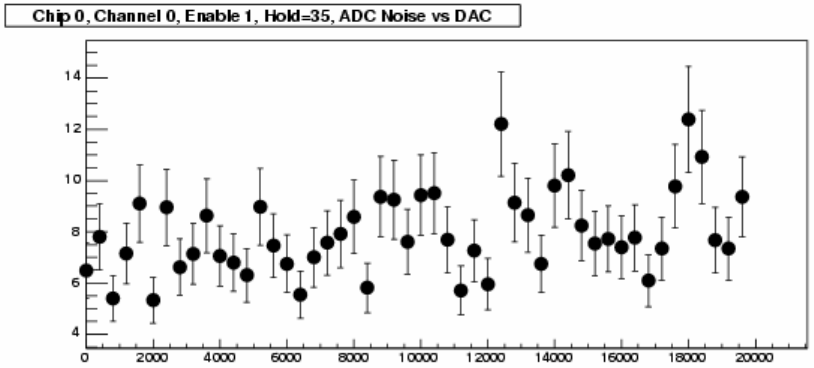


- Responses uniform to ±10%
- Same unresponsive channel on right-handed PCB shows up here

DAC crosstalk

- Typical non-enabled channel (same as before)



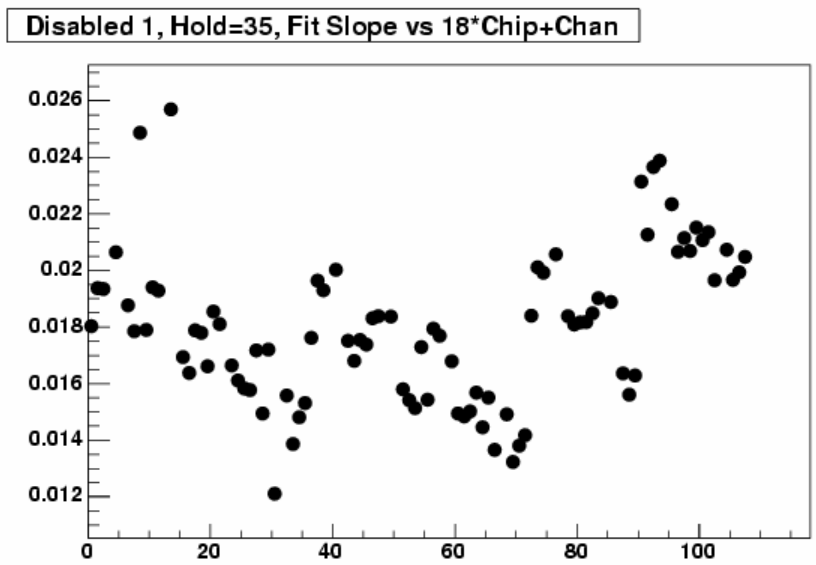


- Slope ~ 0.02 compared with ~ 2.5 for signal slope
- Crosstalk is less than 1% of signal
- Noise shows no significant increase

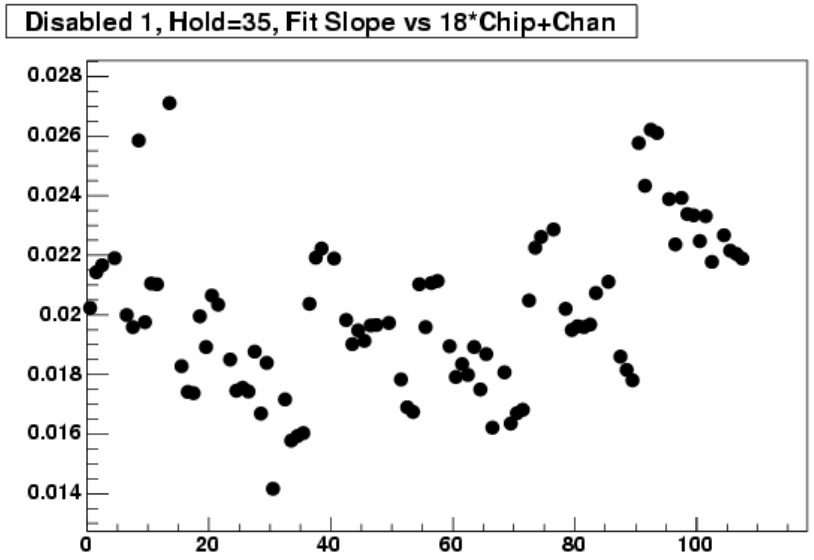
DAC crosstalk (cont)

- Six different combinations of non-enabled channels
- Typical results for left-handed and right-handed PCBs

Left-handed



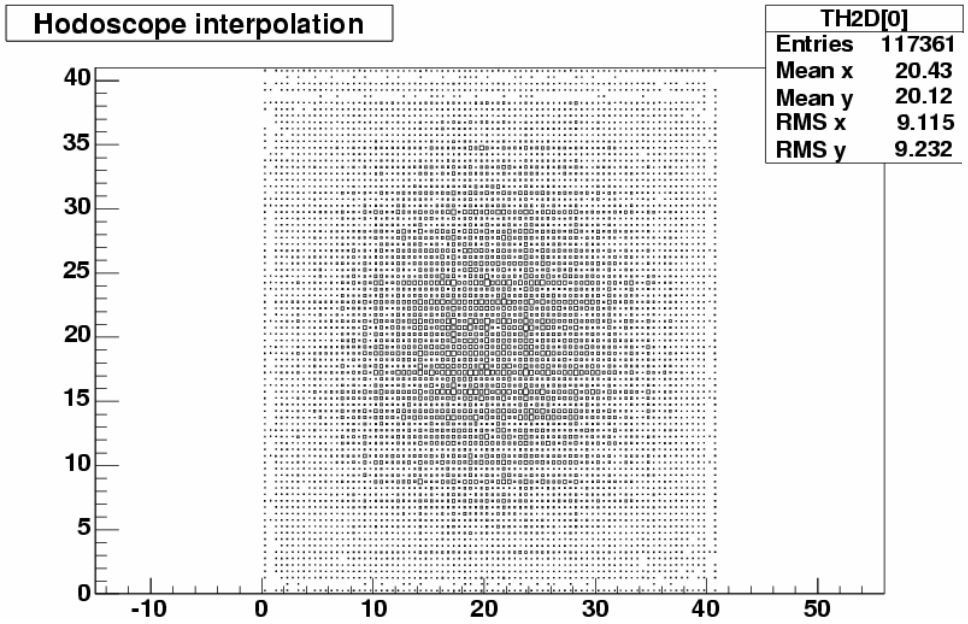
Right-handed

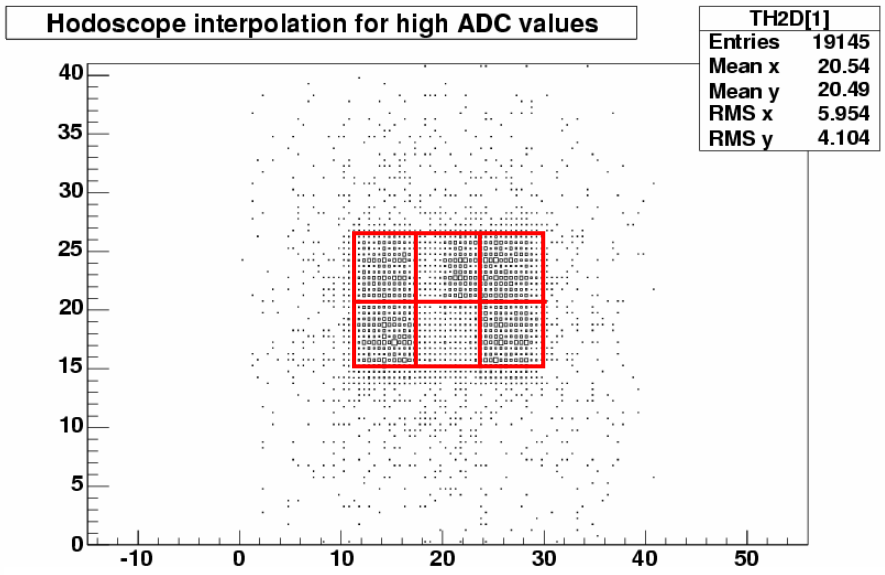


- Crosstalk uniform to ±25% for most enables
- A few channels show bigger crosstalk ~10% due to close tracking on VFE-PCB; can be reduced in production version

Cosmics run

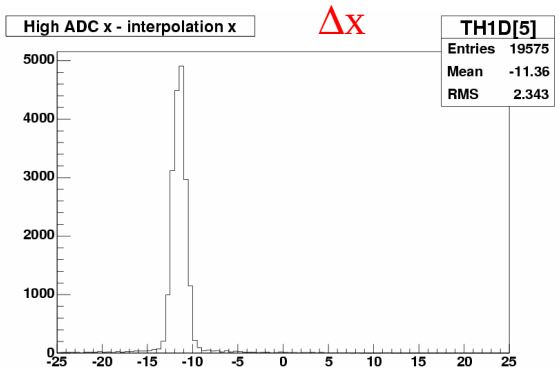
- Full PCB used in Ecole Polytechnique teststand, but…
  - Wafer 1 not depleted so no signal seen on it
  - Bad ADC on CERC for wafer 4; half the wafer had very high noise
- Ran over weekend 18-21 June
  - Total ~ 60 hours, 130k events; worked reliably throughout
  - Around 90% have unique track from scintillator hodoscope
  - Interpolate into plane of PCB; cut on any ADC value > 40 above pedestal

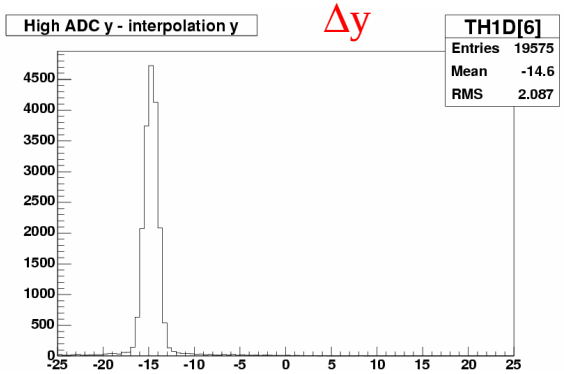




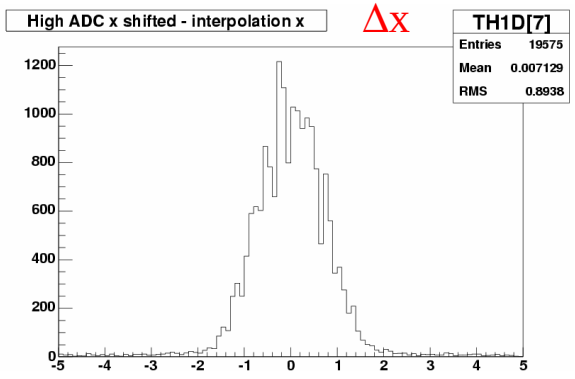
Cosmics alignment

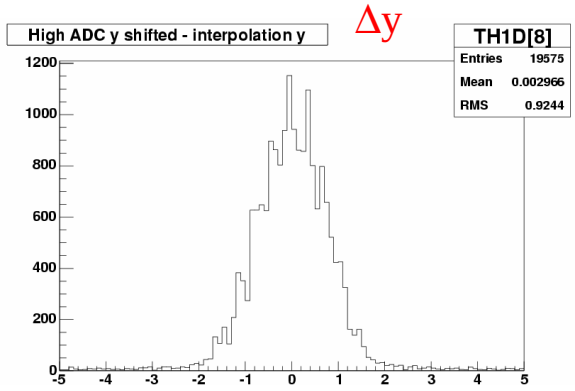
- Compare x and y scintillator interpolation with channel position





- Single peaks; proves no mis-wiring of channels or readout
- Hence, align coordinate systems to agree

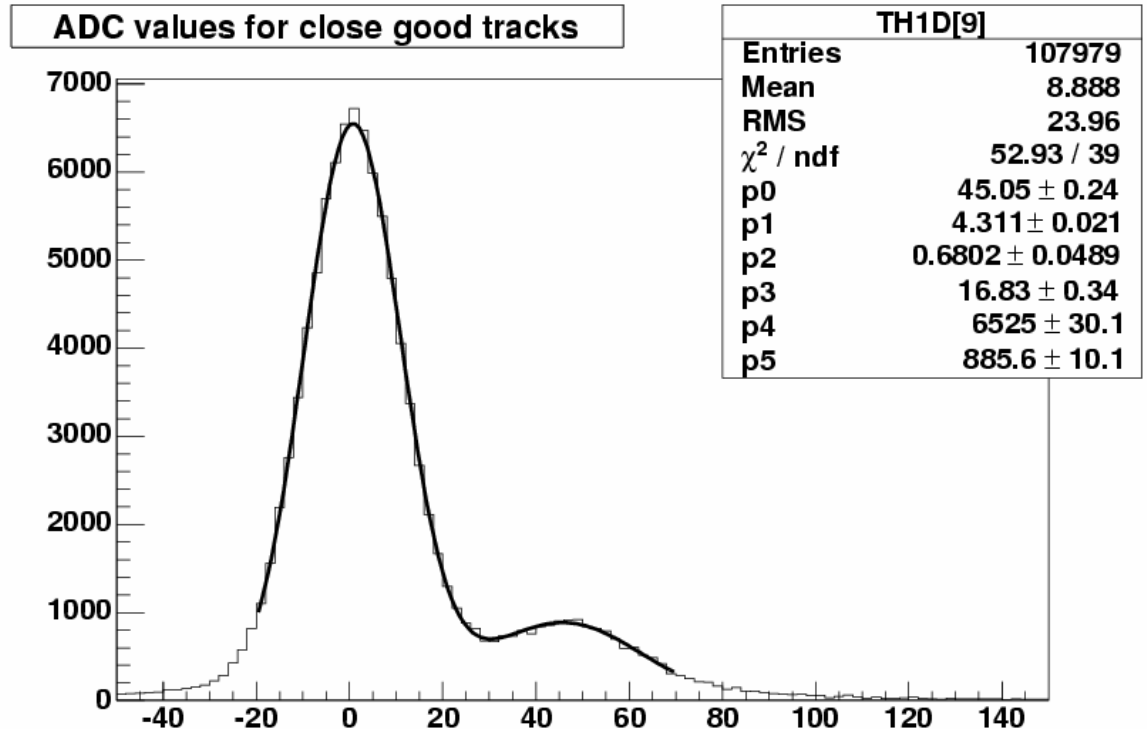




- Width of Δx and Δy distributions ~ 0.9cm

Cosmic signal response

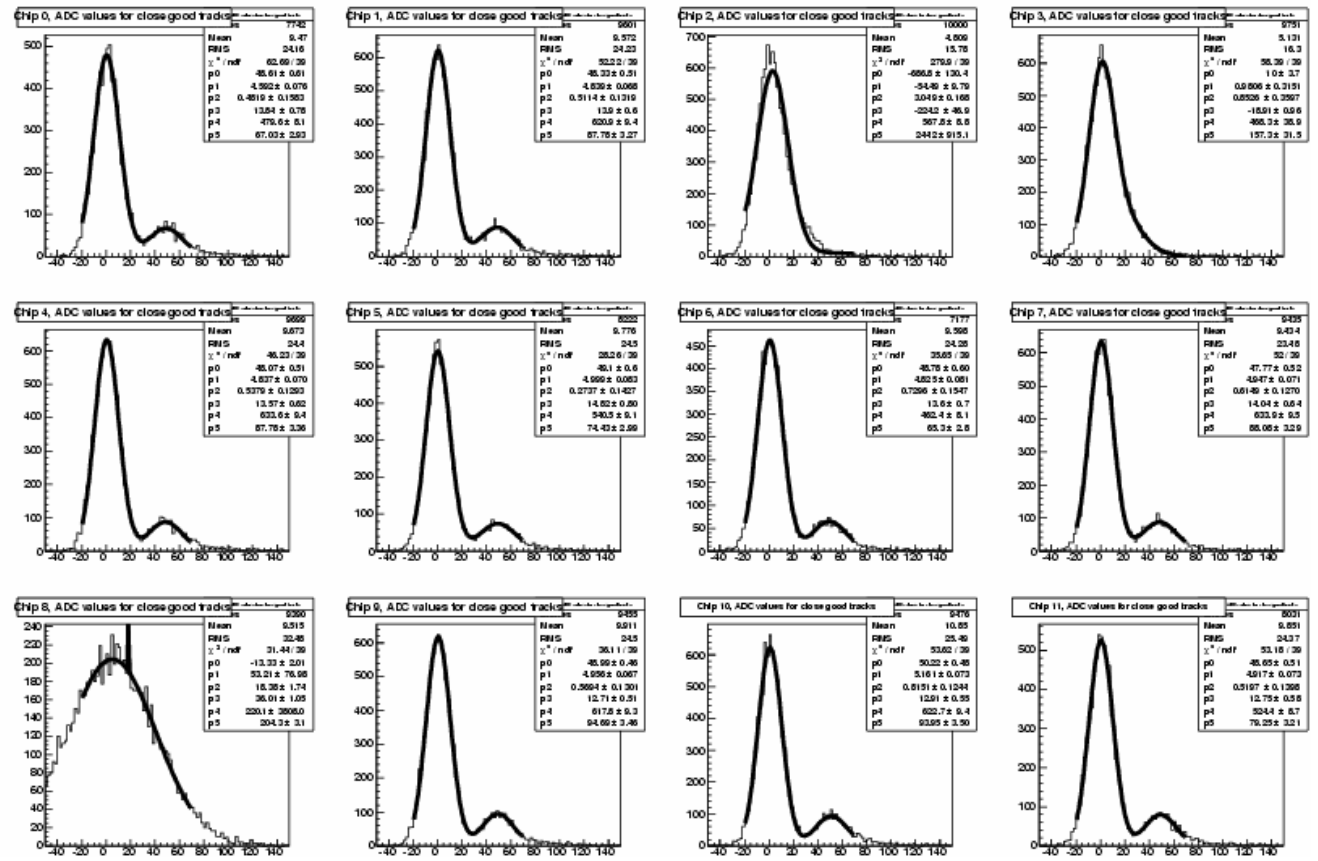
- Require interpolation within 0.9cm of pad centre
- All (good) channels combined



- Simple Gaussian fit gives signal peak at 45 ADC counts = 3.5mV
- But S/N = 4.3, i.e. noise is 10 counts, not 7 counts

Cosmic signal response (cont)

- Divide into separate chips
  - Wafer 1 is chips 2 and 3, bad ADC is chip 8



Chips 0-3

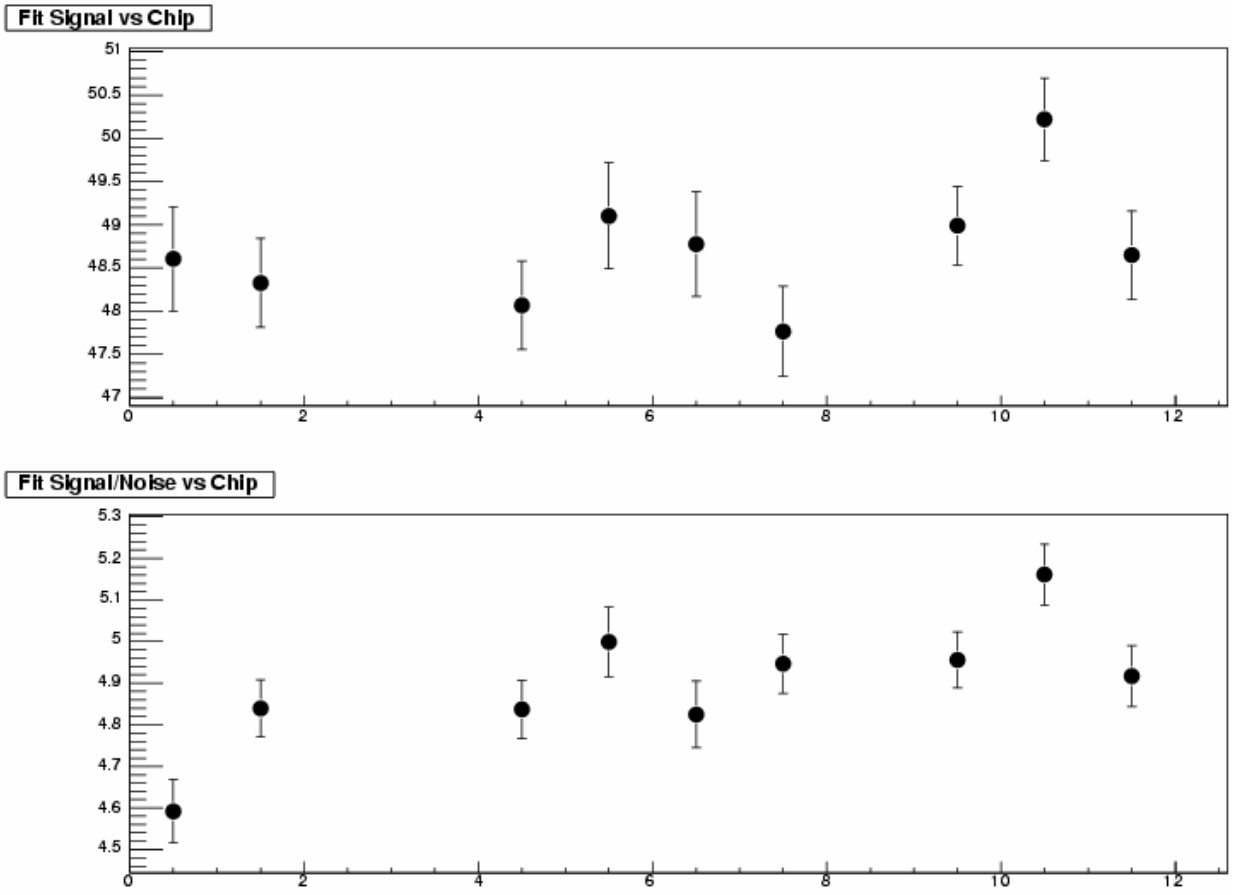
Chips 4-7

Chips 8-11

- Clear signal seen in all good wafers/chips

Cosmic signal response (cont)

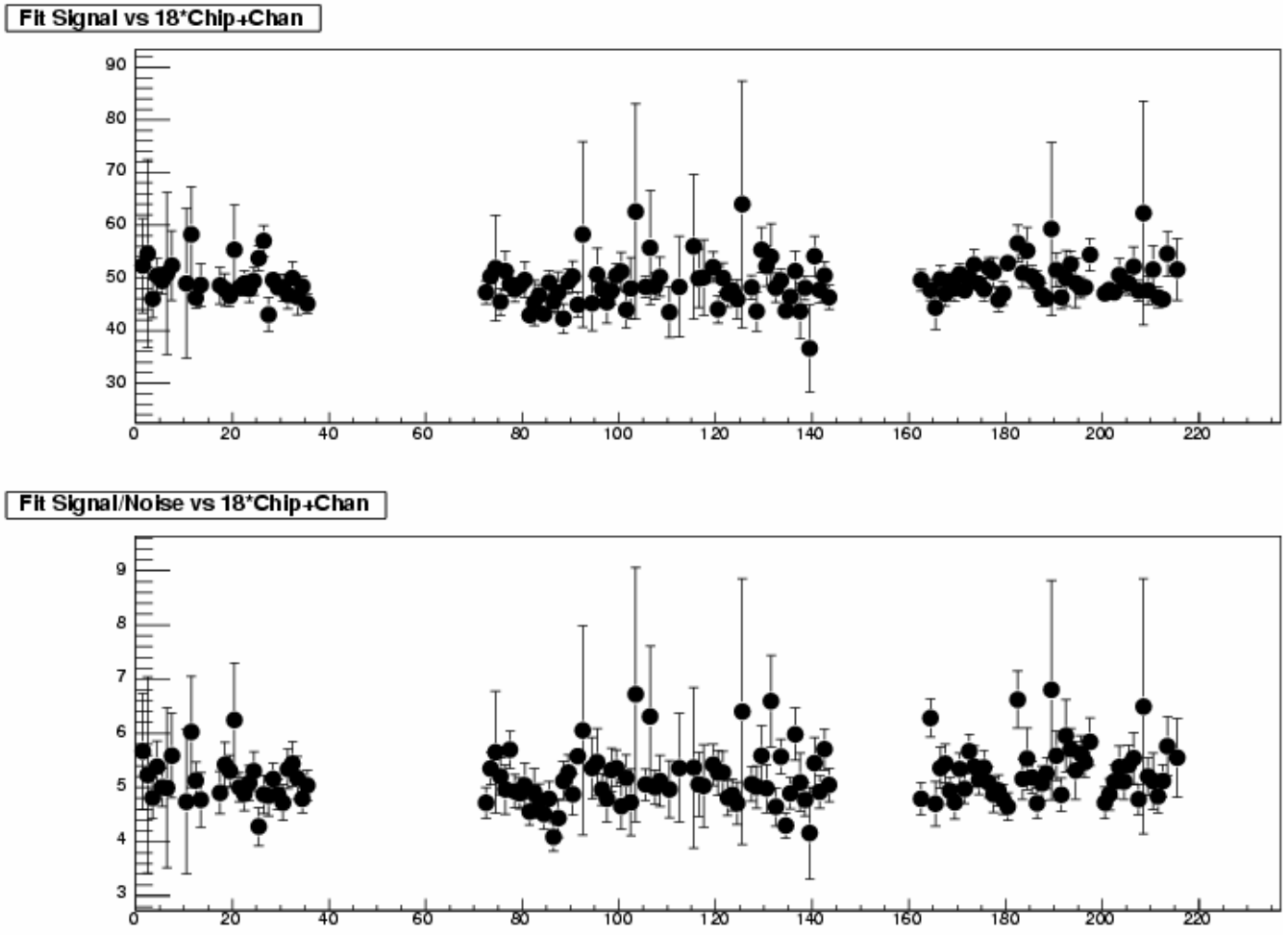
- Look at signal and S/N for good chips



- Both uniform to ± 3%
- Fit gives slightly higher signal ~ 49, and hence S/N ~ 4.9

Cosmic signal response (cont)

- Pushing the stats, look at signal and S/N for good channels



- No obvious bad channels…

Future plans

- Prototype tests completed successfully in June
  - Minor modifications for VFE-PCB and CERC identified
- VFE-PCB released for production in July
  - See talk by B. Bouquet
- CERC redesign was finalised in August
  - Production boards being sent out for fabrication next week
  - Three week turnaround; start testing by end of September
- ECAL system tests from October onwards
  - Initially at least 10 layers in cosmic teststand at Ecole Polytechnique
- DESY ECAL electron beam test from November onwards
  - Initially using first 10 layers
  - Build up over several months to full 30 layer ECAL
- Beam tests with HCAL(s) in hadron beams from 2005 onwards