Rutherford Appleton Laboratory
Particle Physics Department

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Tera-Pixel MAPS system for CALICE Si-W ECAL for ILC

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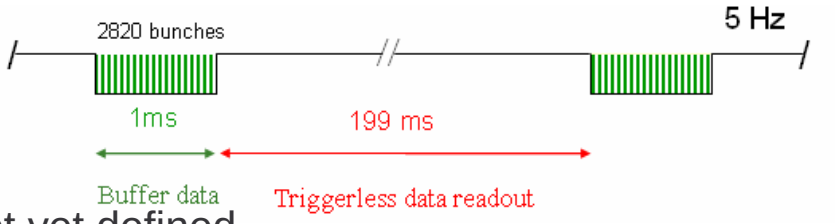
Siena 2006

Outline

- ILC Calice description
- CALICE MAPS Concept, design and simulation results
- Conclusions

ILC operation

TESLA 500GeV



- Exact ICL beam timing parameters not yet defined
  - Assume close to previous (“TESLA”) design
  - Beams collide rapidly within a quick burst (“train”)
  - Long dead time between trains
- Worst case timing assumption as follows
  - Beam collision rate within train = 6.7 MHz, i.e. 150ns between collisions
  - Number of collisions within train = 14000, i.e. train is 2ms long
  - Train rate = 10Hz, i.e. 100ms between trains; 2% duty cycle
- Rate of signals
  - ILC is not like LHC; rate of physics processes is small
  - Most collisions give nothing, but when reaction does happen, many adjacent channels will be hit
  - Expected rate not very well known; needs detailed simulation modeling
  - Assume average ~10^{-6} hits/pixel/crossing, which is ~0.005 hits/pixel/train

CALICE ECAL description

- CALICE has a baseline ECAL design
  - Sampling calorimeter, alternating thick conversion layers (tungsten) and thin measurement layers (silicon)
  - Around 2m radius, 4m long, 30 layers W and Si, total Si area including endcaps ~ $2\times10^7 cm^2$
  - Silicon sensor detectors in baseline are diode pads
  - Pad readout is analogue signal; digitized by Very Front End (VFE) ASIC mounted next to sensor
  - Average dissipated power 1 $\mu W/mm^2$
  - Pad size between 1.0×1.0 and $0.5\times0.5 cm^2$; total number of pads around 20 - 80M
- Mechanical structure
  - Half of tungsten sheets embedded in carbon fiber structure
  - Other half of tungsten sandwiched between two PCBs each holding one layer of silicon detector wafers
  - Whole sandwich inserted into slots in carbon fiber structure
  - Sensitive silicon layers are on PCBs ~1.5m long × 30cm wide

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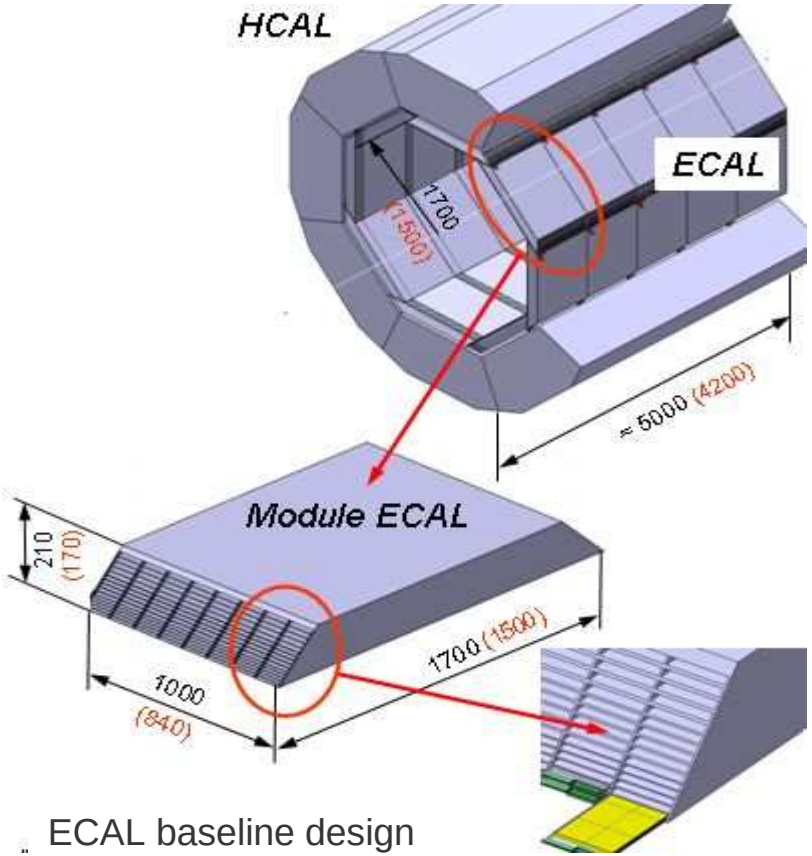
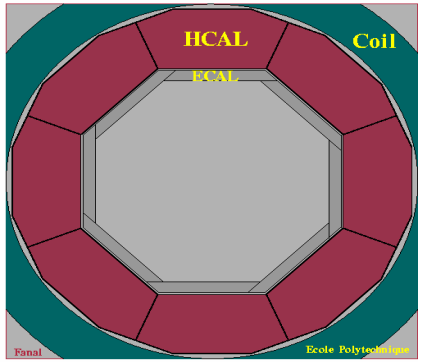
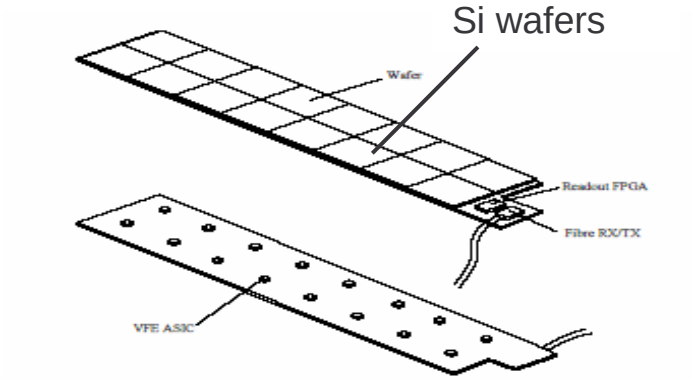
CALICE ECAL description



ECAL baseline design



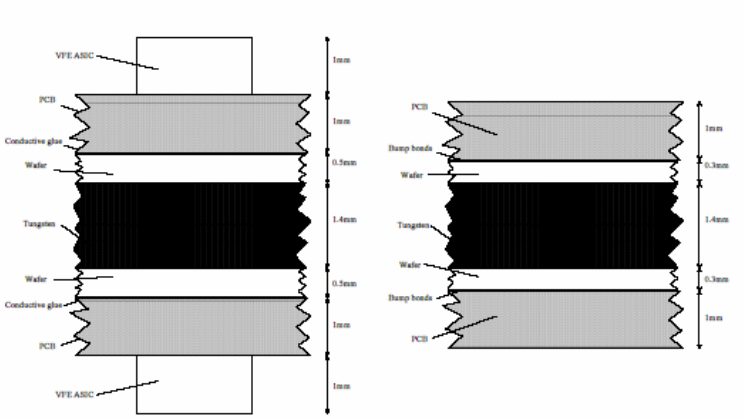


CALICE MAPS concept

q Baseline design largely unaffected by use of MAPS instead of diode pads

q Potential benefits include:

- Reduced PCB section for MAPS → Decrease in Molière radius → Increased resolution
- Increased surface for thermal dissipation
- Less sensitivity to SEU
- Cost saving (CMOS standard process vs. high resistivity Si for producing 2×10^7 cm^2 and/or overall more compact detector system)
- Simplified assembly (single sides PCB, no need for grounding substrate)



Diode pad PCB, with VFE (left) and without (right)

CALICE MAPS design

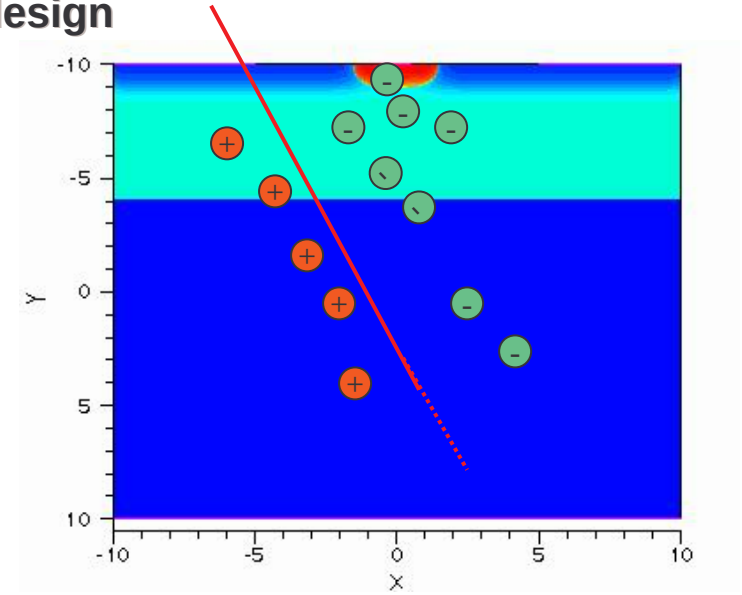
- Additional potential benefits arising from dividing wafer into small pixels so to have low probability of more than one particle going through each pixel.
- Discrimination of single MIP allows binary readout. High granularity improves jet resolution or reduces number of layers (thus cost) for the same resolution.
- With around 100 particles/mm^2 ~ 1 % probability of double hit implies pixel size of ~ 40 × 40μm^2
- Current design with 50 × 50μm^2 pixel
- Total number of pixel for ECAL around 8 × 10^{11} pixels ⟹ Tera-pixel system
- Record collision number each time hit exceeding threshold (timestamp stored in memory on sensor)
- Timestamps read out in between trains

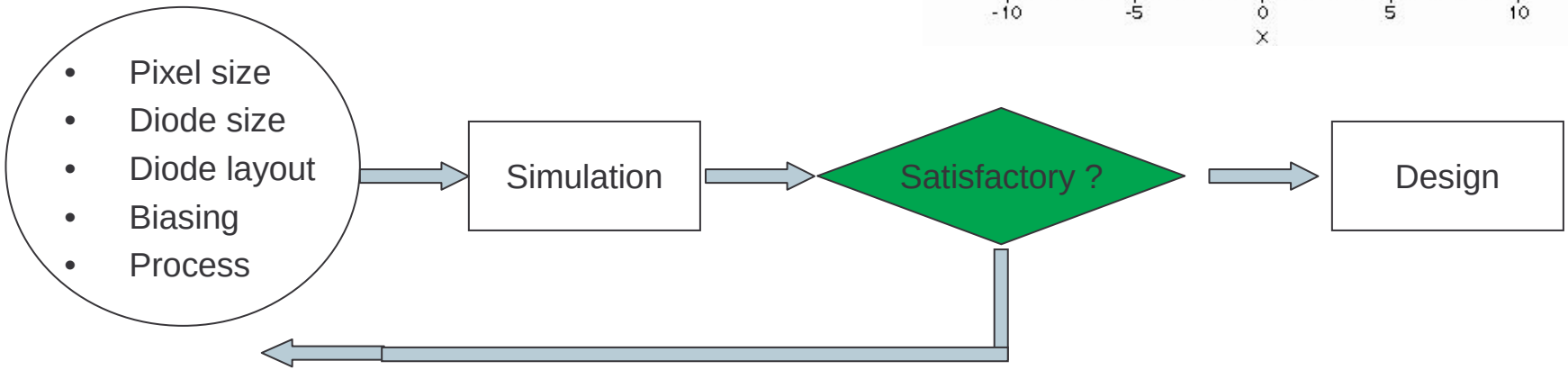
CALICE MAPS design

- First prototype designed in CIS 0.18 μm process will be submitted January 2007
- Different pixel architectures included in the first prototype
- Includes faulty pixels masking, variable threshold
- Data rate of pixels dominated by noise
- High threshold reduces false hits and crosstalk
- 'Optimal' pixel layout and topology essential to guarantee good S/N thus possibility of using high threshold

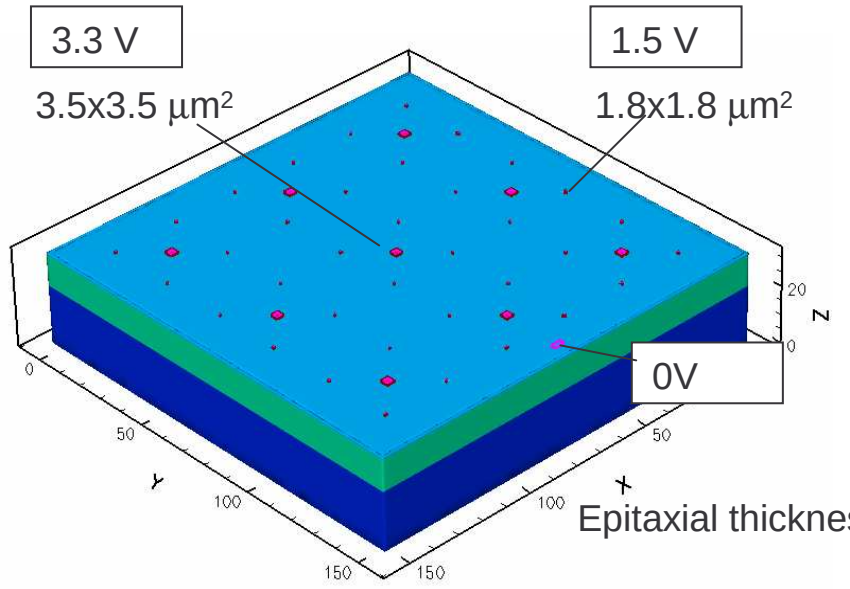
CALICE MAPS design

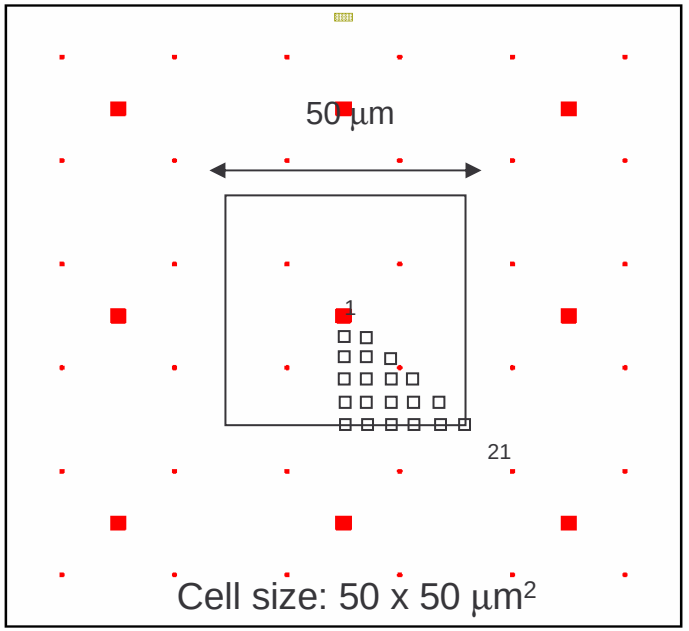
- q Pixel layout optimization
- • Maximization of signal
- • Minimization of charge sharing (crosstalk)
- • Collection time
- q Large phase space



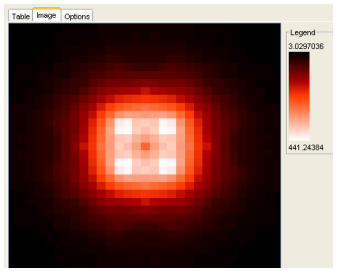


CALICE MAPS design - pixel simulation -

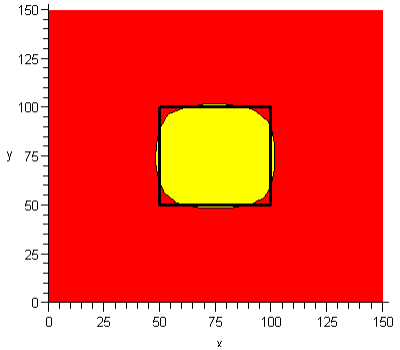




- 21 hits simulated, 5 µm pitch
- 121 extrapolated hits / pixel
- 961 extrapolated hits / cell



CALICE MAPS design - pixel simulation -



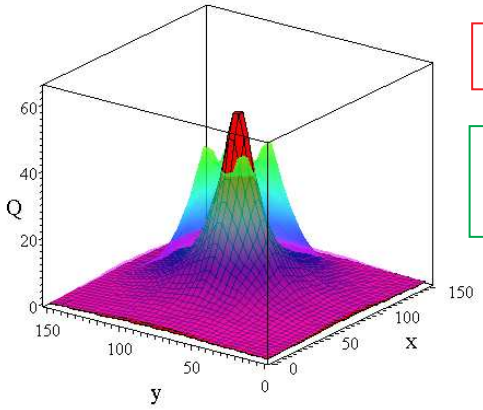
Comparator's threshold: 250 e^-

Charge sharing reduction with comparator's threshold

Σ diodes Collected charge vs (x,y)

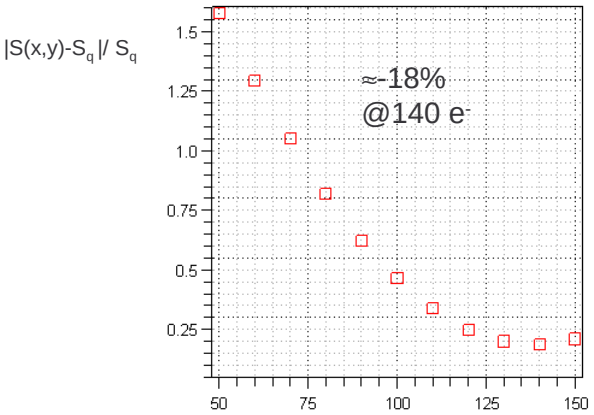
Bias conditions
- Diode : 1.5V fixed
- Nwell: 3.3V
- Pwell: 0V
- Subs: float
- T = 300 K

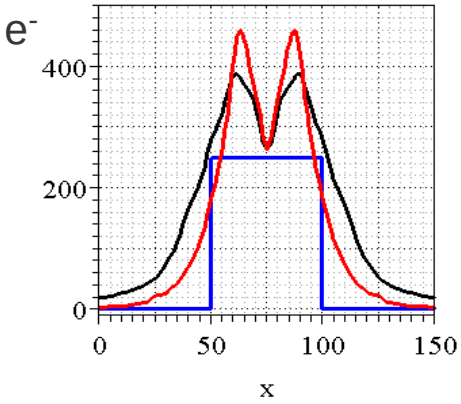
CALICE MAPS design - pixel simulation -

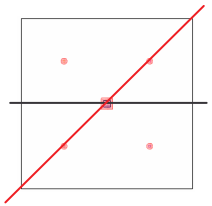


Q lost in NWell

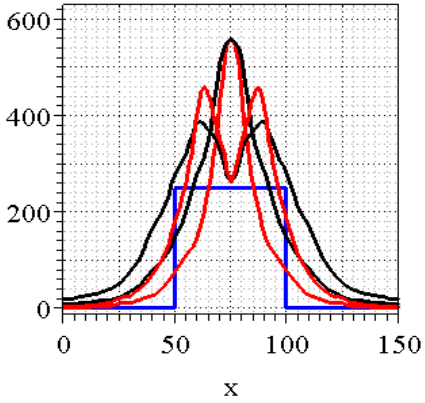
Q collected by diodes



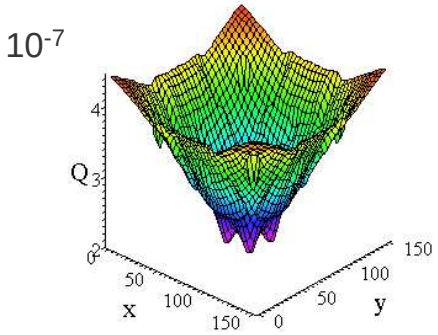




Central cell $Q_{coll}(x,y)$ sample

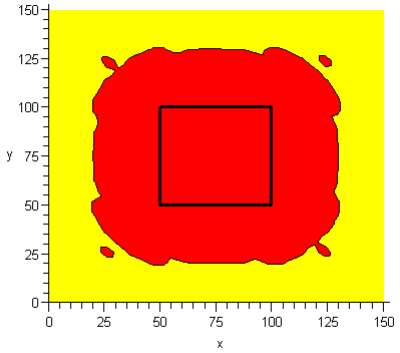


CALICE MAPS design - pixel simulation -



Diode charge collection time (x,y)

350 ns



q Collection time ~ 250 ns for pixel coverage

q Needs further optimization

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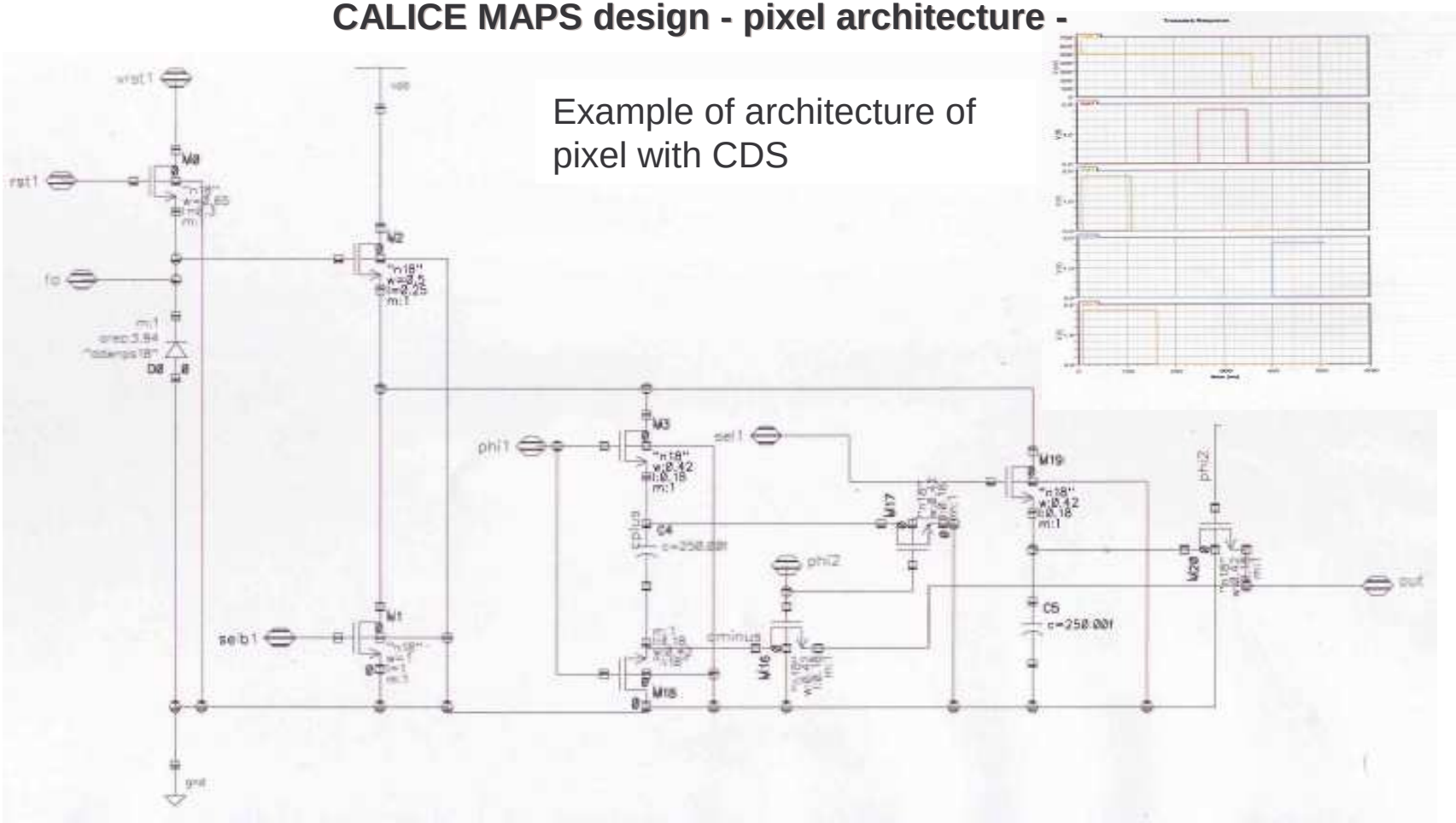
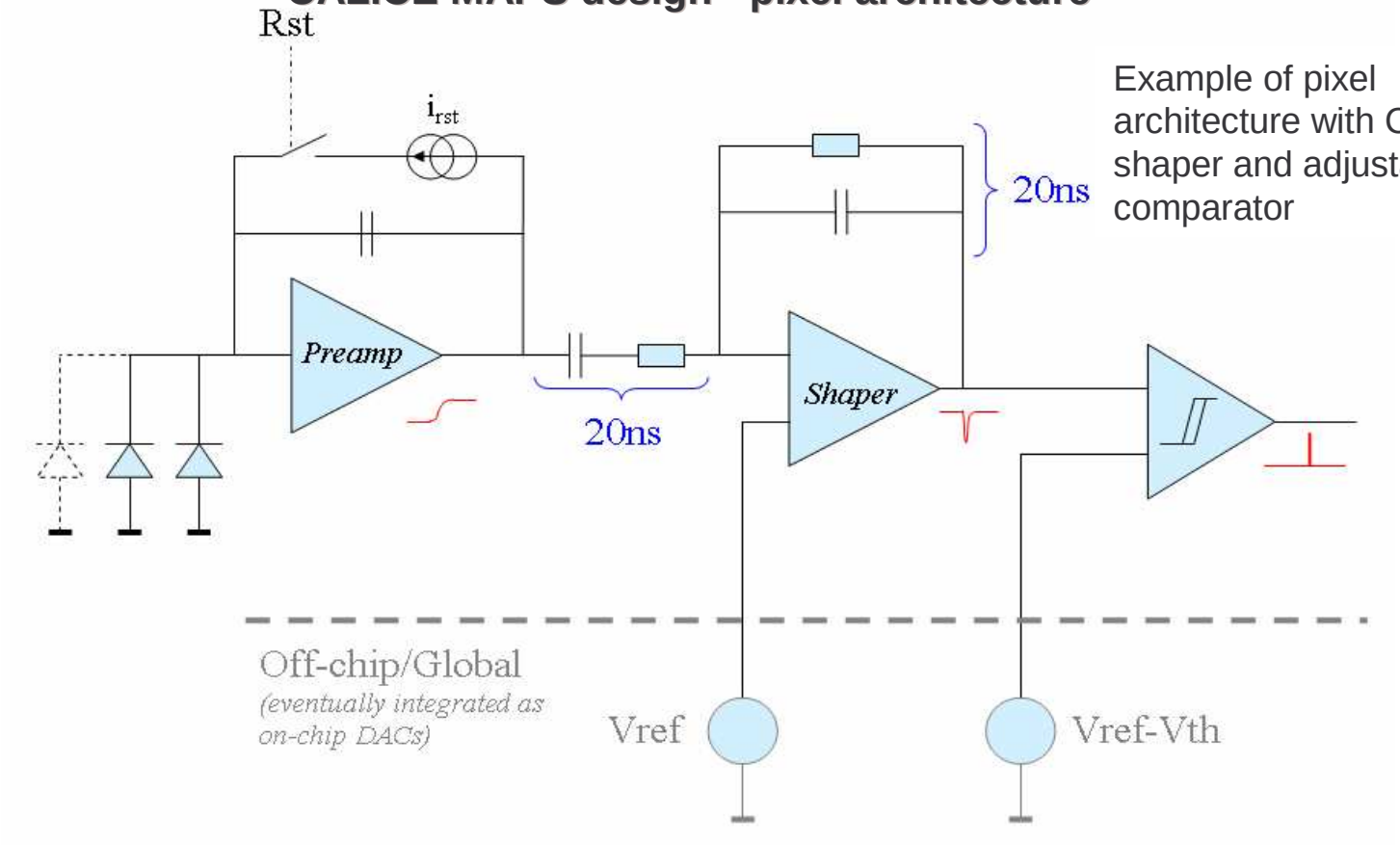
CALICE MAPS design - pixel architecture -

Example of architecture of pixel with CDS



CALICE MAPS design - pixel architecture -



Example of pixel architecture with CA, shaper and adjustable comparator

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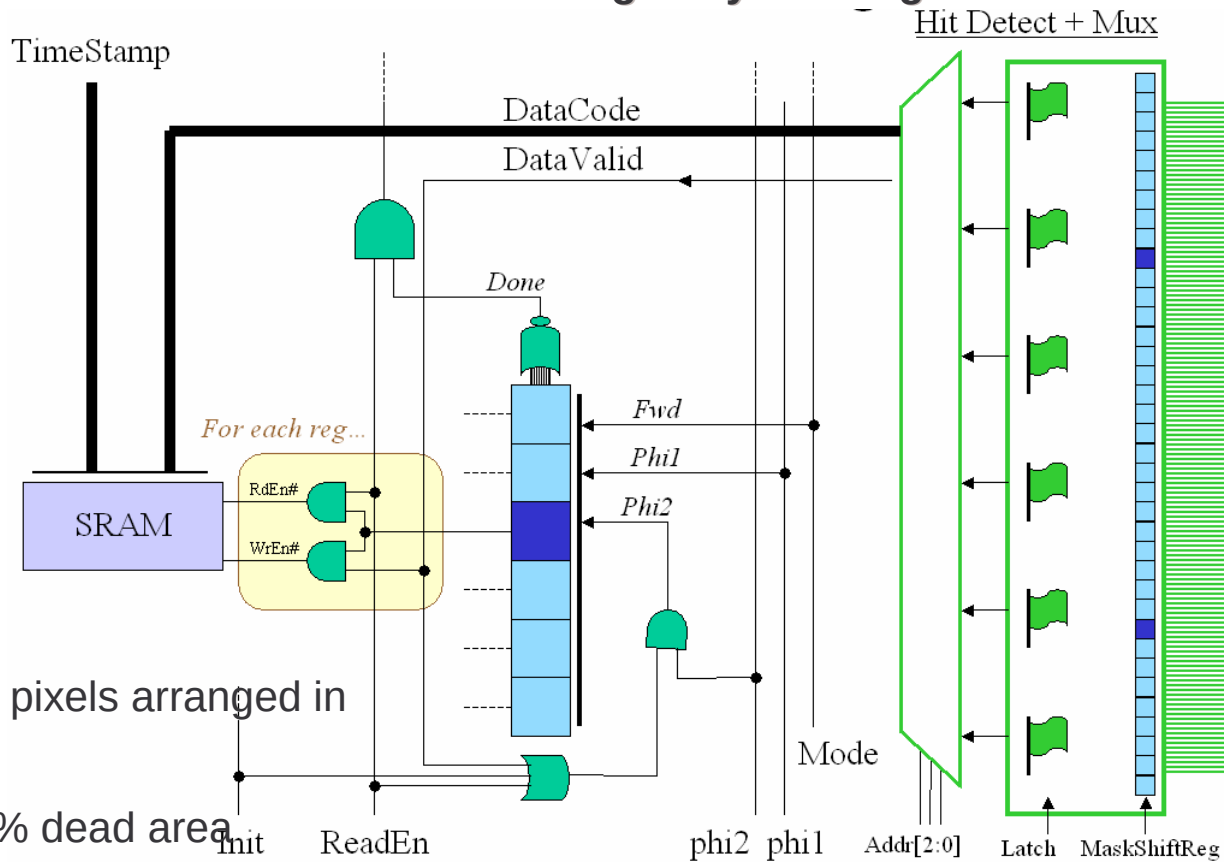
CALICE MAPS design - system logic -



Hit logic

- Serves 42 pixels arranged in row
- Around 8 % dead area

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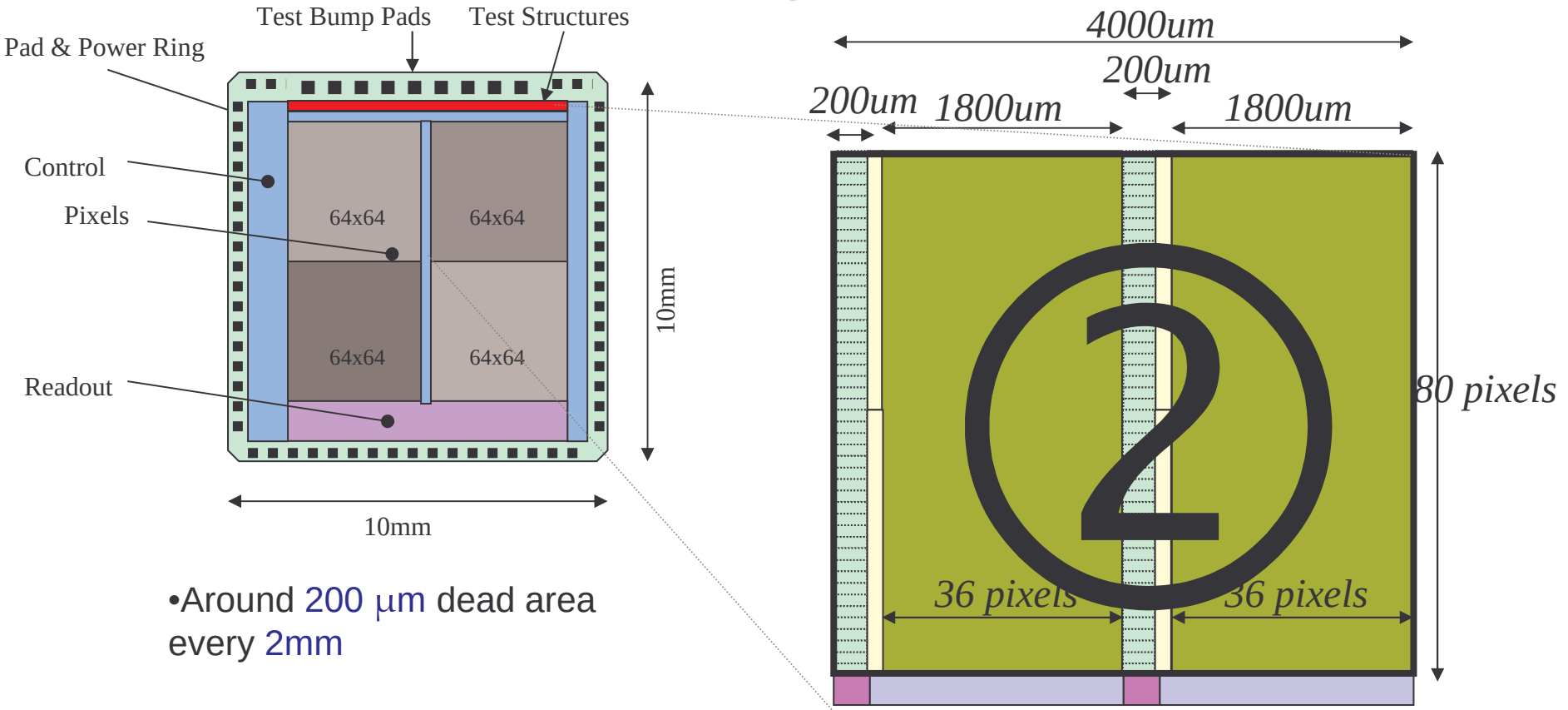
CALICE MAPS design - area estimate -



- Around 200 μm dead area every 2mm

Conclusions

- Minimum Σ charge signal for full pixel coverage ~ 200 e^-
- S/N ~ 10 achievable
- Collection time ~ 250 ns for pixel coverage: optimisation needed
- Likelihood of double hits following collection time reduction in progress
- Improved diodes layout and pixel architecture study in progress
- Power issues require further analysis