CALICE Next Generation DAQ

David Bailey
University of Manchester

Overview

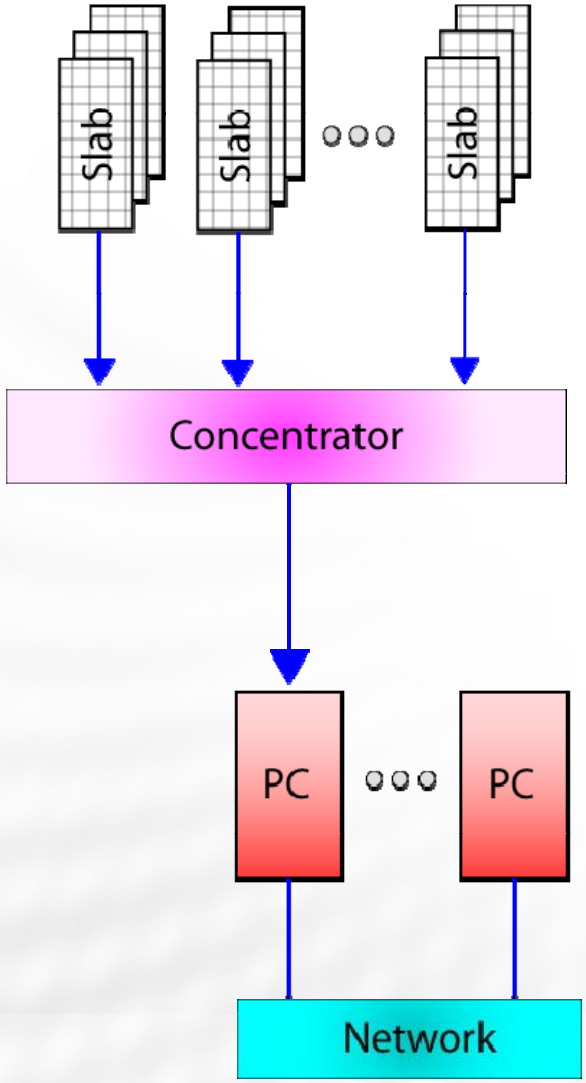
- Aim to develop a generic system
  - Maximise use of off-the-shelf commercial components
    - Reduce as far as possible the need for bespoke solutions
      - Clearly some custom electronics will be needed at the very front end to control and read-out of sub-detectors
  - Provide well defined interfaces between DAQ components to allow for simple upgrading or replacement in future without major re-design or cost

Requirements

- What do we need to provide?
  - Triggerless operation
  - Delivery of clock and control to front end
  - Enough bandwidth to read out (potentially) the whole detector without hitting performance bottlenecks
  - Redundancy in case of DAQ system component failures

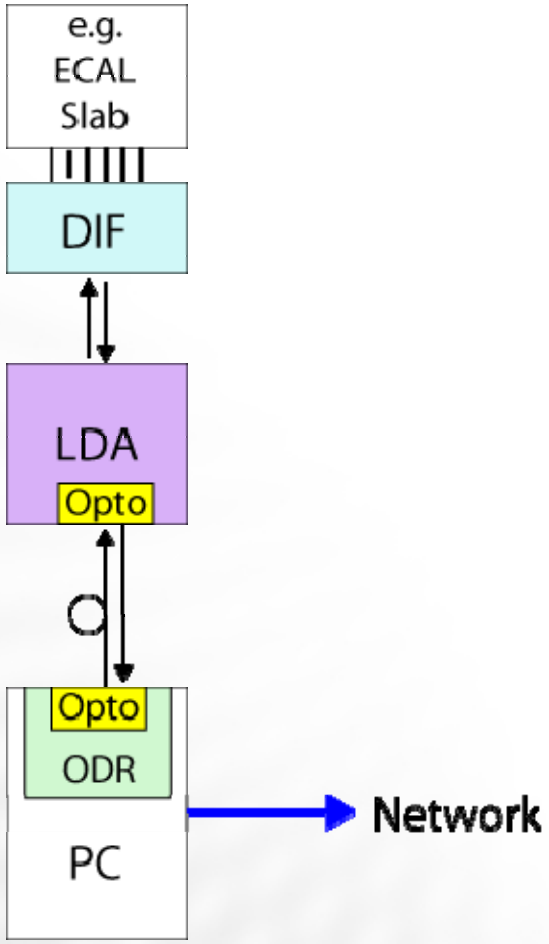
Possible Architecture

- Classic funnel
  - Front end read out into on (or very near) detector data concentrator
  - Concentrator buffers, frames and transmits data over high-bandwidth links to off detector receivers
  - Off detector data unpacking, filtering and storage



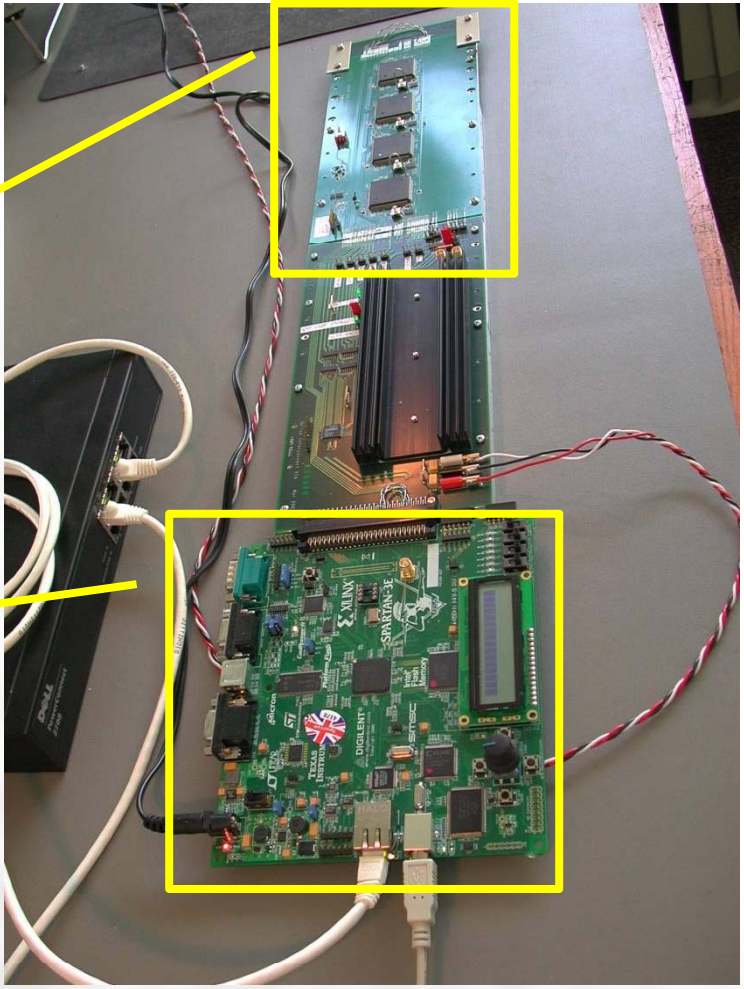
Prototype

- EUDET DAQ
  - Control interface to front-end electronics on component specific Detector InterFace (DIF) board
  - On/Near detector concentrator (LDA)
    - Clock and control master for DIF
    - Direct input from machine clock or provided from ODR
      - Link/cost implications
  - Off Detector Receiver currently implemented as PCI express card in a PC
    - Consider other technologies such as ATCA as they mature
    - Also may be able to convert directly to network protocols on ODR and assemble complete events in a virtual, network based event builder



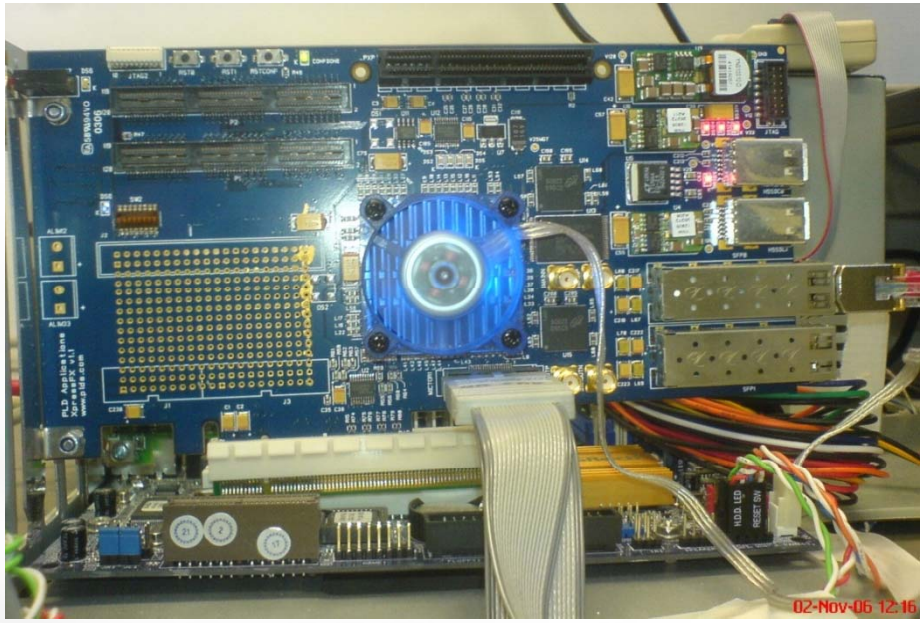
Very Front and Front End System

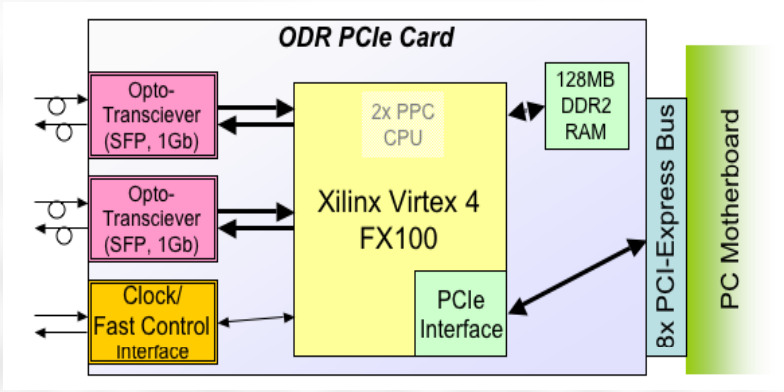
- On-detector test system
  - Investigate data integrity over long PCBs
    - Eventually 7 modules will be stitched together
    - FPGAs used to simulate ASICs
    - Allows testing of layout, data rates, protocols and signalling schemes
  - Commercial Xilinx development board used to prototype DIF
    - Onboard USB and 10/100 Ethernet for control and data link testing



Off Detector Systems

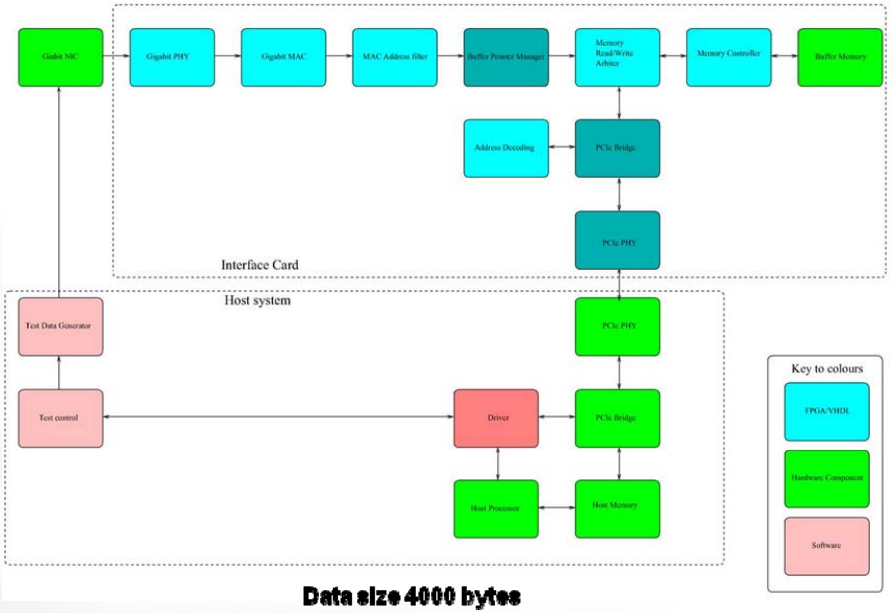
- Prototype ODR
  - Implemented on Virtex 4 development boards supplied by PLDApplications
    - Onboard PCI-express interface
    - Large Virtex 4 FPGA
    - DDR2 memory
    - 2 SFP opto/copper link interfaces
  - 1 Gbit/s Ethernet integrated as part of design to simplify initial testing
    - Also allows card to be used as network packet generator

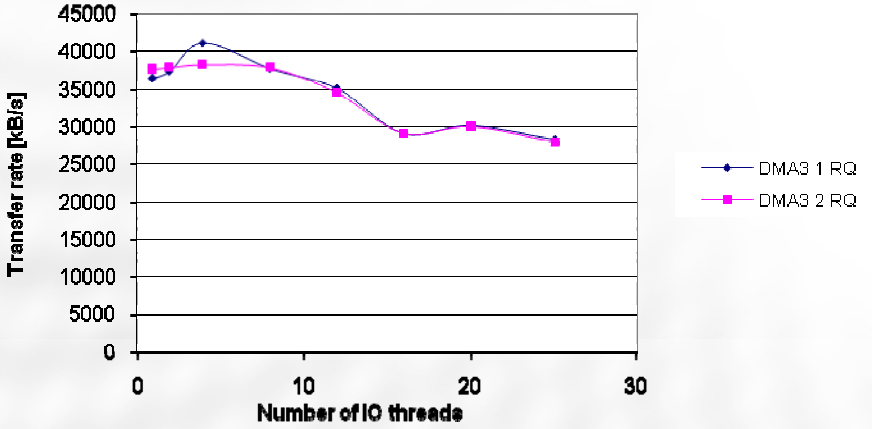




ODR Prototype

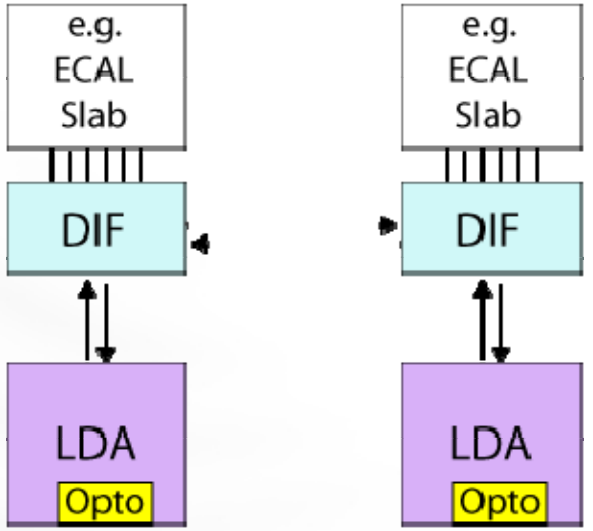
- Status
  - Initial firmware complete
  - Host PC driver working
  - Investigating data rate throughput to local disks
    - Reasonable rates already achieved with first iteration
- Bottom line
  - We have a working ODR prototype

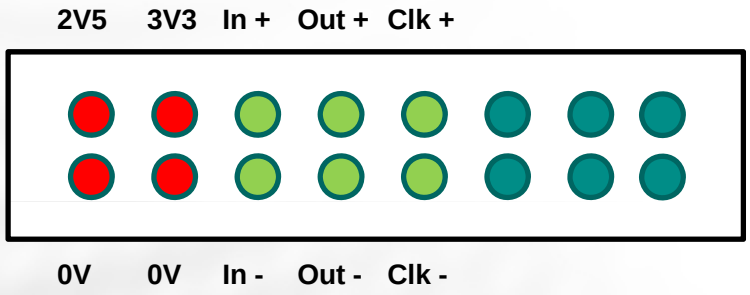




LDA, DIF and Redundancy

- Highly desirable to have option for DIFs connected to separate LDAs to have redundant data and clock path
  - Failover in case of link failure
  - Vital as master clock to front end is provided by/derived from LDA
  - Current ideas use pairs of DIFs, but could easily extend to a token ring system if needed
  - Envisage a rather simple system for test beams
- LDA-DIF physical link technology under discussion
  - Needs to be synchronous with machine clock and of fixed latency
    - Beam on/off signals for power pulsed modes of operation
    - External triggering
- Have an initial specification for the physical interface to the DIF which is completely independent of link/clock technology

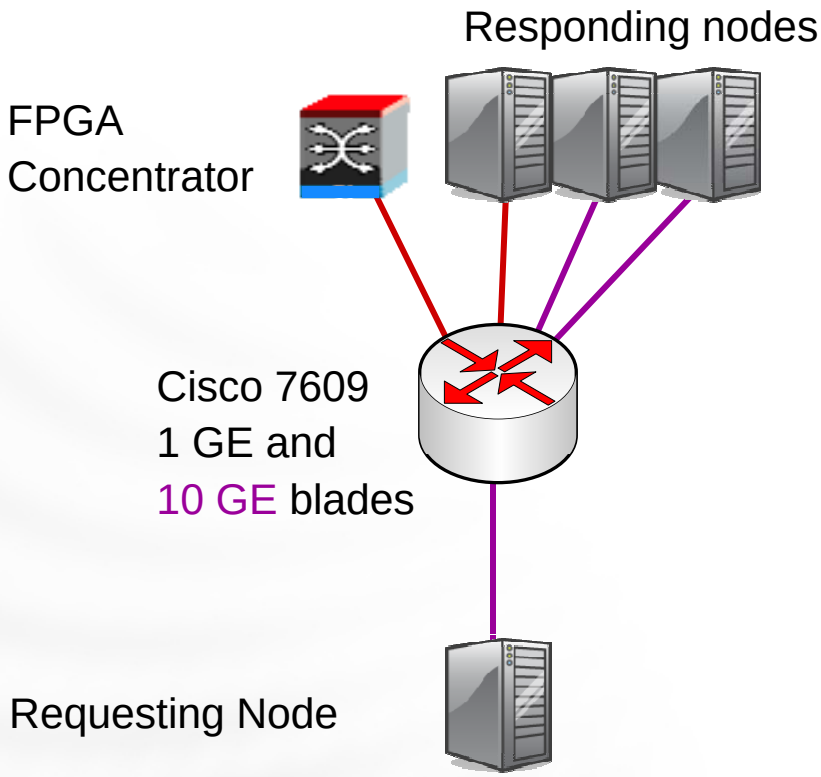




Simple IDC connector with LVDS signals and power

Networking

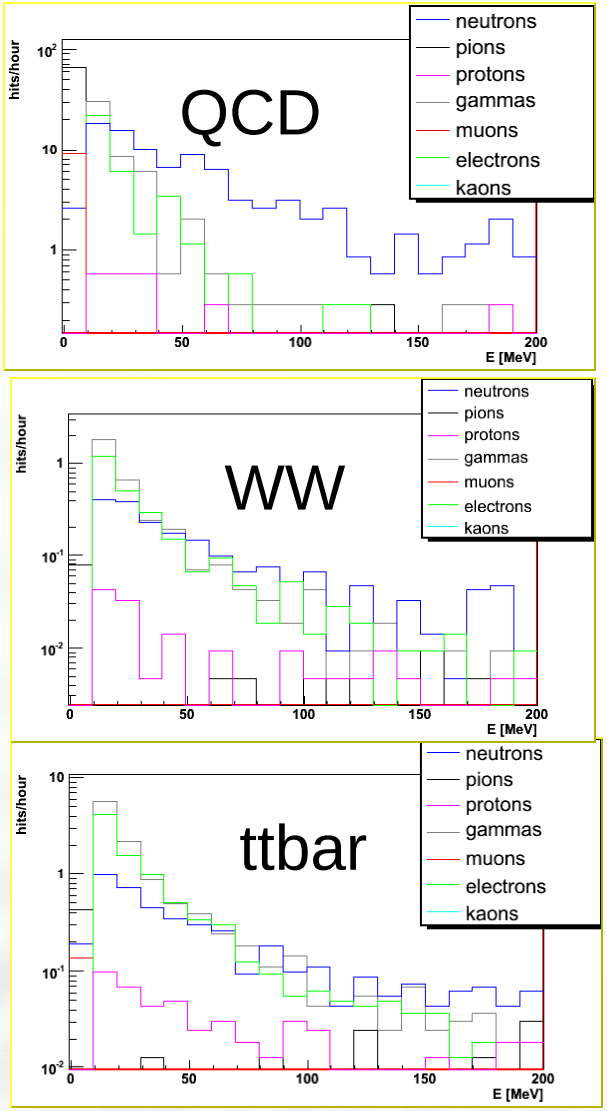
- Using FPGA for network protocol and topology tests
  - ODR board used as data source and sink directly on network
  - Use for testing Raw Ethernet Frame generation by the FPGA
  - Test Data collection with Request-Response protocols
- FPGA easily drives 1Gigabit Ethernet at line rate
  - Packet dynamics on the wire as expected
  - Loss of Raw Ethernet frames in end host being investigated
- Request-Response style data collection promising
  - Developing a simple Network test system
- Planned upgrade to operate at 10Gbit/s



Details in proceedings of IEEE Realtime 2007 Wokshop at Fermilab, May 2007

FPGA Robustness

- ASICs and FPGAs embedded in detector
  - Need to assess robustness against single event upsets induced by showers
  - Simulate various processes and estimate upset rate
    - See V. Bartsch's talk in the DAQ parallel for details



FPGA Robustness

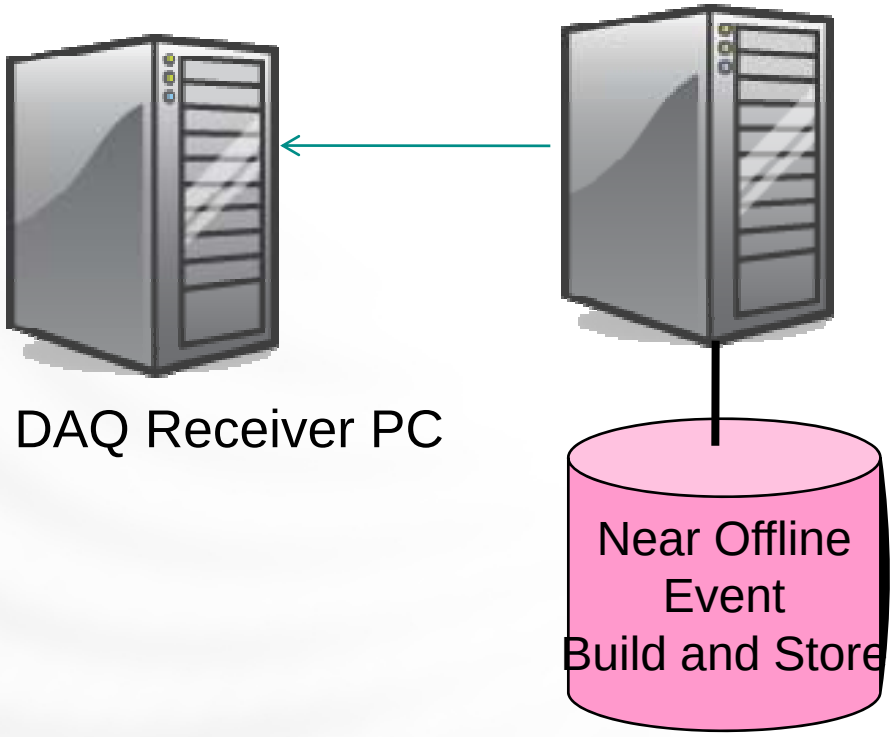
FPGA	threshold [MeV]	SEU σ [cm^2/device]	SEUs/day
Virtex II X-2V100 & Virtex II X-2V6000	5MeV	$8*10^{-9}$	0.17
Altera Stratix	10MeV	10^{-7}	1.99
Xilinx XC4036XLA	20MeV	$3*10^{-9}$	0.02
Virtex XQVR300	10MeV	$2*10^{-8}$	0.38
9804RP	20MeV	10^{-8}	0.17

all data from literature, references not given in talk

- Looks like FPGAs need to be reconfigured once a day
- Before operation, radiation tests need to be done with FPGAs chosen for experiment

DAQ Software

- Hardware is not the only story
  - Need control software to integrate with the rest of the testbeam/experiment
  - Need event builder software to merge bunch train data from disparate sources into complete single event data
    - See R. Poeschl's talk in the DAQ parallel for details



Bunch train data processing relies on meta-data embedded in the data stream

Conclusions

- DAQ Development very active
  - Clearly this is not the final ILC system!
    - At least 5 years away...
    - Aiming to test and evaluate commercial systems as much as possible
  - Deliver a common prototype system as part of EUDET
    - Serious tests of off-the-shelf components and technology
    - First prototypes of some systems are already working
  - Need to plan for test of single event upsets in FPGAs in realistic conditions
  - DAQ control software development beginning
- Would love to engage with people beyond the calorimetry community to exploit synergies and understand other's requirements