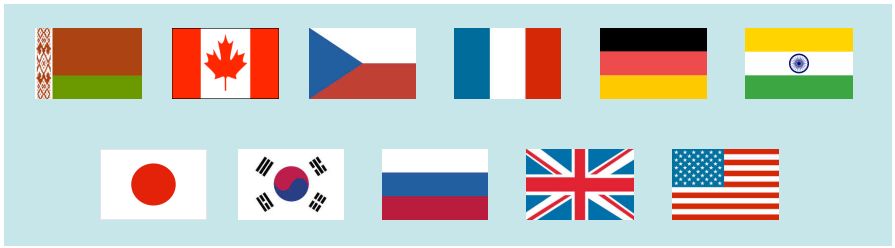


CALICE - DAQ communication & DAQ software

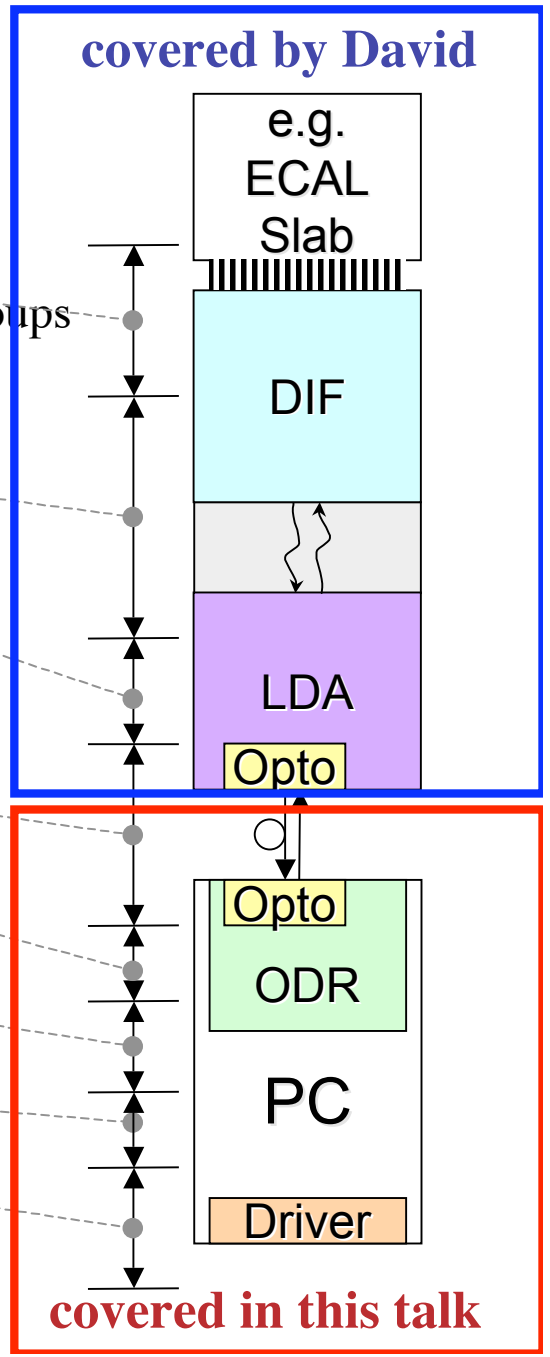
V. Bartsch (UCL) for the CALICE DAQ UK group

outline:

- options for network / switching
- clock
- control: SEUs
- DAQ software for EUDET

DAQ Overview

- **Detector Interface (DIF)**
  - Sub-detector specific, in conjunction with detector groups
- **DIF to LDA**
  - Generic, Copper links (25Mbit)
- **Link/Data Aggregator (LDA)**
  - Data format
  - Clock/Commands fan-out
- **LDA to ODR opto-links**
- **Off-Detector Receiver (ODR)**
- **ODR to disk**
  - PCI-Express driver software
- **Local Software DAQ**
- **Full blown Software DAQ**

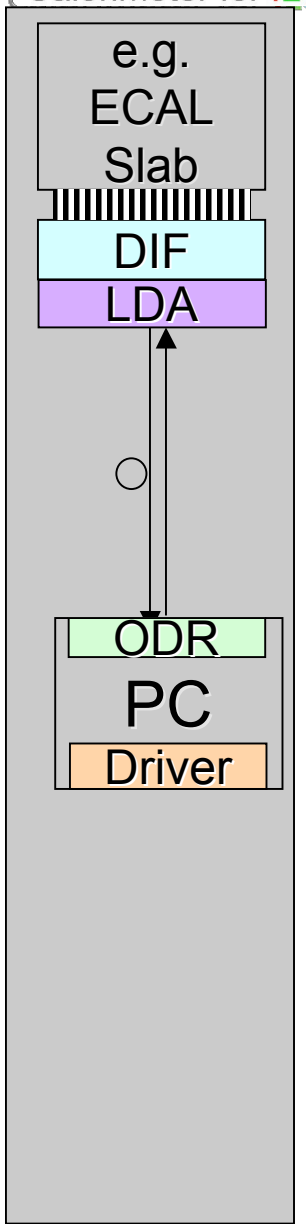


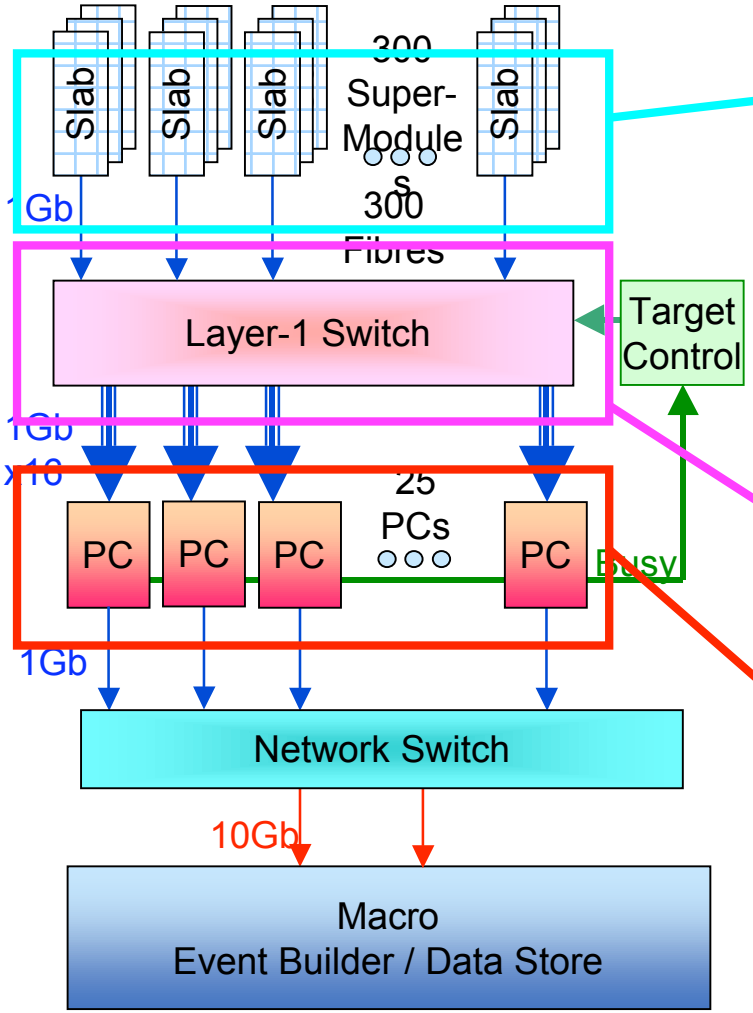
network / switching

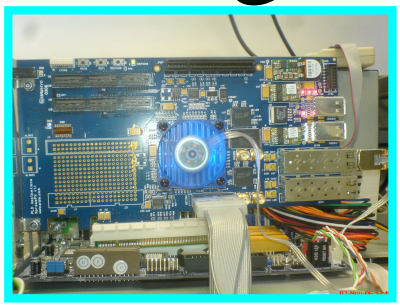
Motivation:

- **useful R&D for detectors that need it**
- **useful for aggregating data together and thereby needing less hardware**

options for network / switching





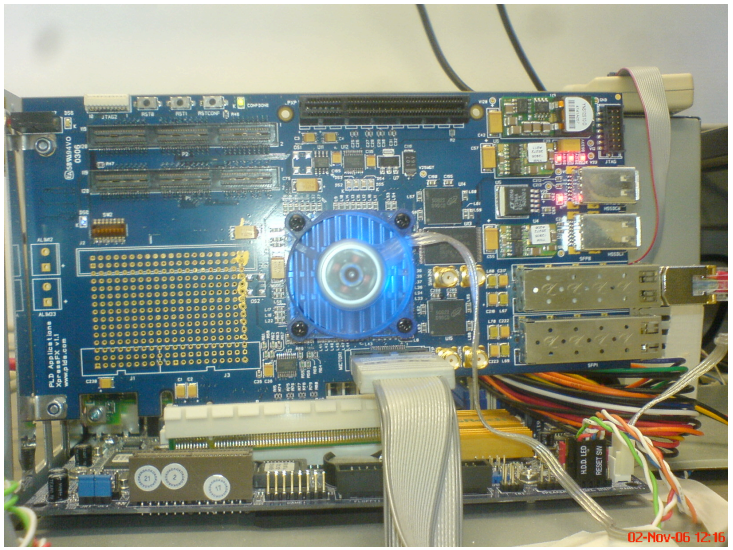


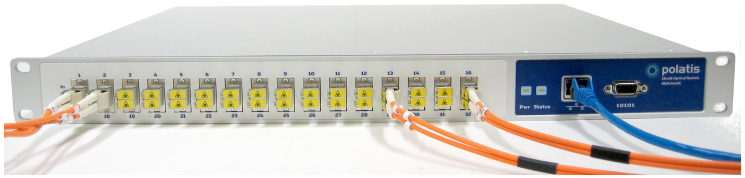
working FPGA based Ethernet system, using RAW frames

optical switch delivered

high (>9GBits) bandwidth usage using PCIe 10Gig cards (from Myricom)

networking





Off detector receiver

- working FPGA based Ethernet system, using RAW frames
- successfully doing bi-directional communications in a request-response mechanism to simulate data transfer from a detector readout to off detector receivers
- Larger scale test and 10Gigbit upgrade options currently under evaluation

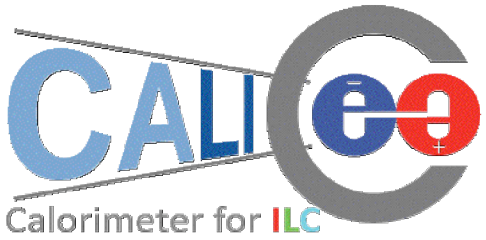
All optical switch

- 16x16 multi mode switch Polatis, 20ms switching time, piezzoel. MEMS, LC Connectors, about 20k brit. Pounds

=> dispatching and routing task

PCI boards

- successfully shown high (>9GBits) bandwidth usage using PCIe 10Gig cards (from Myricom)
- reasonable CPU usage



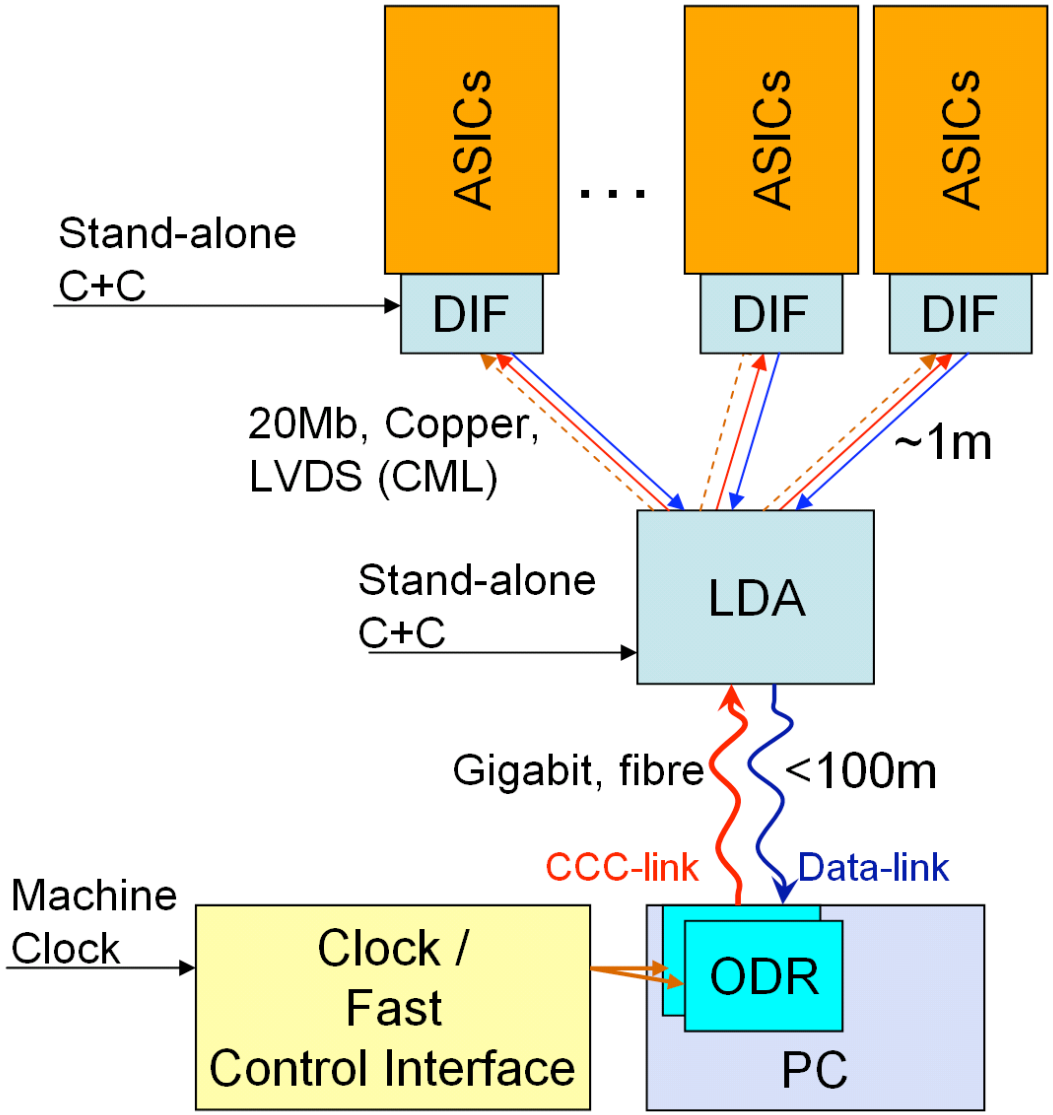
clock

Requirements need to settled for design

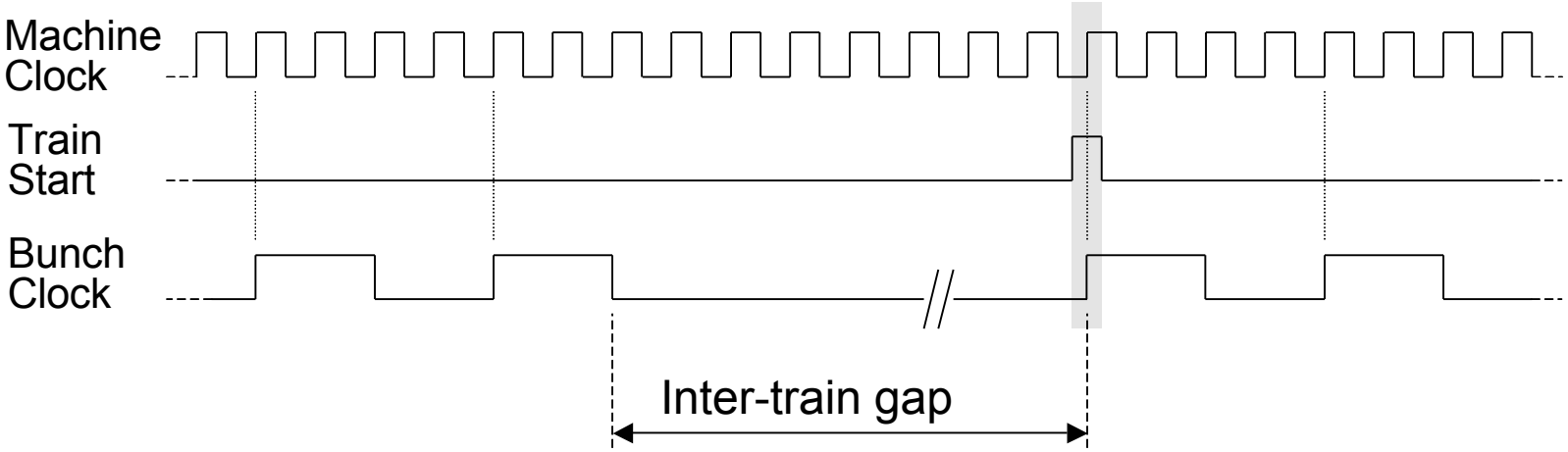
clock

Requirements:

- 'Machine' Clock (*MCLK*): <= 50MHz, low jitter
- Fast commands: Accurate to an MCLK period
  - i.e. Links require fixed latency command channel
- ODR: 125MHz clock because of 1Gb link specifications (very low jitter), multiple of machine clock
- LDA: Derive *MCLK* with low jitter (for other? detectors): <1ns
- DIF: MCLK from link used as ASIC digital clock (low jitter)
  - Bunch Clock = MCLK/16 because of bunch spacing (appr. 320ns)
  - Fast commands to determine bunch clock phase with respect to MCLK.



BC clock synchronisation



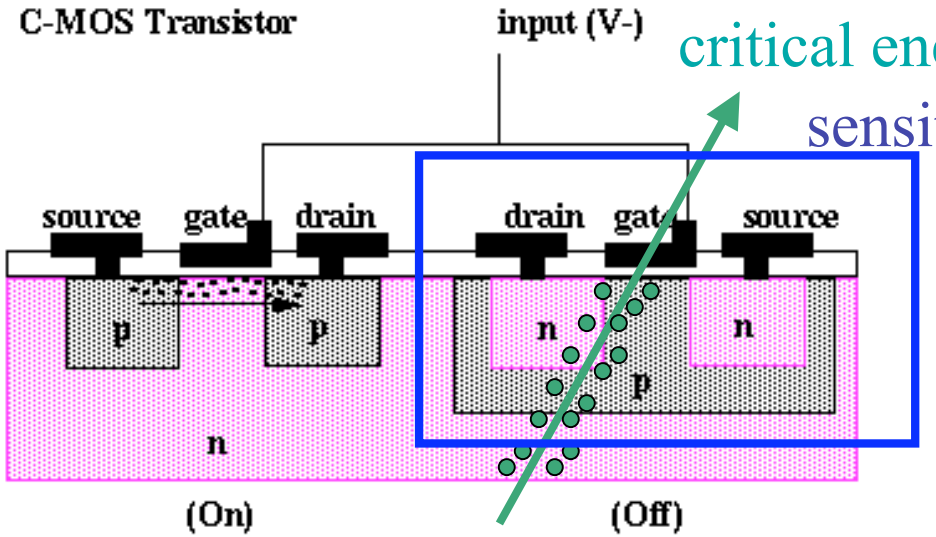
Machine-clock is 4x bunch-clock in this example

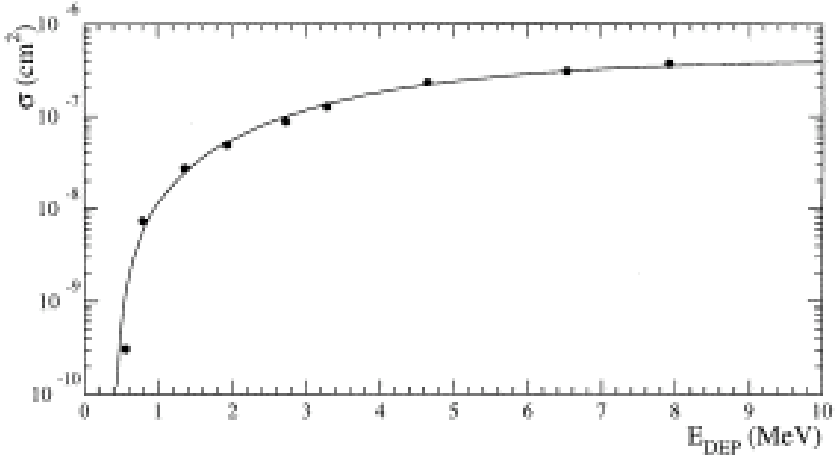
control: SEU

Motivation:

• bottle necks in the design need to be found and studies be done

SEU principle

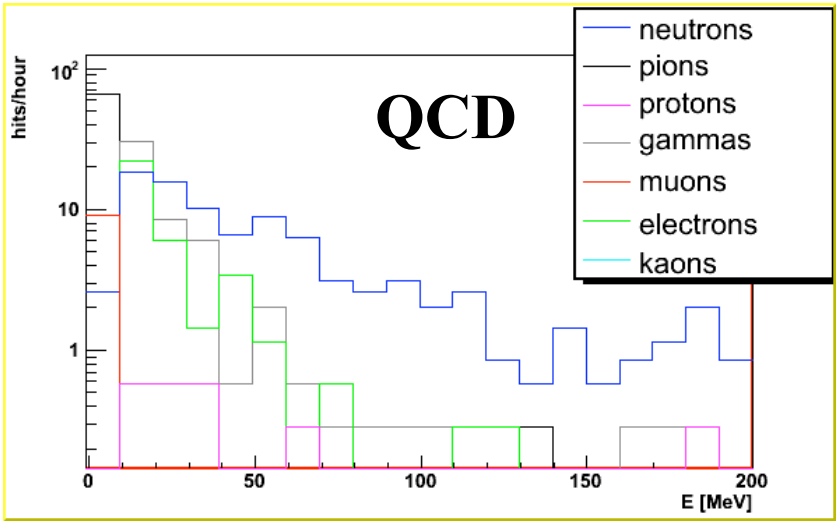




from E. Normand, Extensions of the Burst Generation Rate Method for Wider Application to p/n induced SEEs

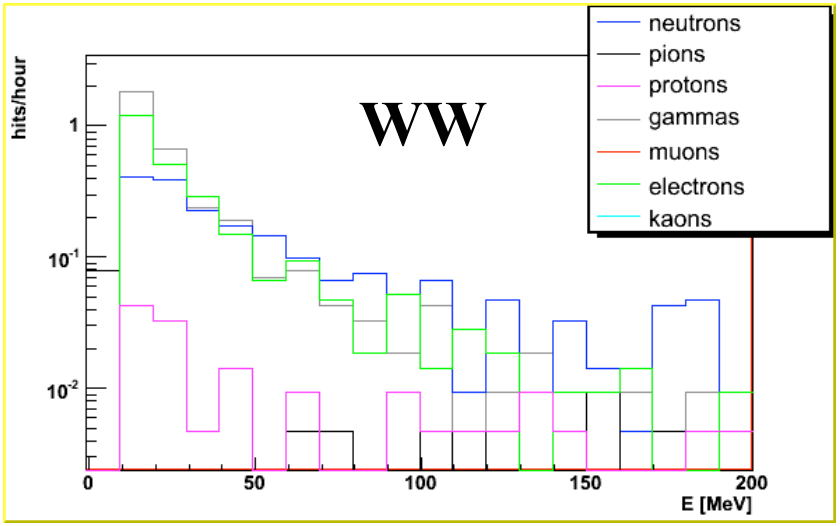
=> look for neutrons, protons and pions depositing energy in the FPGAs

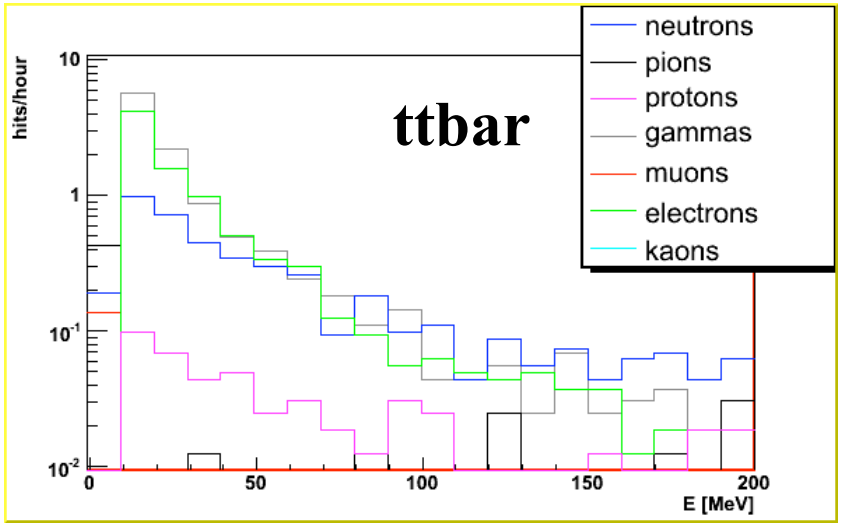
SEU: energy spectrum of particles in the FPGAs



- ttbar: 50-70 events/hour
- WW: 800-900 events/hour
- QCD: 7-9Mio events/hour

from TESLA TDR





SEU: other FPGAs

FPGA	threshold [MeV]	SEU σ [cm^2/device]	SEUs/day
Virtex II X-2V100 & Virtex II X-2V6000	5MeV	$8*10^{-9}$	0.17
Altera Stratix	10MeV	10^{-7}	1.99
Xilinx XC4036XLA	20MeV	$3*10^{-9}$	0.02
Virtex XQVR300	10MeV	$2*10^{-8}$	0.38
9804RP	20MeV	10^{-8}	0.17

all data from literature, references not given in talk

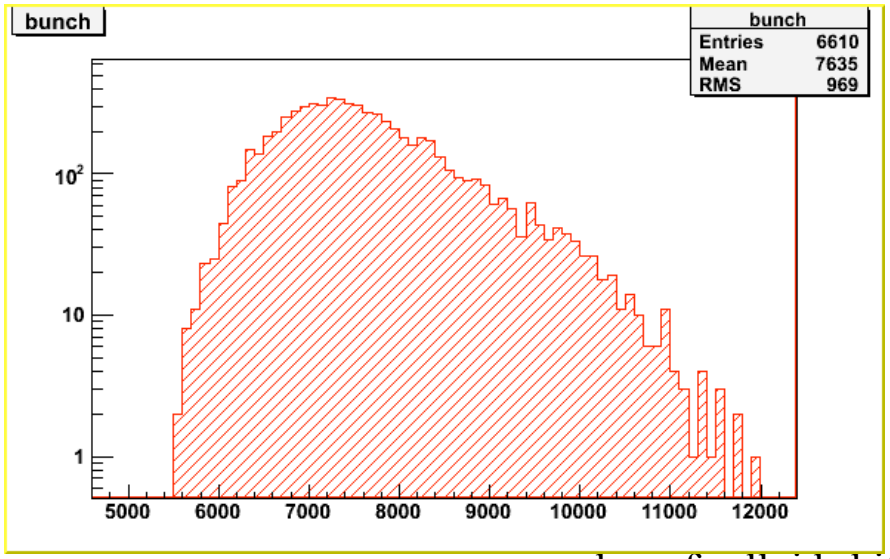
⇒ looks like FPGAs need to be reconfigured once a day

⇒ before operation radiation tests need to be done with FPGAs chosen for experiment

occupancy - for the barrel

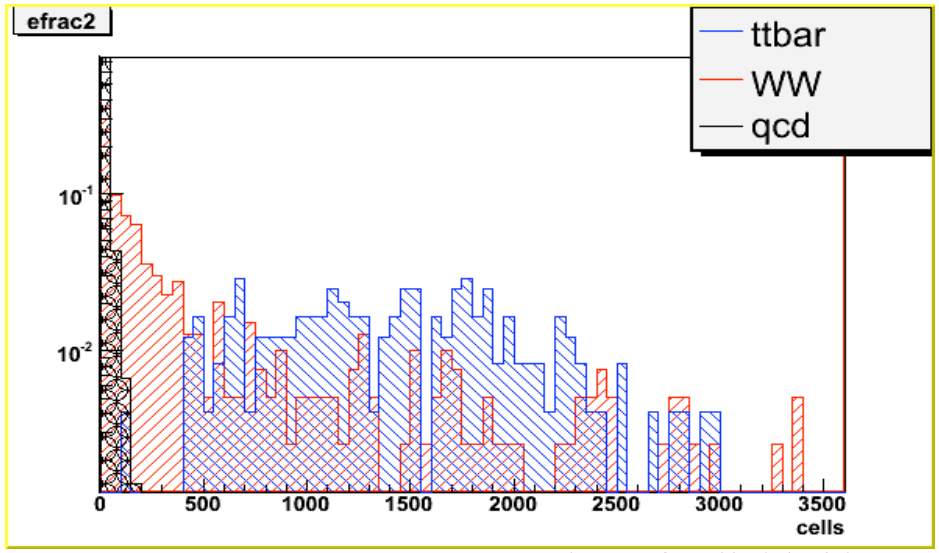
Hits per bunch train

(assuming Gauss distribution of events)



number of cell_ids hit

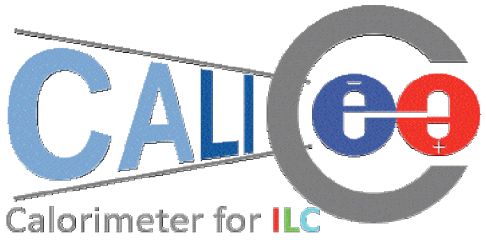
hits per bx



number of cell_ids hit

$\Rightarrow$ Occupancy derived from physics events per bunch train:

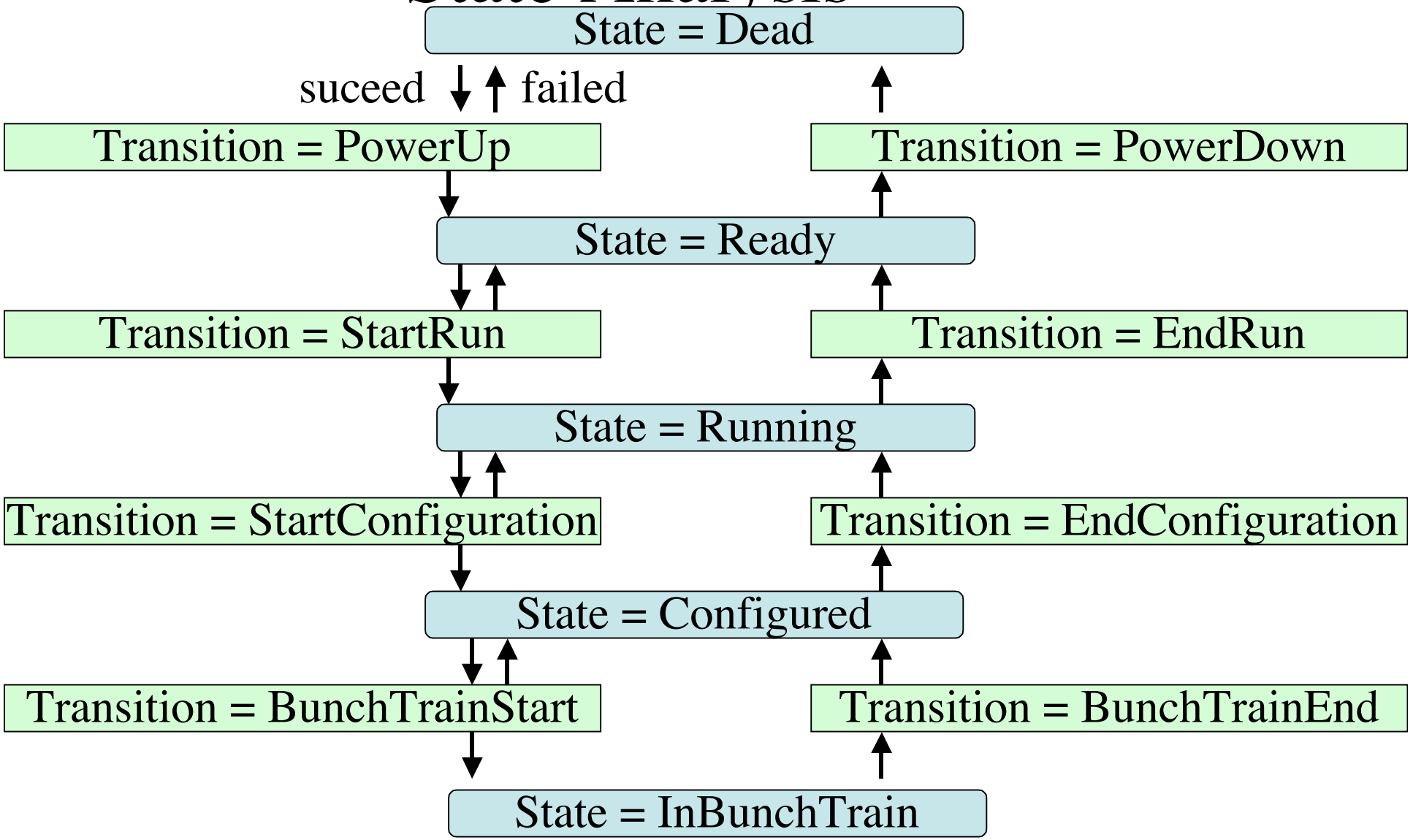
12000 hits/24Mio cells = $5*10^{-4}$



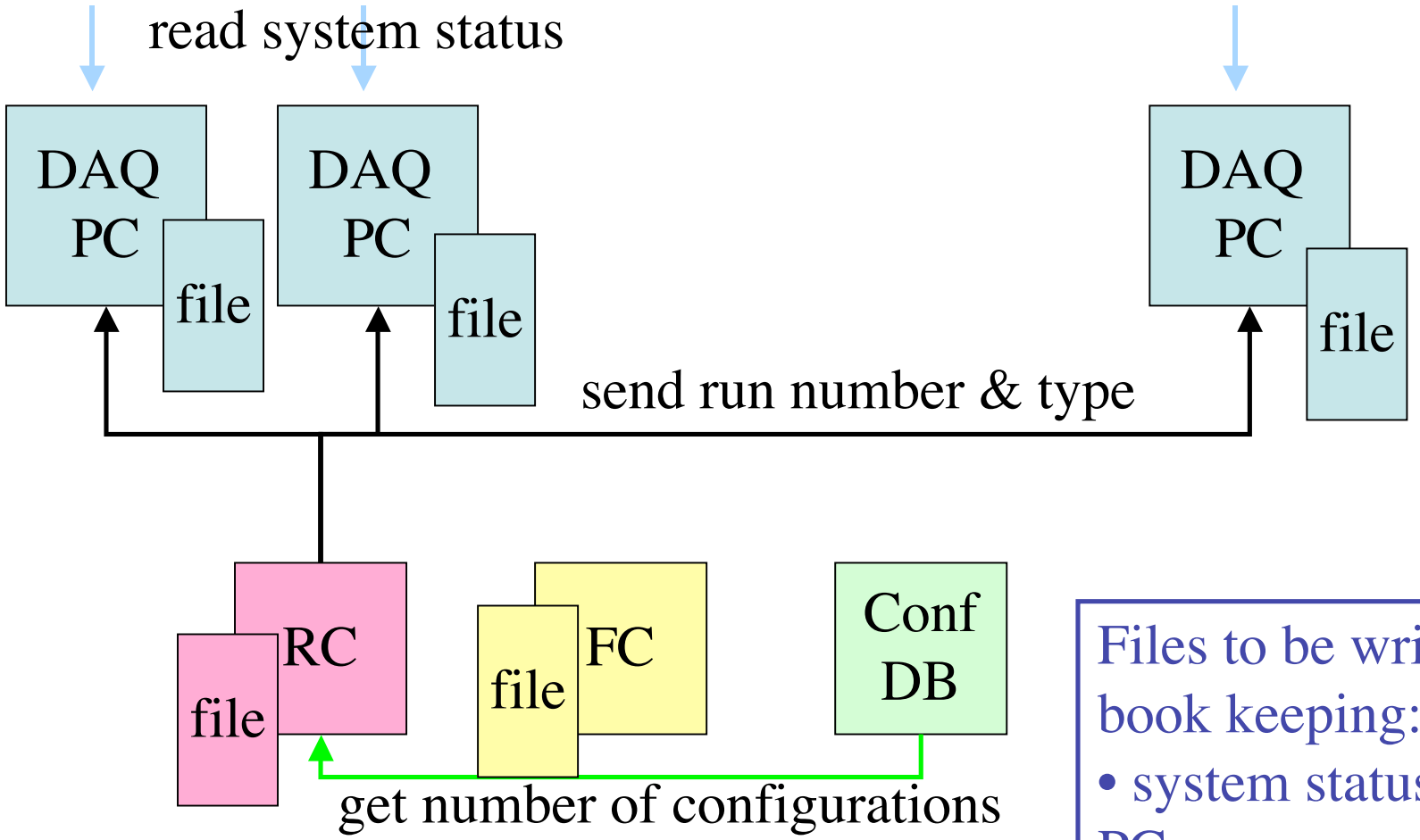
DAQ software for EUDET

Requirements need to be settled
It is important in contrast to software for Testbeams to think about data being delivered in bunch trains not in events

DAQ software for Eudet: State Analysis



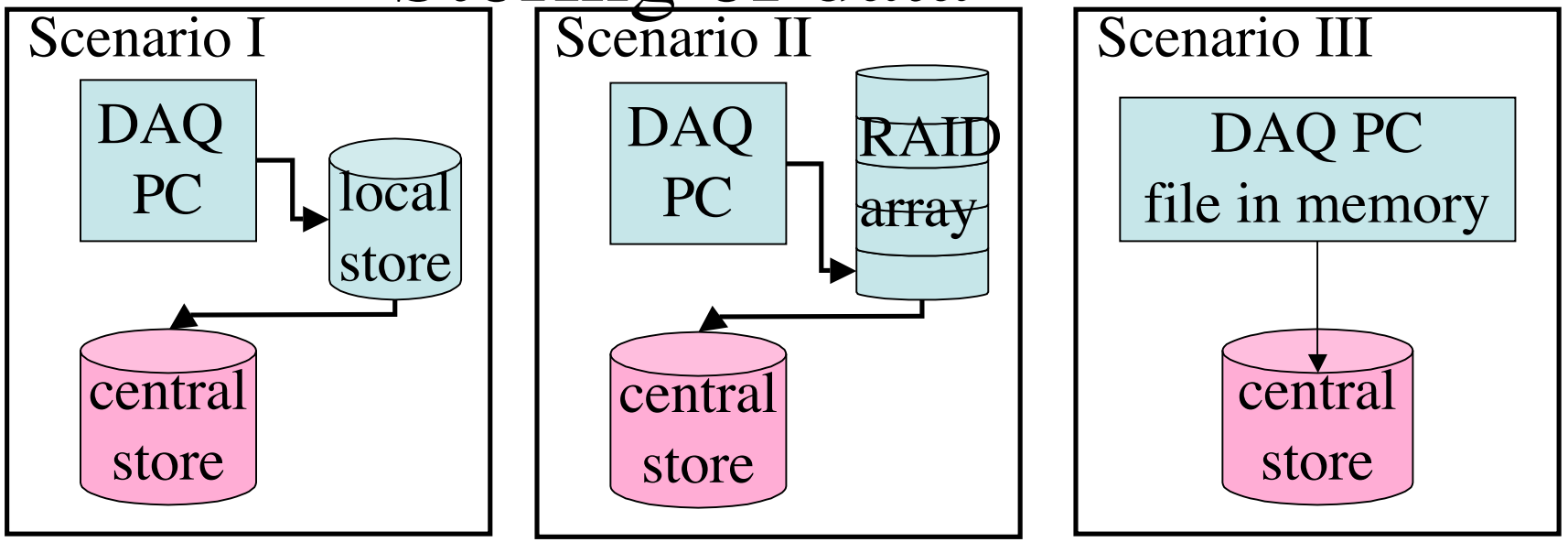
DAQ software for EUDET: Transition: StartRun



Files to be written for book keeping:

- system status by DAQ PC
- run info by RC PC
- system status by FC

DAQ software for EUDET: Storing of data



- which scenario to choose depending on the bandwidth with which the data gets produced: (I) up to 200Mbit/sec, (II) up to ~1600Mbit/sec, (III) from there on
- desirable to have files because transfer is easier and in case of timing problems error handling is easier, but keep system flexible for now
- worst case estimate (very rough):

30layers*100cm*100cm*2kB memory @ each ASIC/72 no of channel @ ASICS = 10MB/bunch train = 400Mbit/sec

summary

- requirements of clock/control data need to be discussed
- network switching activity started
- estimate on radiation effects on FE electronics done and as expected small effects
- use cases for software DAQ for EUDET sorted and design decisions can still be discussed

acknowledgement

- Matt Warren, Matthew Wing, UCL
- Richard Hugh-Jones, Marc Kelly, David Bailey, Manchester
- Owen Miller, Birmingham
- Paul Dauncey, Imperial
- Tao, RHUL

DAQ system - general R&D work

- Make assumptions as to what can be done in the VFE, in the FE => need to be flexible. Assume reading out higher volume and can definitely do anything lower.
- Using commercial, off-the-shelf products, which should be cheap, scalable and maintainable.
- Identify bottlenecks in this concept, effects on the calorimeter system.
- Should be applicable to the HCAL - other non-calorimeter components?
- Test-bench work and demonstration of workability of concept.
- Also: should be able to provide DAQ for prototype calorimeters being developed.

clock

Structure:

- Clock source/interface feeds ODRs with ‘machine’ clock
- ODR synchronises CCC-link to LDA with this clock
  - –Clock transferred to ODR via optic-fibre
- LDA derives FE link clock
  - –Clock distributed multiple DIFs via LVDS up-links
- FE extracts clock in hardware

Addition standalone/debug structure:

- Standalone clocks on LDA and DIF
- Clock LDA directly
- Clock DIF directly
  - –Allows clock to be received separately from control.