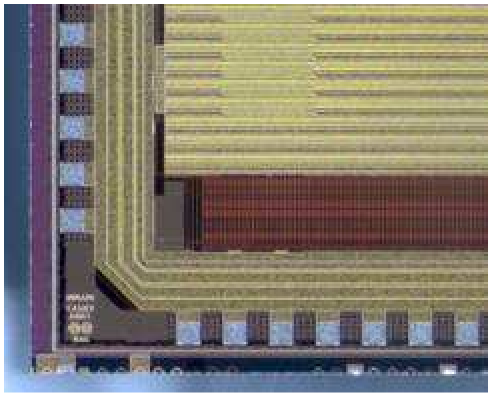
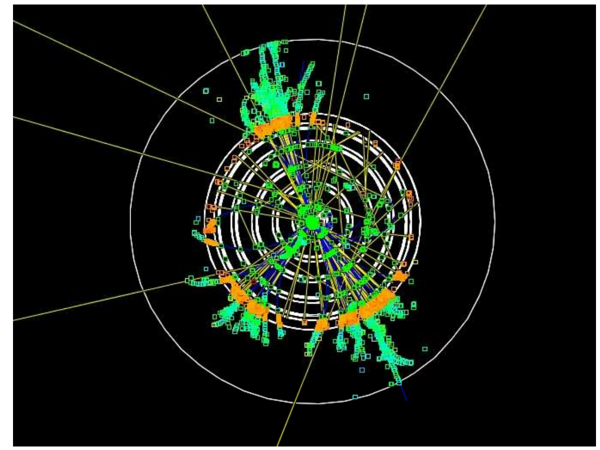
MAPS ECAL

SiD Workshop
RAL 14-16 Apr 2008

Nigel Watson
Birmingham University

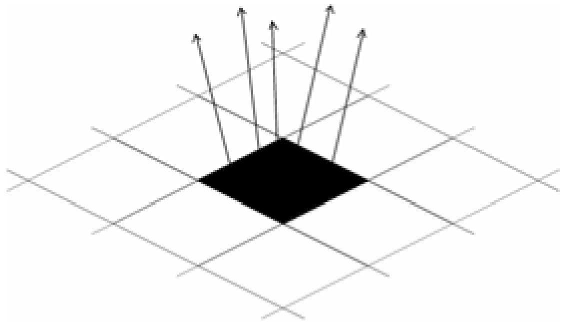


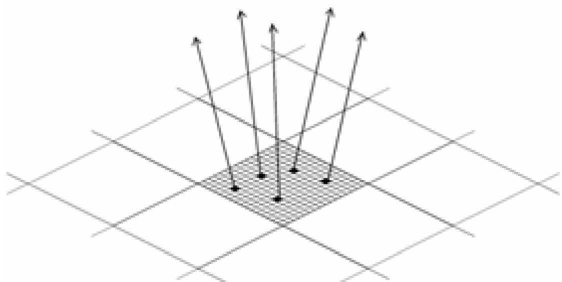


- Overview
- Testing
- Summary

For the CALICE MAPS group
J.P.Crooks, M.M.Stanitzki, K.D.Stefanov, R.Turchetta, M.Tyndel, E.G.Villani (STFC-RAL)
J.A.Ballin, P.D.Dauncey, A.-M.Magnan, M.Noy (Imperial)
Y.Mikami, **T.Martin**, O.D.Miller, V.Rajovic, NKW, J.A.Wilson (Birmingham)

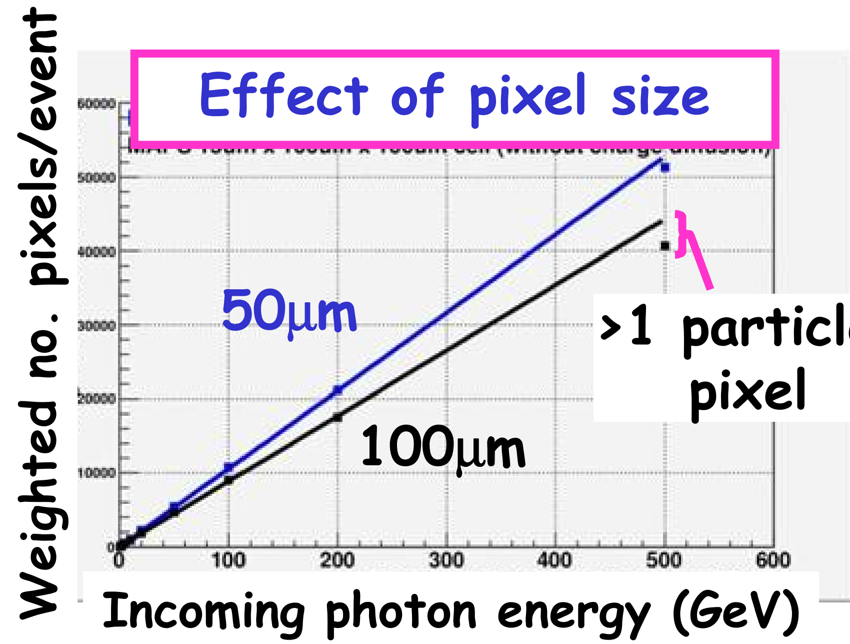
MAPS ECAL: basic concept





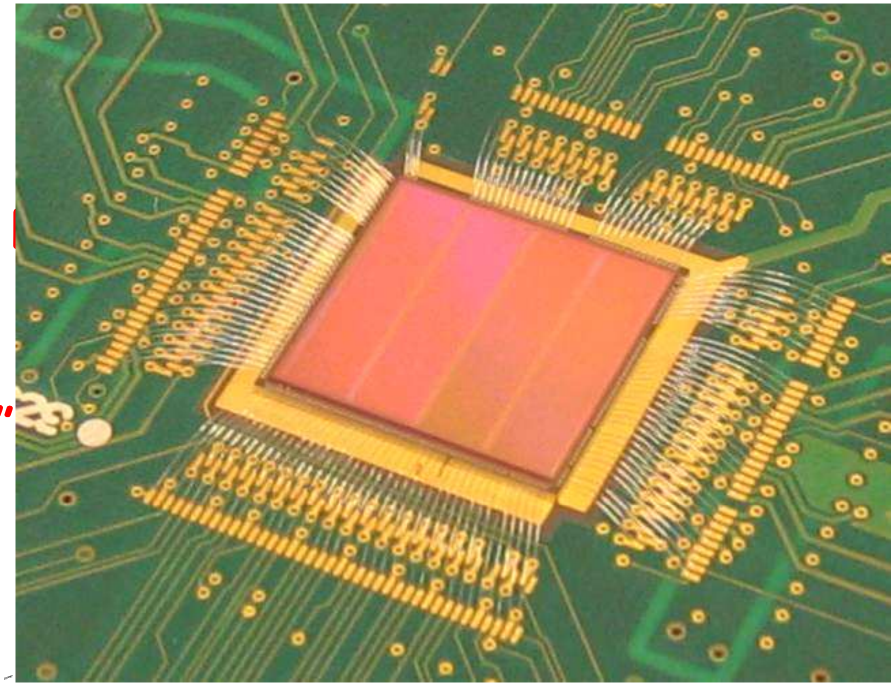
- Swap ~0.5x0.5 cm^2 Si pads with small pixels
  - "Small" := at most one particle/pixel
  - 1-bit ADC/pixel, i.e. **Digital ECAL**

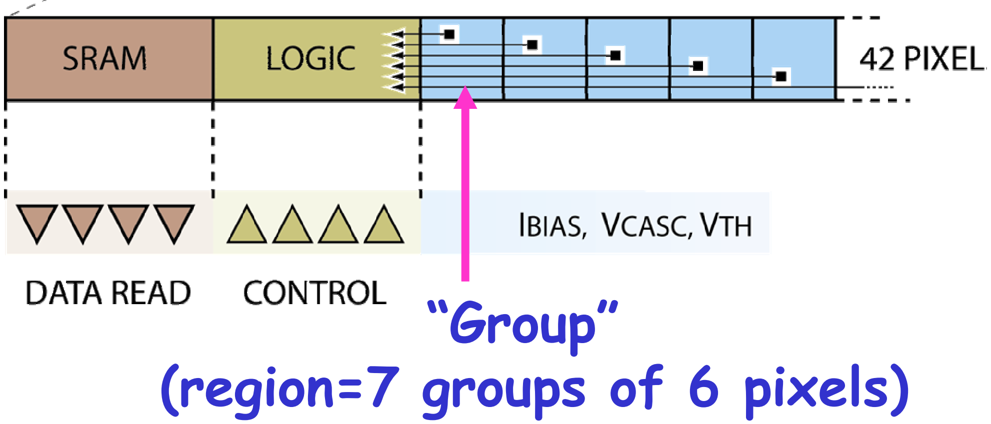
- How small?
  - EM shower core density at 500GeV is ~100/mm^2
  - Pixels must be<$100\times100\mu m^2$
  - Our baseline is $50\times50\mu m^2$
  - Gives ~10^{12} pixels for ECAL – "Tera-pixel APS"



TPAC1 overview

- 8.2 million transistors
- 28224 pixels; 50 μm; 4 variants
- Sensitive area 79.4mm^2
- Four **columns of logic+SRAM**
  - Logic columns serve **42 pixel "region"**
  - Hit locations & (13 bit) timestamps
  - **Local SRAM**
  - **11% deadspace for readout/logic**
- Data readout
  - Slow (<5 MHz) – train buffer
  - Current sense amplifiers
  - Column multiplex
  - 30 bit parallel data output





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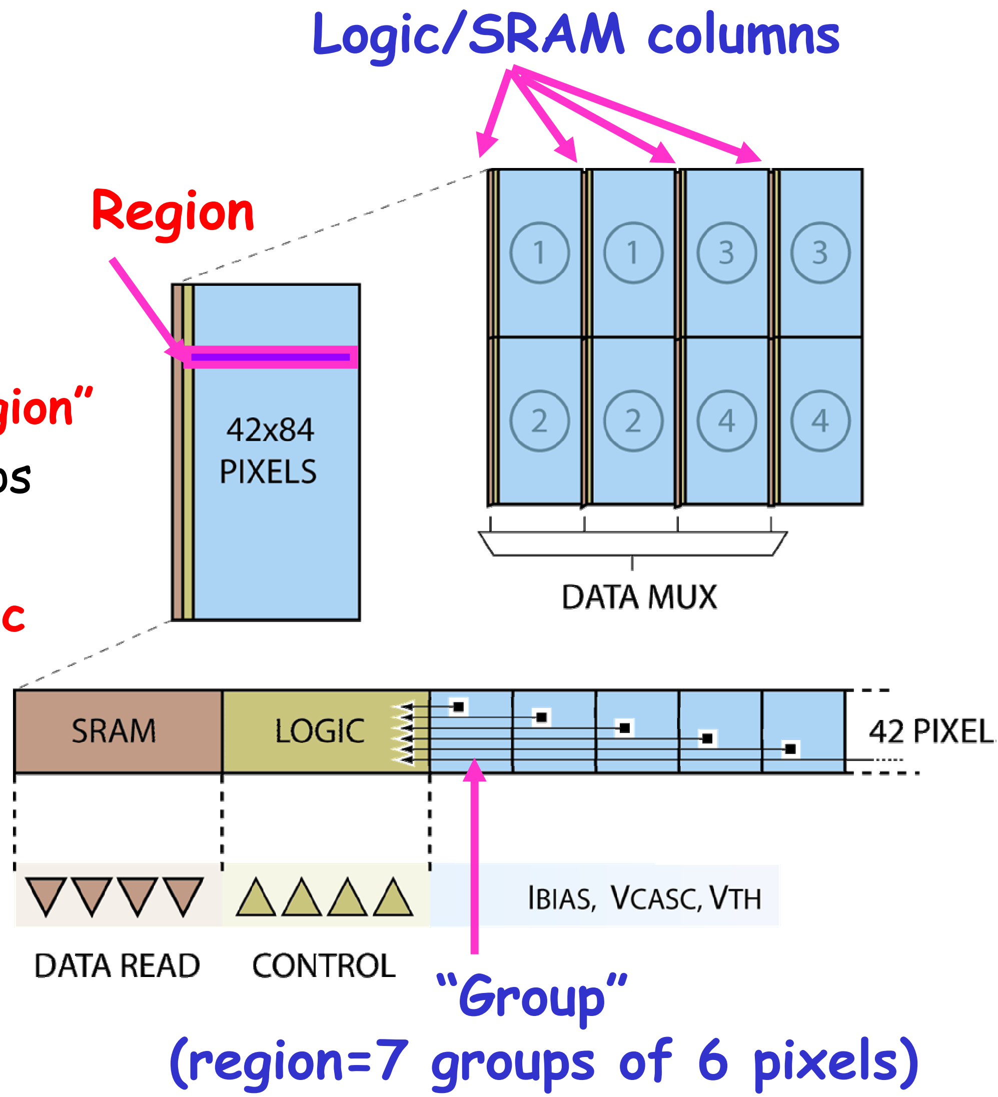
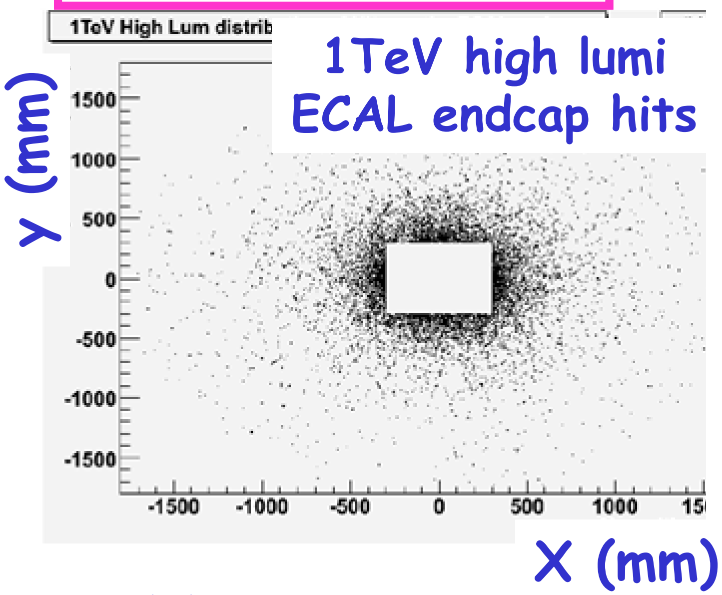


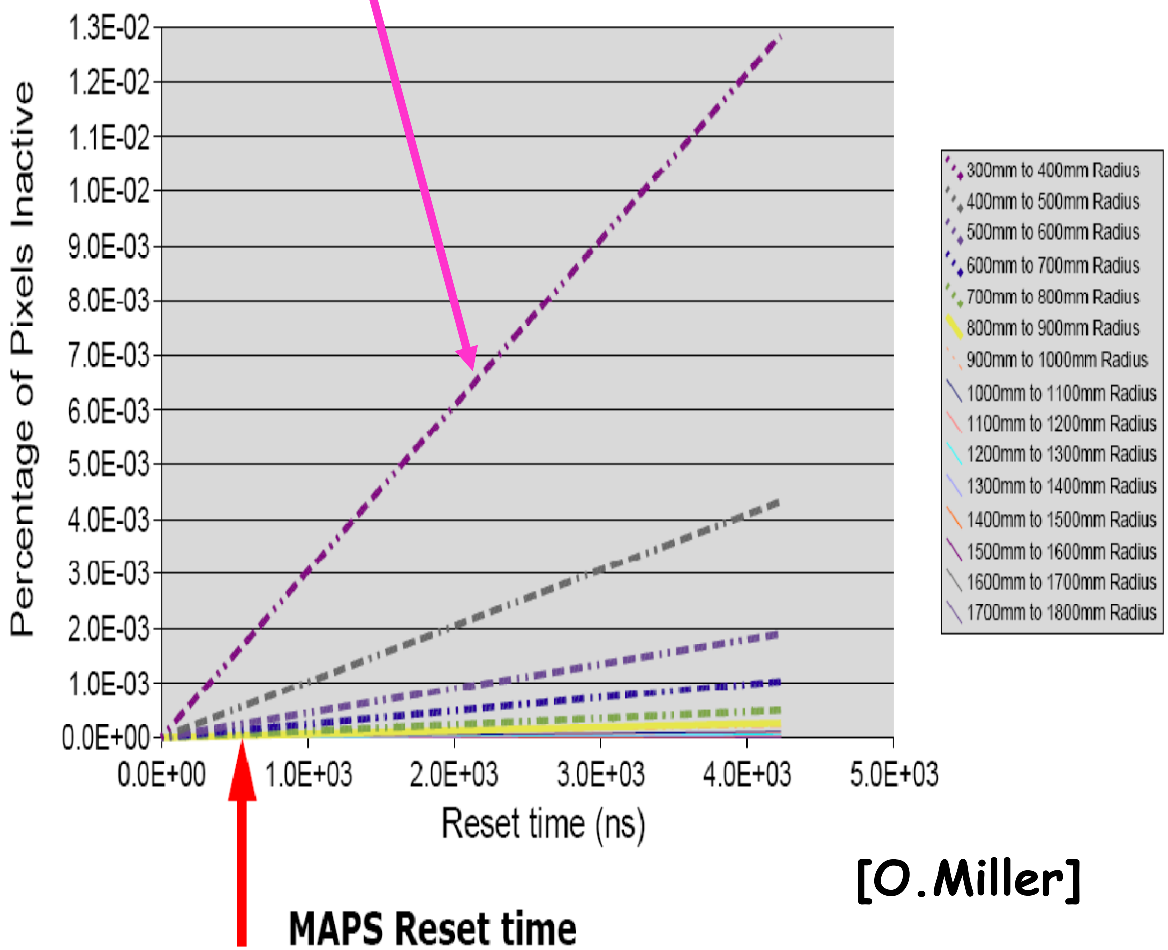
Beam background

- Beam-beam interaction by GUINEAPIG
- LDC01sc (Mokka)
- 2 machine scenarios :
  - 500 GeV baseline,
  - 1 TeV high luminosity

Repeat in SiD01, verify optimisation



purple = innermost endcap radius
500 ns reset time Ł ~ 2‰ inactive pixels



[O.Miller]

Progress with sensor tests

SID Workshop
SLAC January 2008

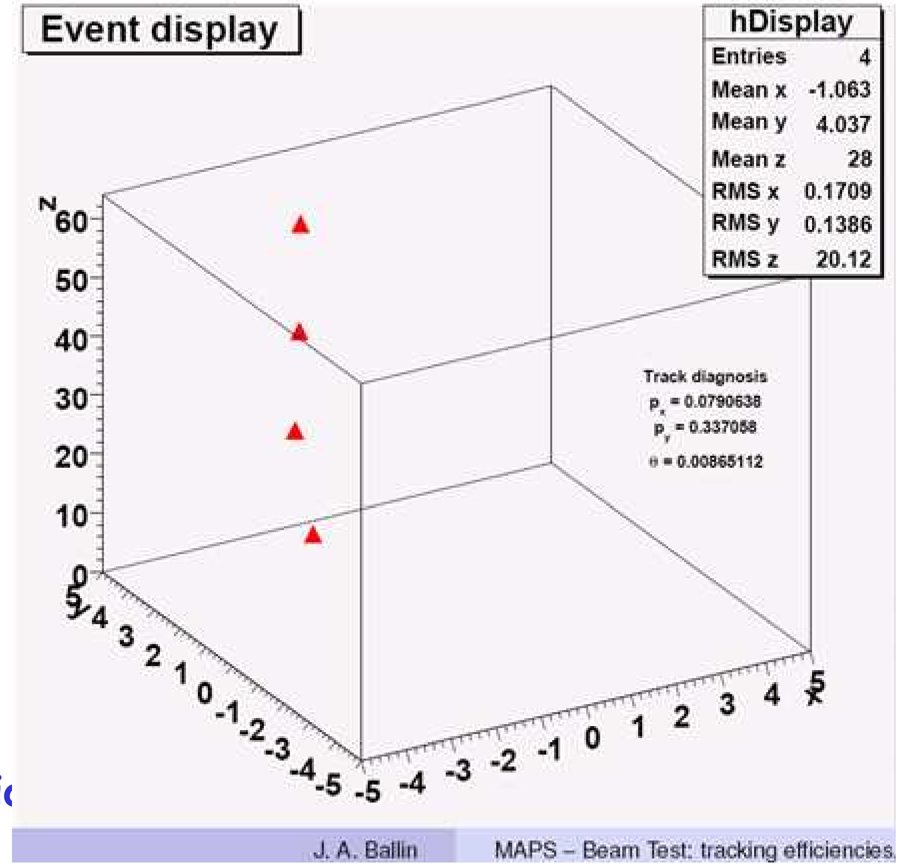
Sensor testing

- Started testing program using several set-ups
  - Laser setup
    - analog characteristics
    - Pixel tests
  - Source runs with ^{55}Fe and ^{90}Sr
  - Test beam

- **Work ongoing to test unformity of threshold and gain**
- **Report today on testbeam**

MAPS testbeam

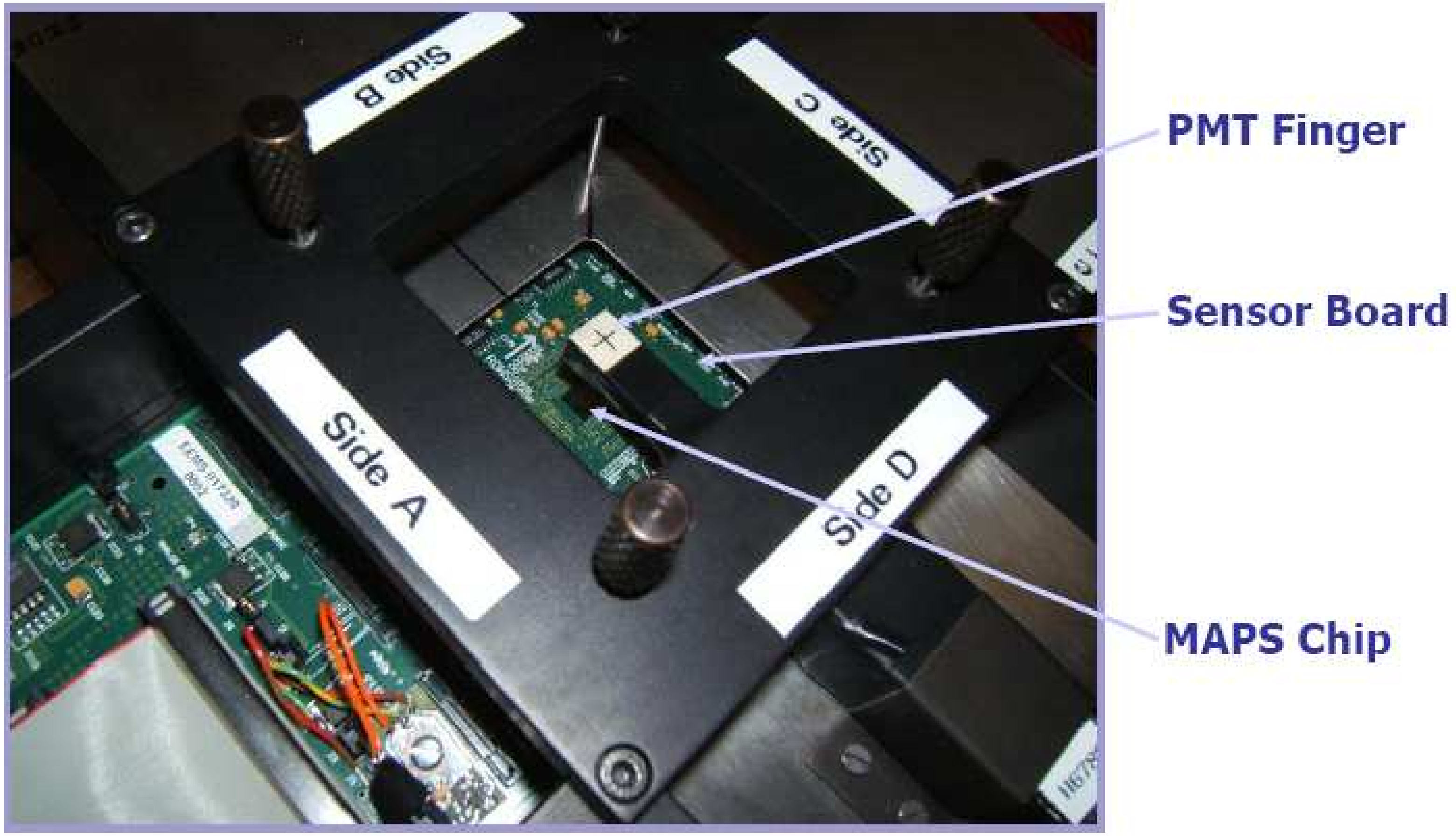
- Desy 10-17 Dec. 2007 (or + 9 months)
  - Extremely tight schedule…
- 4 sensors, PMT pair
  - 3, 6 GeV e^-
  - With/without W pre-shower material
  - Threshold scans
- Design allows to cope with pixel-to-pixel variations
  - Foreseen to calibrate channel-by-channel (no built in calib$^{n.}$)
- As we had
  - Moderate pixel-pixel variations
  - Insufficient time before beam test
- Forced to set high threshold to keep noise/rate acceptable for reliable operatio
  - Ran without problems for whole run
- Will not quote efficiency today



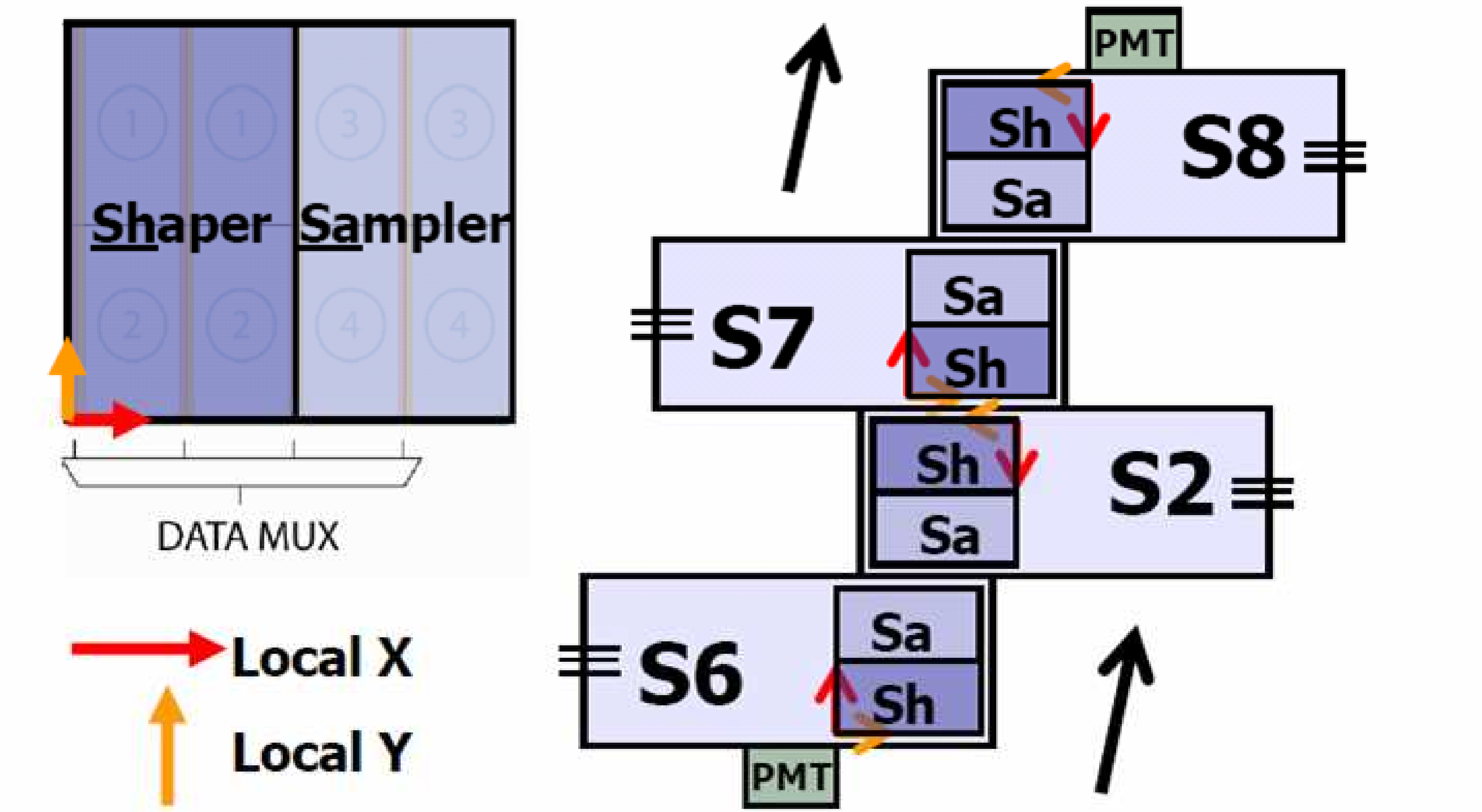
USB_DAQ crate

Experimental area

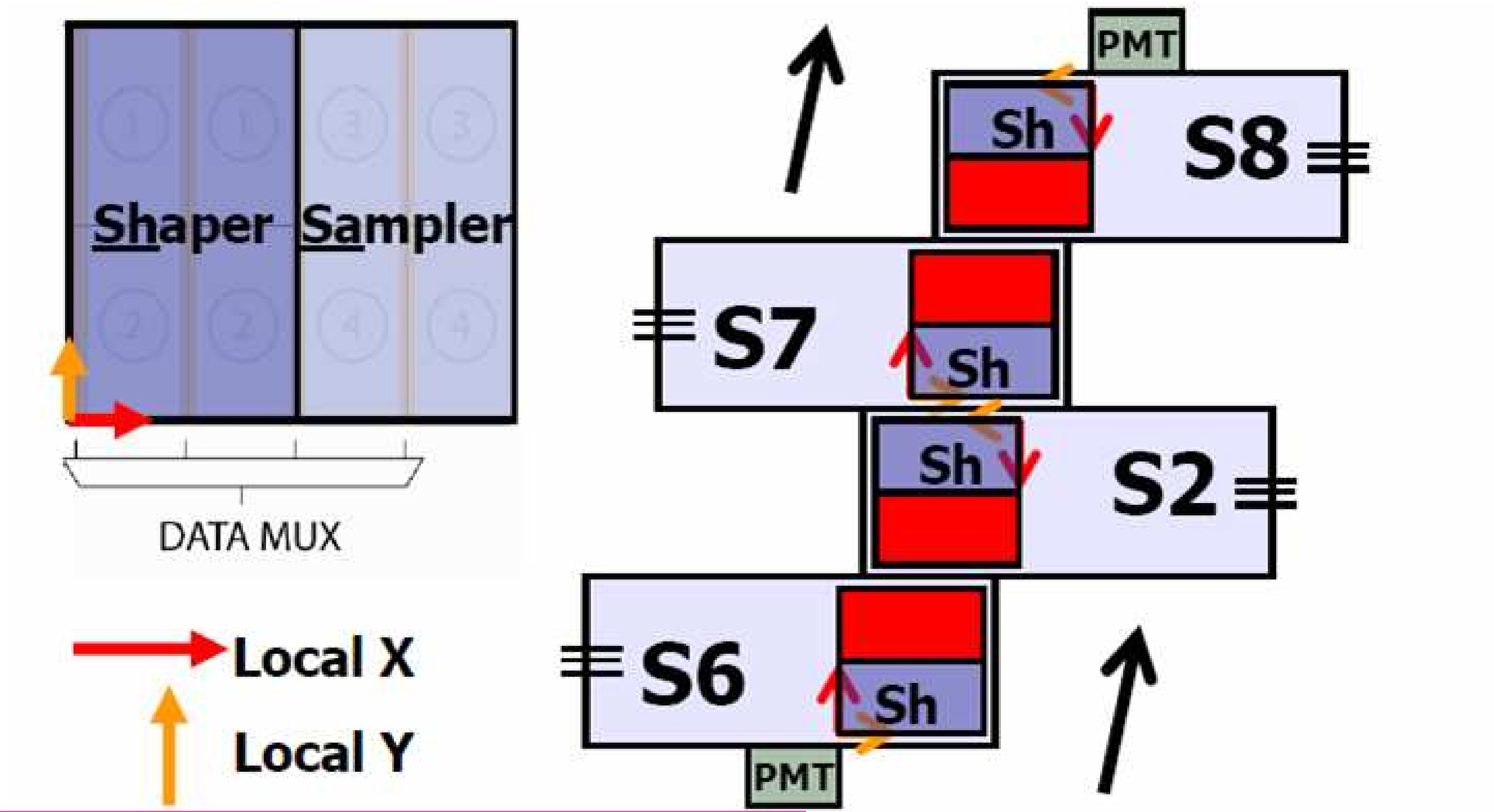
PMT trigger



Sensor setup in testbeam



Concentrate on shapers

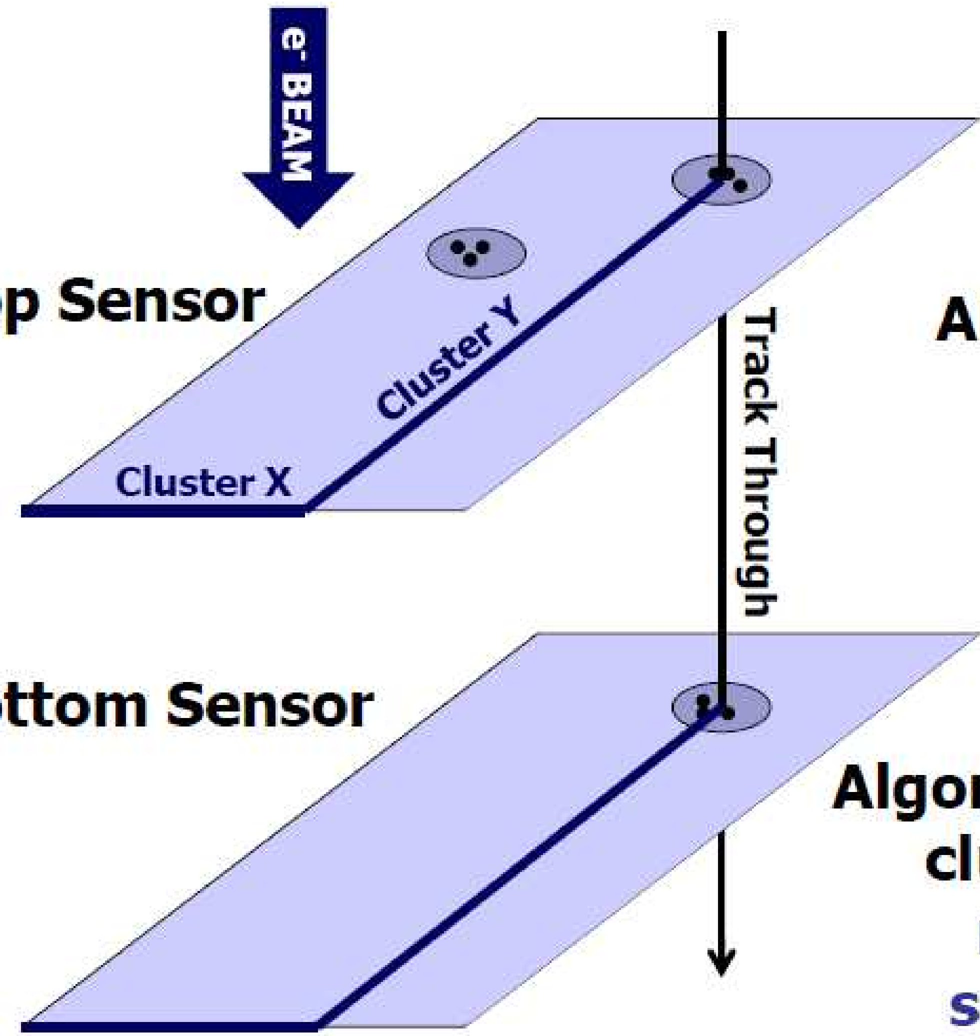


Concentrate on a single pixel variant
"Like-with-like" comparison
Two overlapping layers

Strategy

- Want to start with the highest purity sample we can
- Scintillators behaviour “not optimal”
- Ensure sensor hits genuine
  - Use clusters of hits initially, not single pixels
- Can we match clusters between sensors?

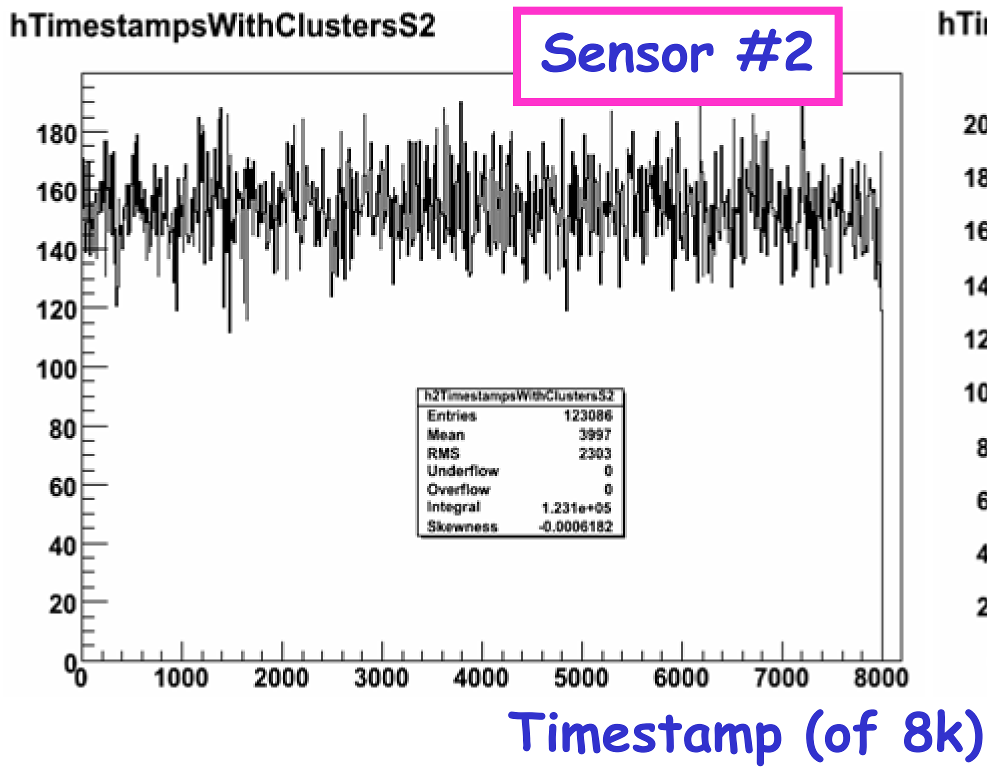
Clustering

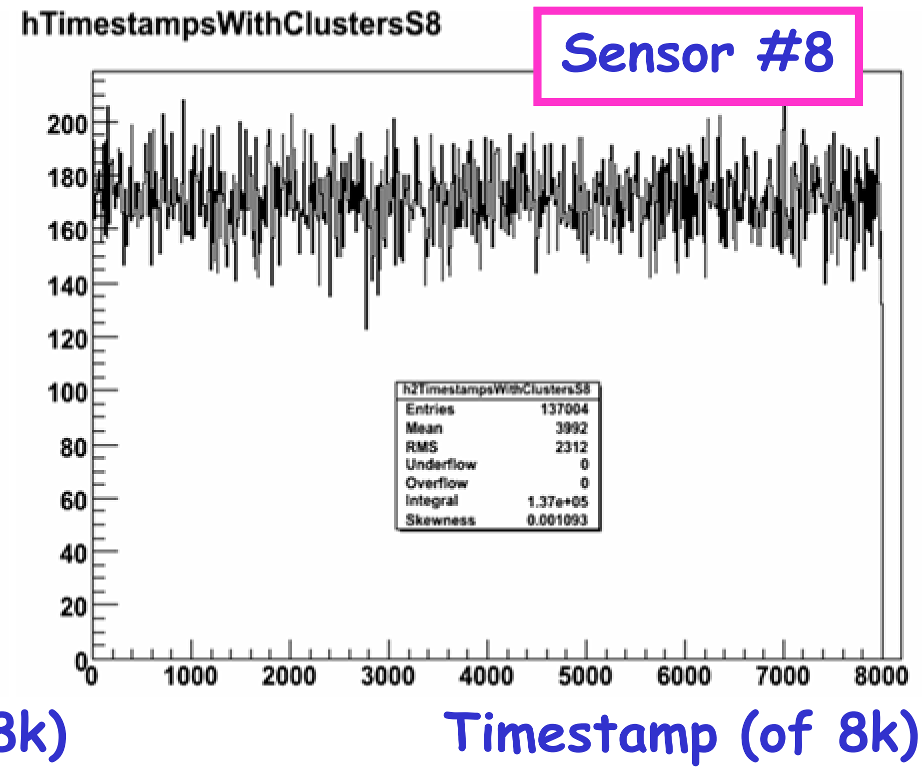


All happening in **1 time stamp**.

Algorithm matches clusters with **minimum separation**.

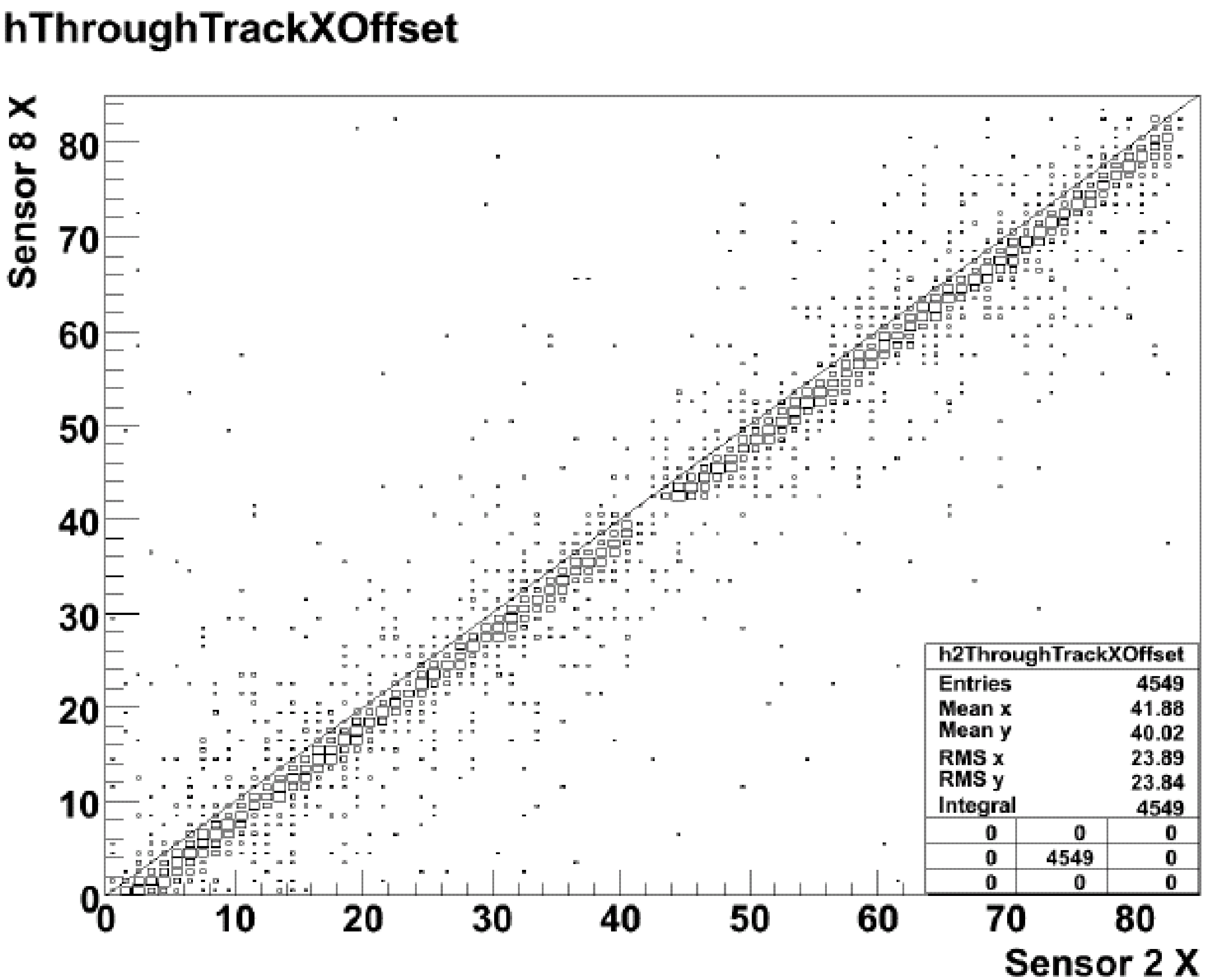
Timestamp within train



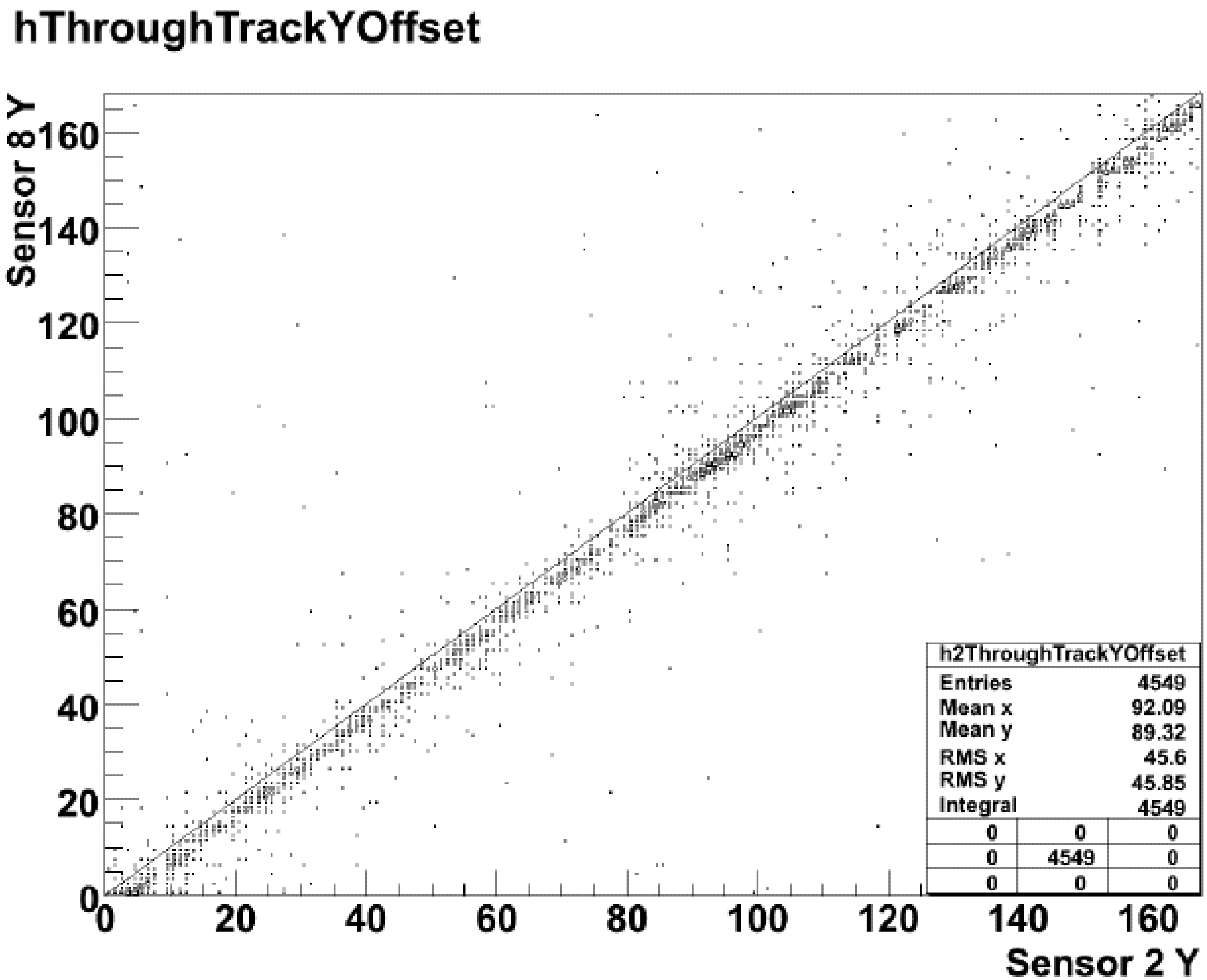


- Basic data validity check
- Clusters uniform in timestamp within train
- Indicates buffers not saturating

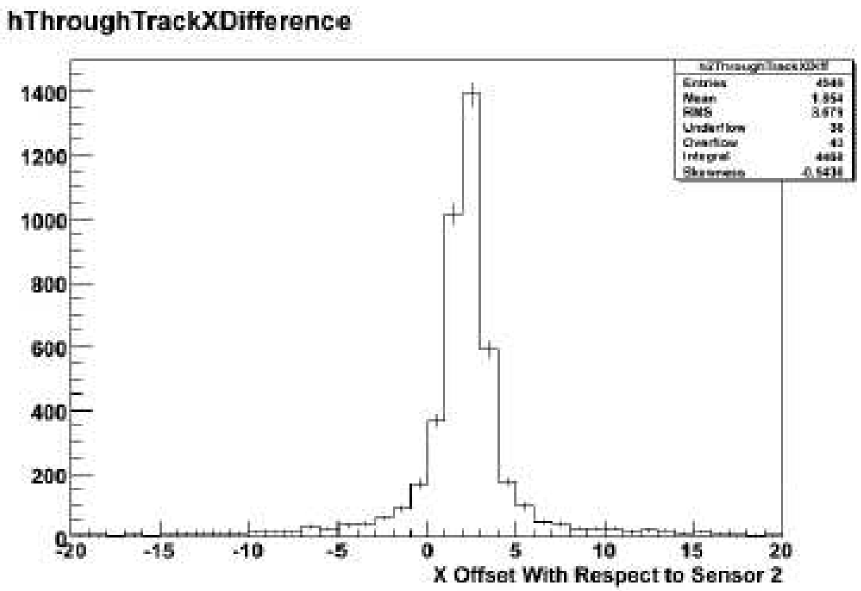
Layer-layer correlations: x

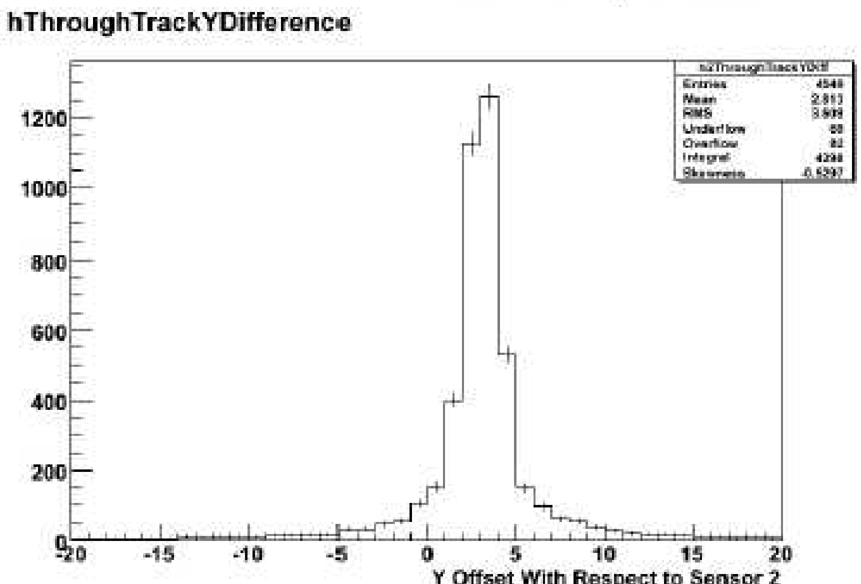


Layer-layer correlations: y



Layer-layer alignment





- Look at absolute offset of the matched cluster on S8 with respect to S2's coordinate system.
- Find strongly correlated offset of (3,4) pixels.
- Most likely cause, relative sensor alignment.
- Still, taking all equipment setup into account a, 250 μm offset is very good!

Summary

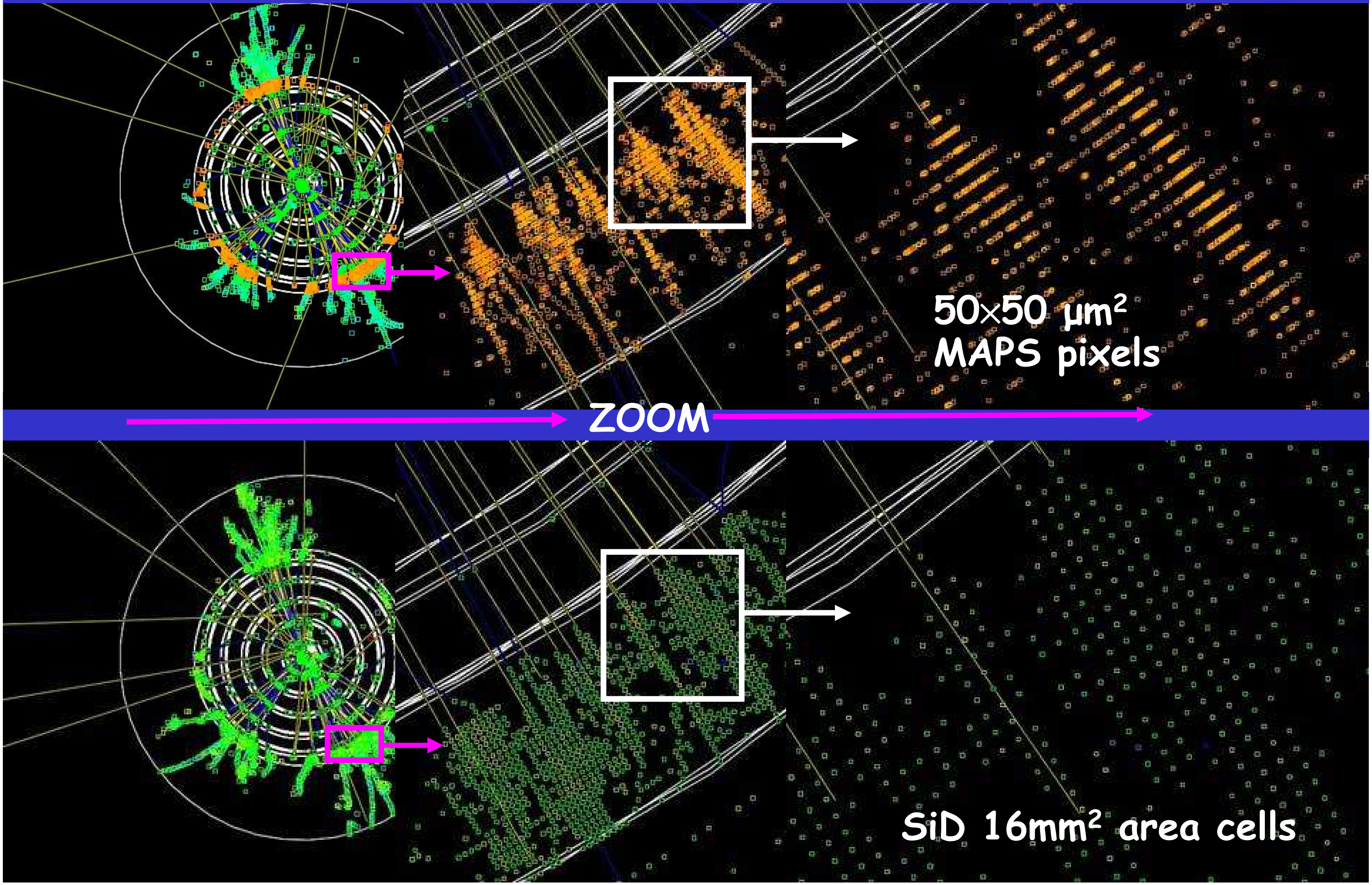
- MAPS ECAL: alternative to baseline design (analogue SiW)
  - Multi-vendors, cost/performance gains
  - New INMAPS deep p-well process (optimise charge collection)
  - Four architectures for sensor on first chips
  - Tests of sensor performance ongoing
  - Physics benchmark studies to evaluate performance relative to standard analogue Si-W designs for SiD (also ILD)

Future plans

- **Recognised as "generic" sensor technology with "generic" applications**
- **Much interest to continue development of concept for ECAL**
  - **Including for SiD**
- Systematic studies of pixel to pixel gain and threshold variations
  - Absolute gain calibration
  - Second sensor…

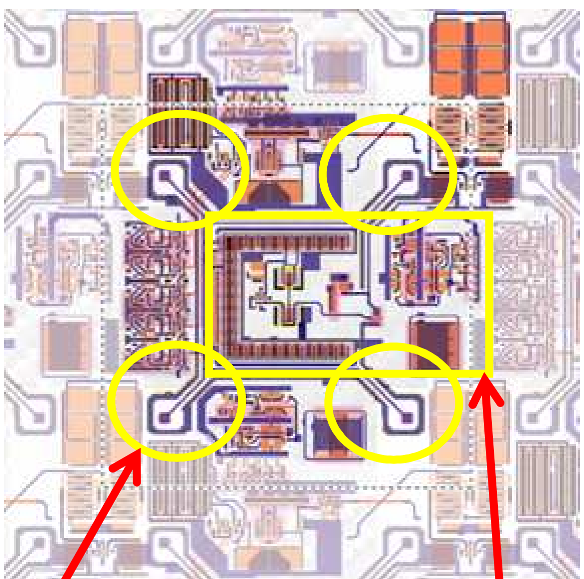
Backup/spares

Tracking calorimeter



CALICE INMAPS TPAC1

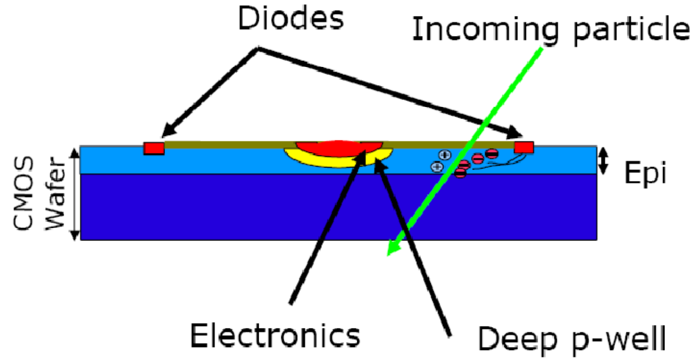
First round, four architectures/chip
(common comparator+readout logic)



4 diodes
Ø 1.8 μm

Architecture-specific
analogue circuitry

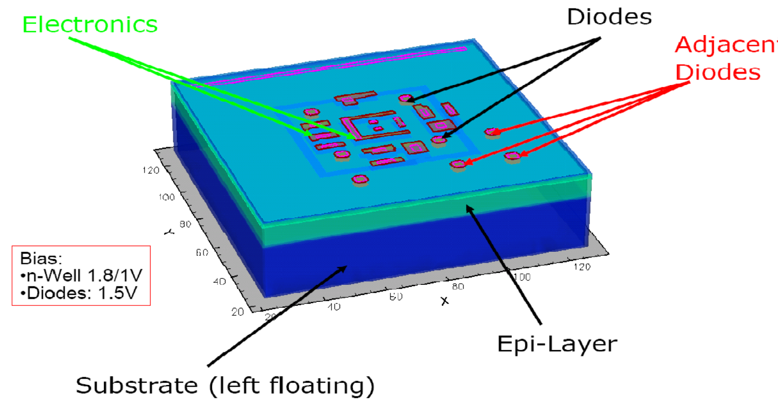
0.18μm feature size



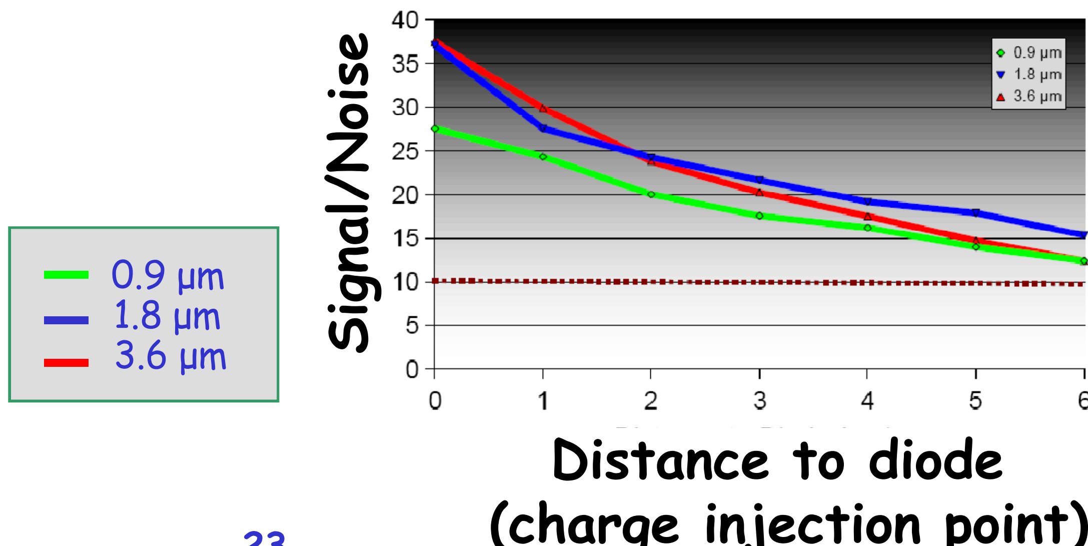
INMAPS process: deep p-well implant 1 μm thick under electronics n-well, improves charge collection

Device level simulation

- Physics data rate low – noise dominates
- Optimised diode for
  - Signal over noise ratio
  - Worst case scenario charge collection
  - Collection time

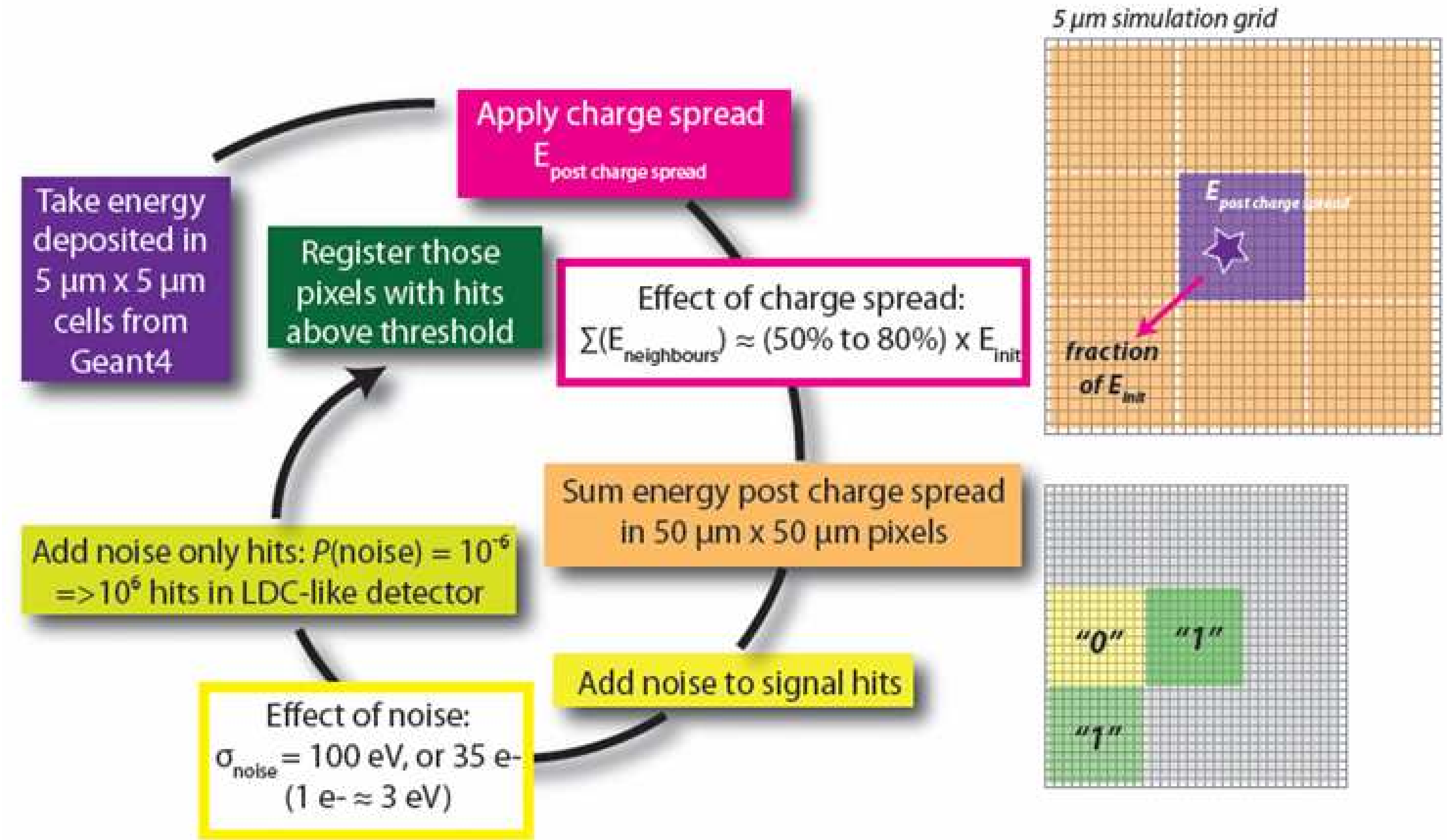


Signal/noise



Attention to detail 1: digitisation

Digital ECAL, essential to simulate
charge diffusion, noise, in G4 simulations



[J.Ballin/A-M.Magnan]

System considerations

- A Tera-Pixel ECAL is challenging
- Benefits
  - No readout chips
  - CMOS is well-known and readily available
  - Ability to make thin layers
- Current sources of concern
  - DAQ needs
  - Power consumption/Cooling

DAQ requirements

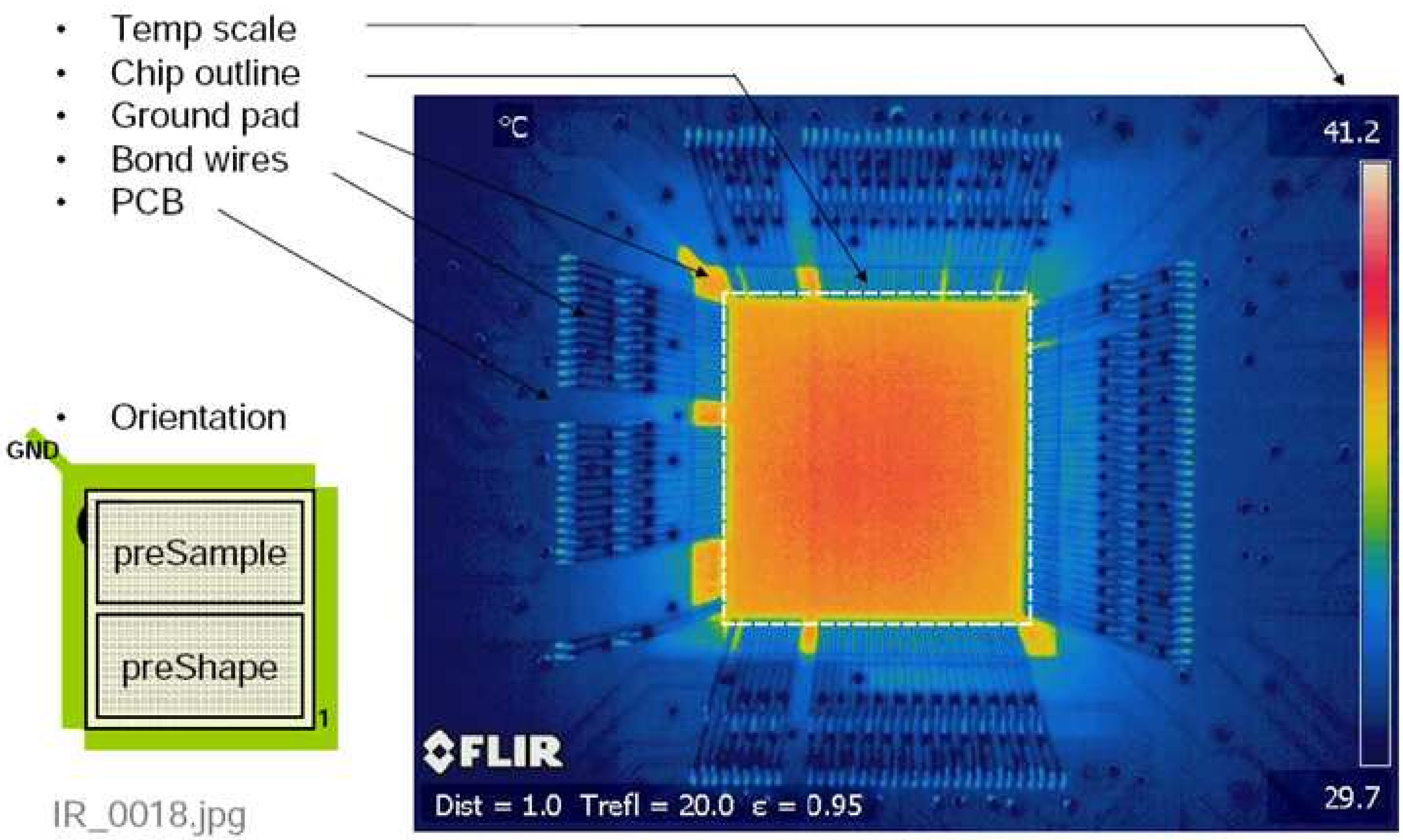
- $O(10^{12})$ channels are a lot ...
- Physics rate is not the limiting factor
- Beam background and Noise will dominate
- Assuming 2625 bunches and 32 bits per Hit
  - 10^6 Noise hits per bunch
  - ~O(1000) Hits from Beam background per bunch (estimated from GuineaPIG)
- Per bunch train
  - ~80 Gigabit / 10 Gigabyte
  - Readout speed required 400 Gigabit/s
  - CDF SVX-II can do 144 Gigabit/s already

Cooling and power

- Cooling for the ECAL is a general issue
- Power Savings due to Duty Cycle (1%)
- Target Value for existing ECAL ASICS
  - 4 μW/mm2
- Current Consumption of MAPS ECAL:
  - 40 μW/mm2 depending on pixel architecture
  - TPAC1 not optimized at all for power consumption
- Compared to analog pad ECAL
  - Factor 1000 more Channels
  - Factor 10 more power
- Advantage: Heat load is spread evenly

Thermal properties

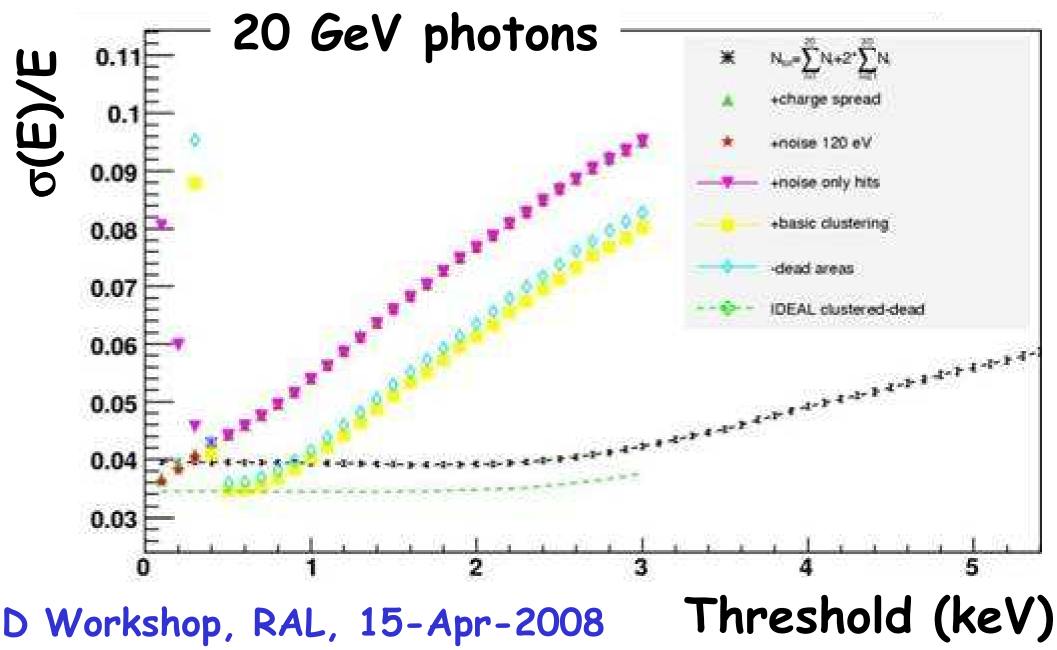
Orientation: Chip top view

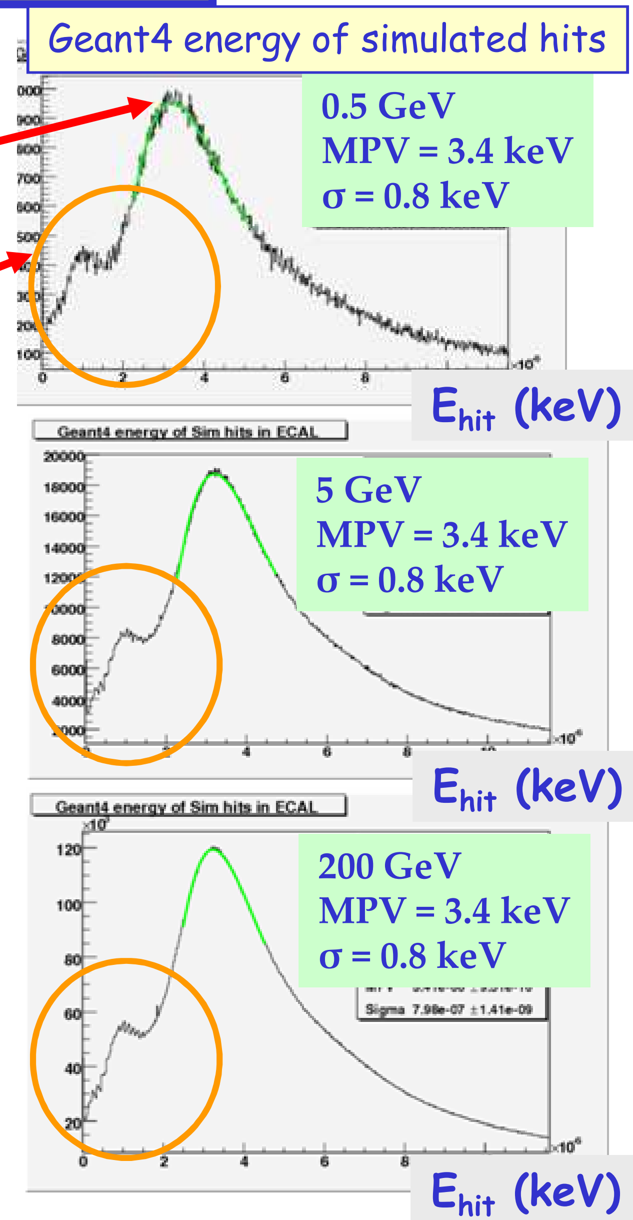


[Marcel Stanitzki]

Physics simulation

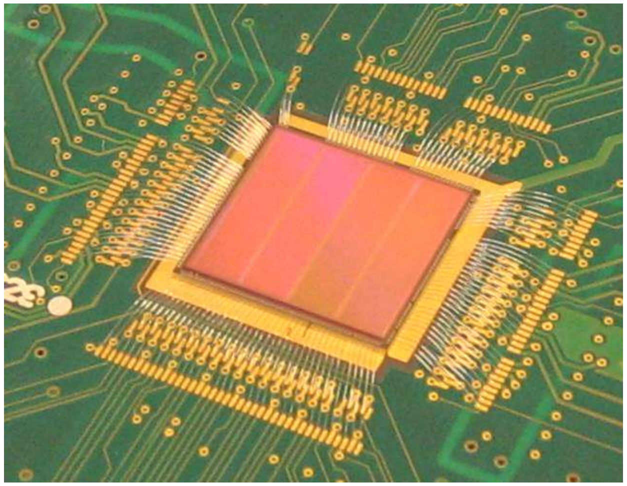
- MAPS geometry implemented in Geant4 detector model (Mokka) for LDC detector concept
- Peak of MIP Landau stable with energy
- Definition of energy: E α N_{pixels}
- Artefact of MIPS crossing boundaries
  - Correct by clustering algorithm
- Optimal threshold (and uniformity/stability) important for binary readout





The CALICE TPAC1

- 50x50 μm cell size
- Comparator per pixel
- Capability to mask individual pixels



- 4 Diodes for ~uniform response w.r.t threshold
- 13 bit time stamp (>8k bunches individually tagged)
- Hit buffering for entire bunch train (~ILC occupancy)
- Threshold adjustment for each pixel
- Usage of INMAPS (deep-p well) process

[Marcel Stanitzki]