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Off-detector & Software development of DAQ System for the EUDET calorimeters

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EUDET DAQ Targets

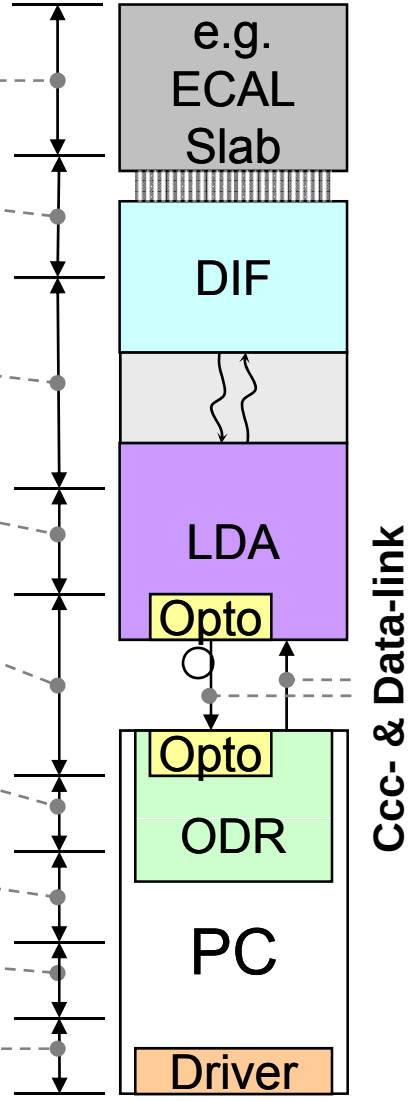
- Maximizing to use of off-the-shelf commercial components, cheap, scalable and maintainable
- Provide well-defined interfaces between DAQ components to allow for minimizing costs and development cycles;
- A control system to easily integrate the rest of sub-systems of detectors
- Software to build events from bunch train data and disparate sources into single event data
- Manage network and data storage

DAQ Mechanical Design targets

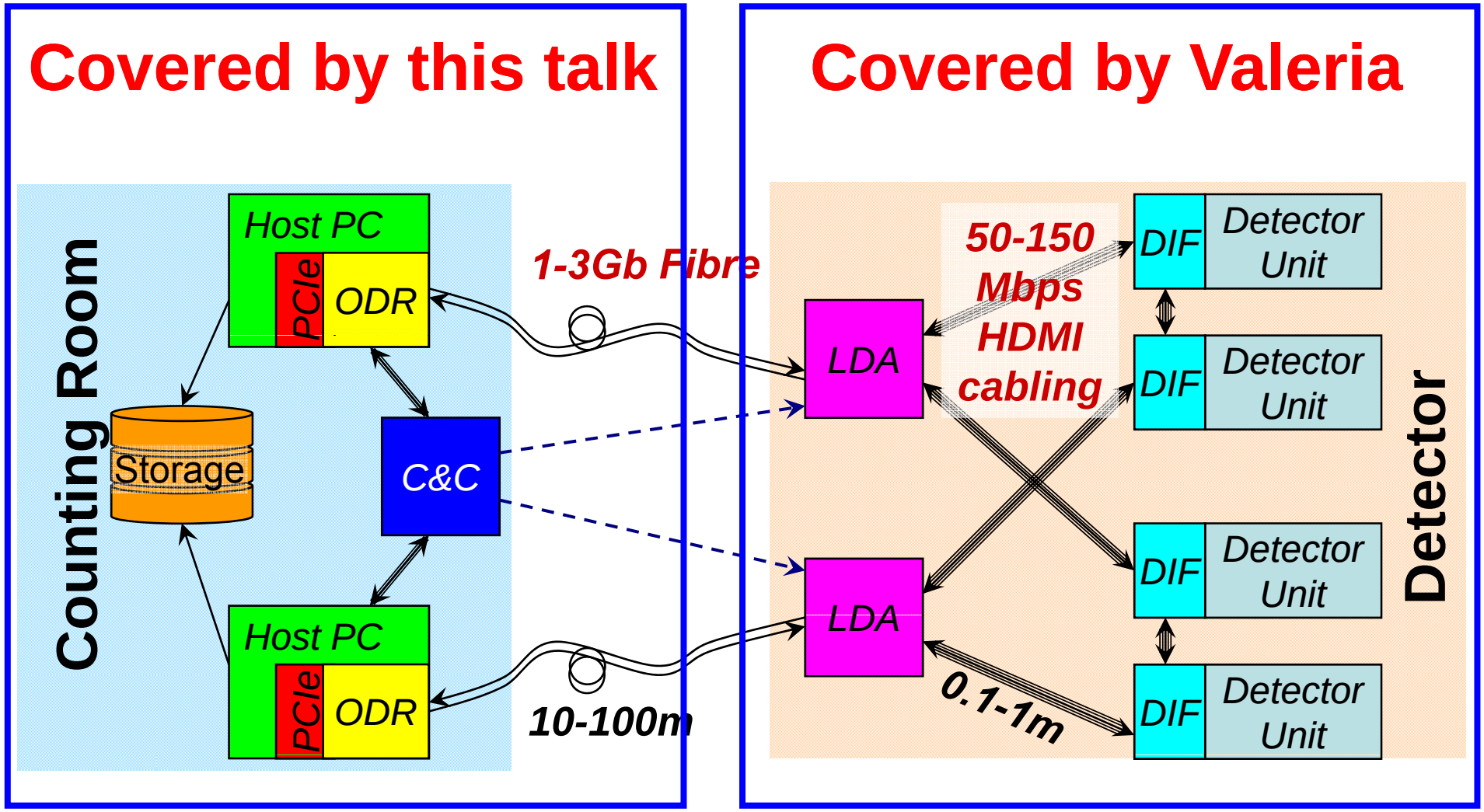
- Targeting EUDET Module and ILC/CALICE;
- Aim to develop a generic system e.g. ECAL/HCAL
- Triggerless DAQ system: use C&C instead
  - All data are sent off detector within a bunch train
  - Use bunch struct. as advantages: 1ms in bunch train, read out data within 200ms of inter-train gap;
- DAQ system will also control power cycling of readout ASICs
- A funnel-like DAQ to collect, wrap and transmit data in stages before sending to central storage

DAQ Architecture Overview

- Slab hosts VFE chips (ASICs)
- **Detector Interface** connected to Slabs
- LDA servicing DIFs
- **Link/Data Aggregator**
- LDAs read out by ODR via opto-links
- **Off-Detector Receiver**
- PC hosts ODR
  - PCI-Express driver software
- Local Software DAQ
- Full blown Software DAQ

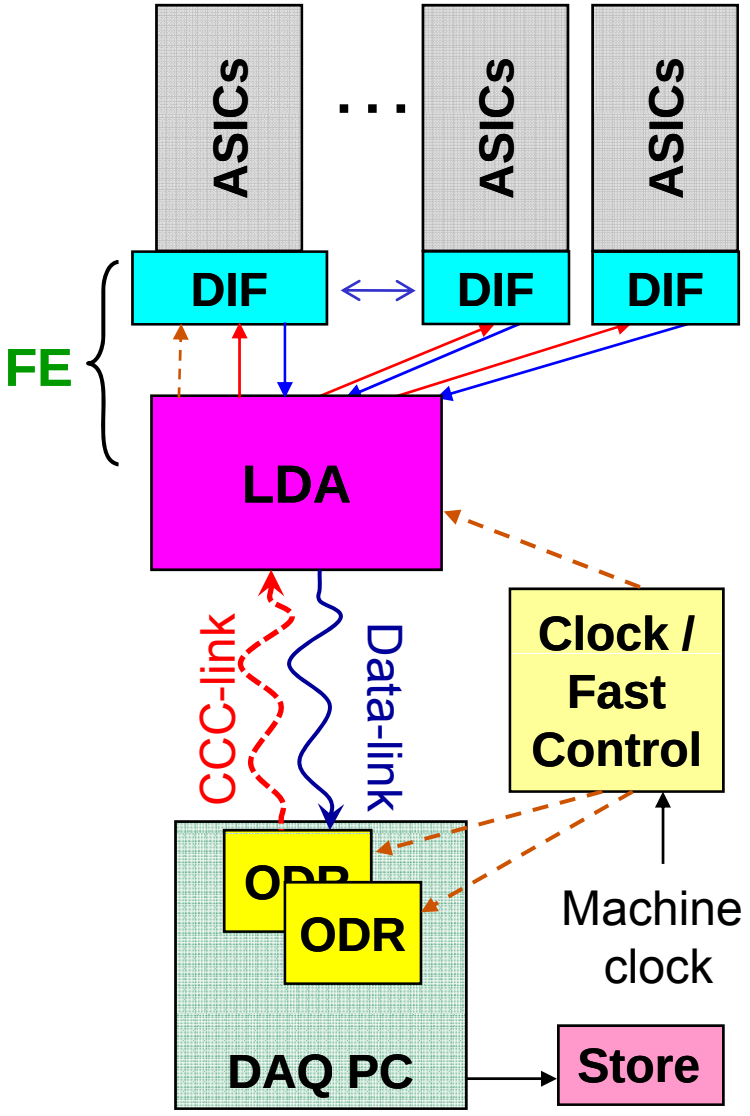


DAQ Architecture Hierarchy



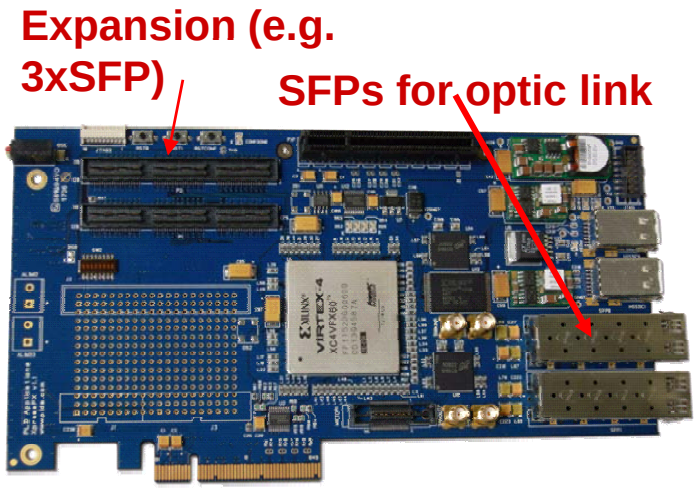
Current Architecture: ODR

- Assemble data into a usable form for processing
- Logical tasks:
  - Receive from LDA
  - Process e.g. event building
  - Store
- Current input is Ethernet for testing performance
  - Internal FPGA test data generator;
  - External data stream via network



Off Detector Receiver (ODR)

- Receives modularized data from LDA
  - Realized as PCI-Express card, hosted in DAQ PC.
  - 1-4 Opti-links/card (Gigabit), 4 LDAs/card, 1-2 cards/PC
  - Buffers and transfers to store as fast as possible
- Sends controls and configs to LDA for distribution to DIFs
- Performance studies & optimisation on-going

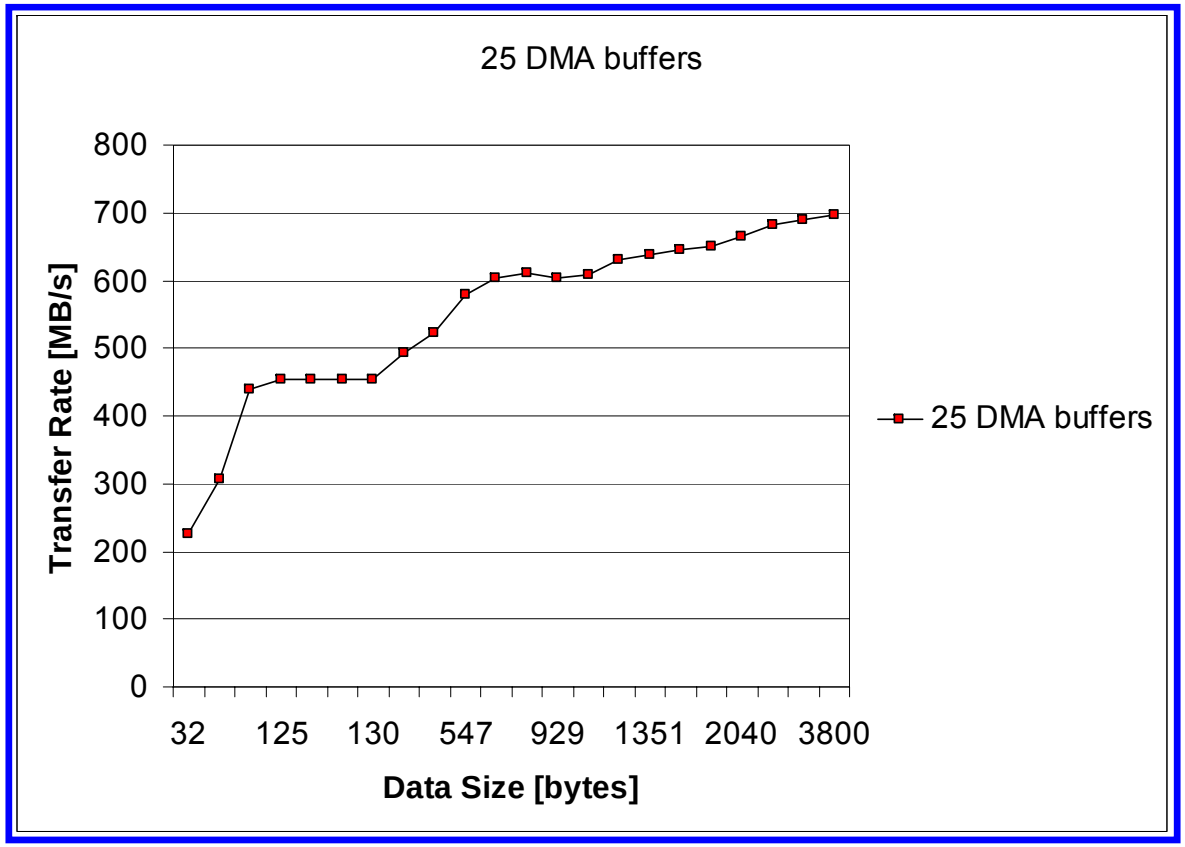


Hardware:

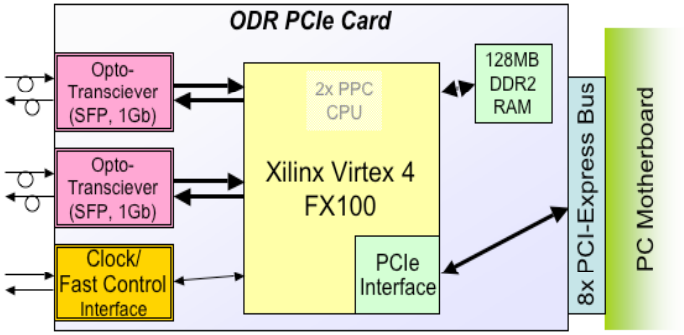
- Using commercial FPGA dev-board:
  - PLDA XPressFX100
  - Xilinx Virtex 4, 8xPCIe, 2x SFP (3 more with expansion board)

B.G., A.M @ RHUL

ODR Data Access Rate



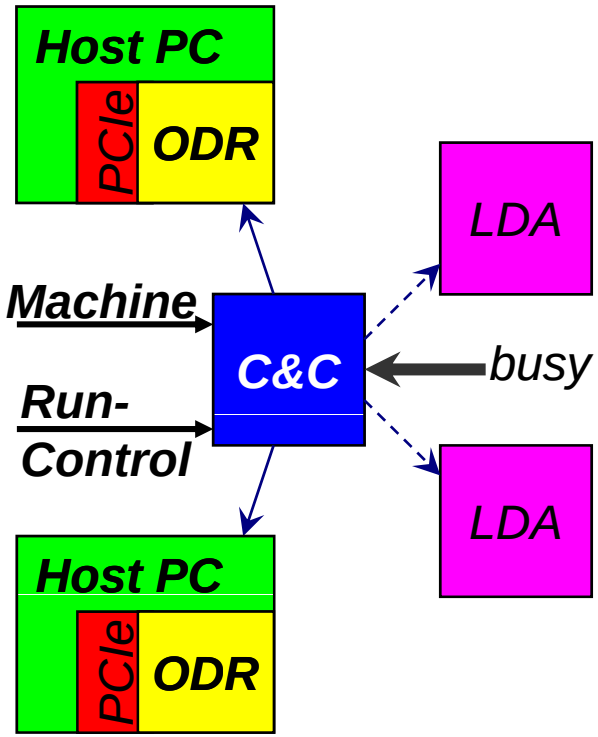
transfer the data from ODR memory to the user-program memory via 4 links
~700 MByte/sec
by 25 DMA buffers



All measurements: single requester thread,
no disk write, data copied to the host memory.

B.G., A.M @ RHUL

Clock & Control (C&C) board

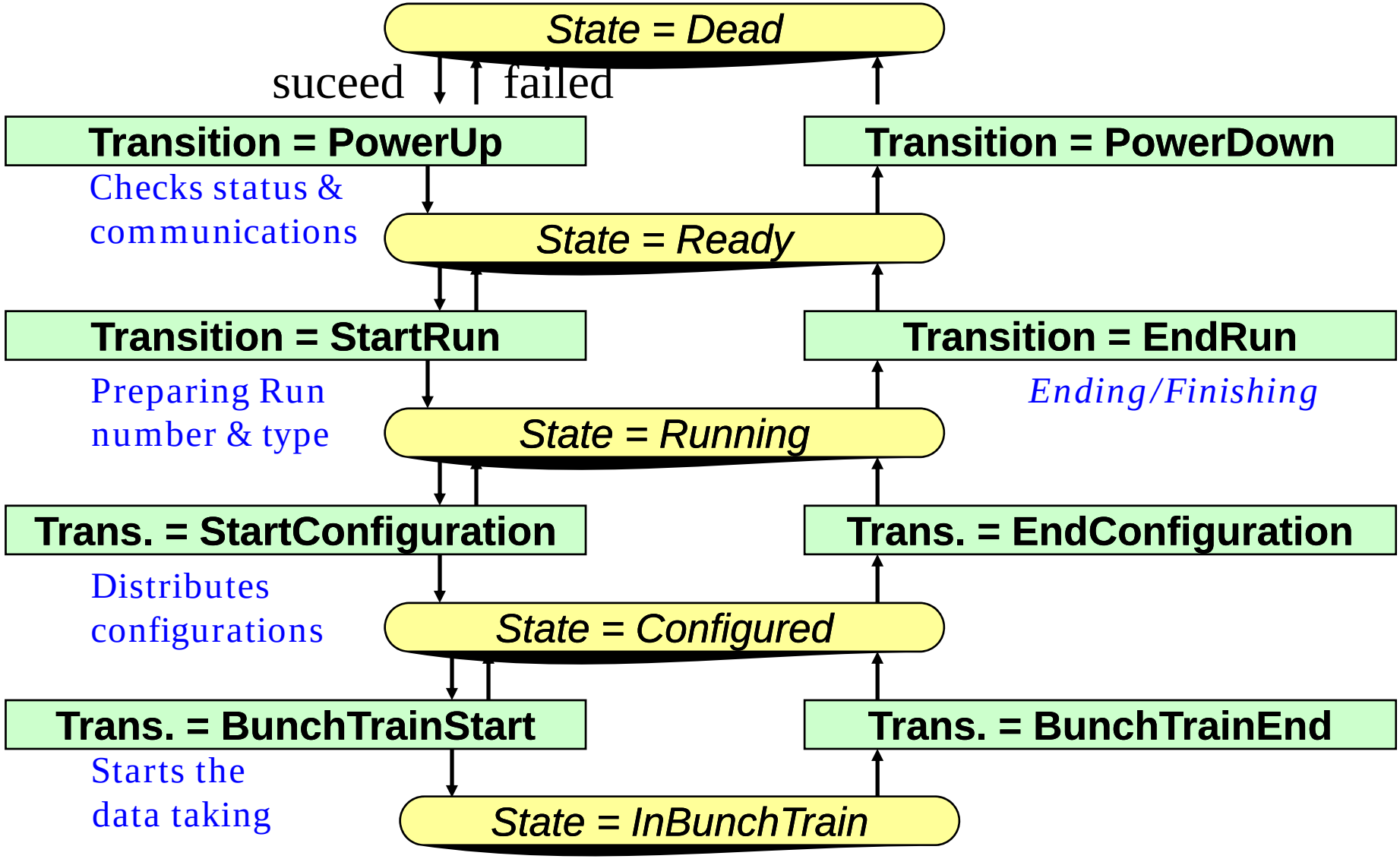


- C&C unit provides machine clock and fast signals to 8x ODR/LDA.
- A low jitter and fixed latency;
- Logic control (FPGA, connected via USB)
- Link Data Aggregator provides next stage fanout to Detector Interfaces
  - Eg C&C unit →8 LDAs →8 DIFs = 64 DUs.
- Signalling over same HDMI type cables
- Facility to generate optical link clock (~125-250MHz from ~50MHz machine clock)

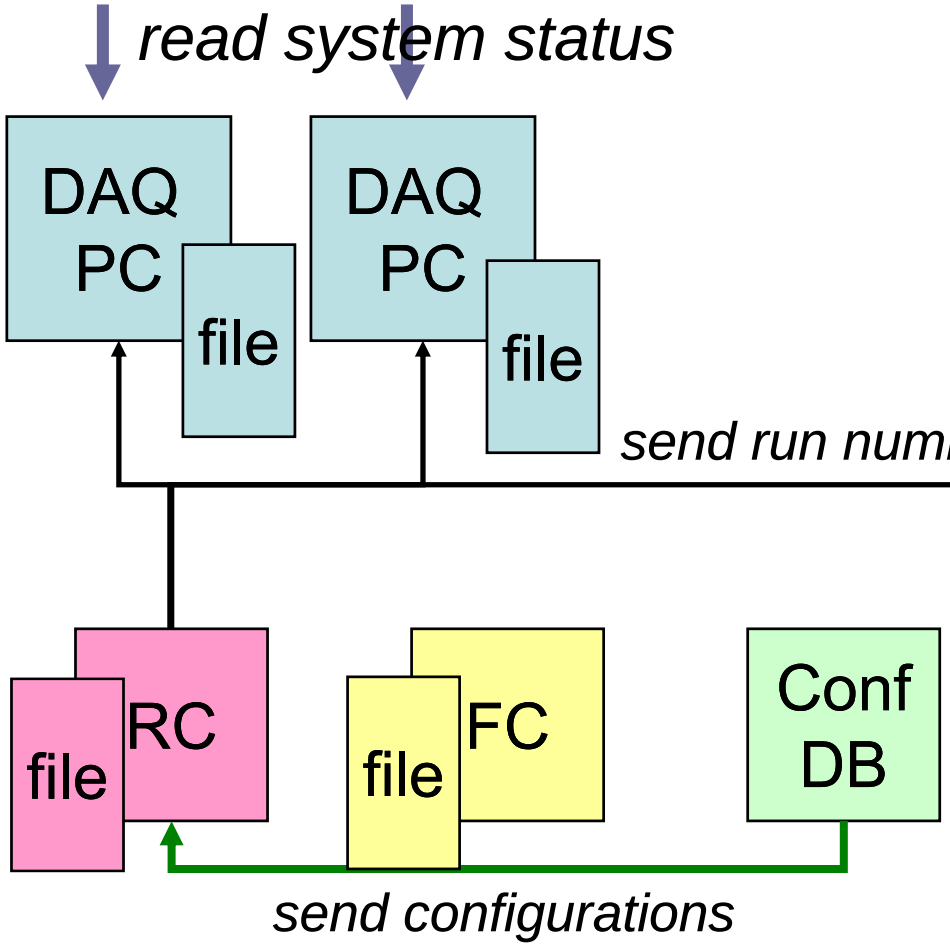
Board is already designed, will be build soon

M.P., UCL

EUDET DAQ software: State



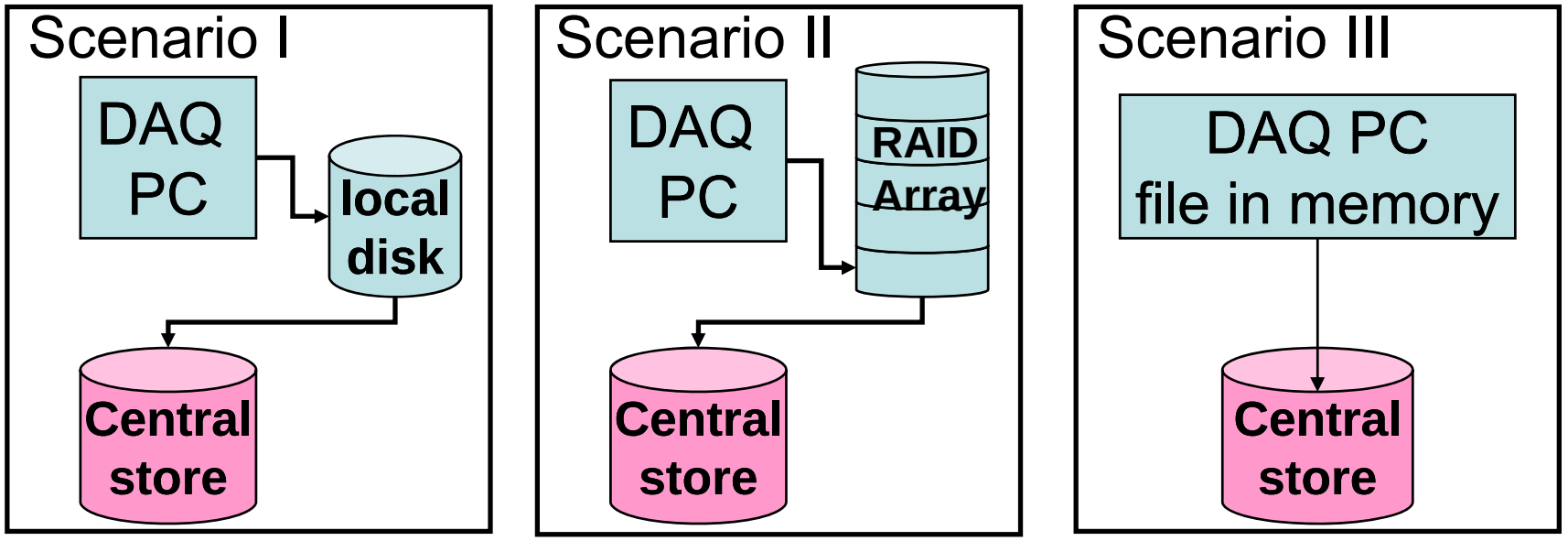
Transition: StartRun



Files to be written for book keeping:

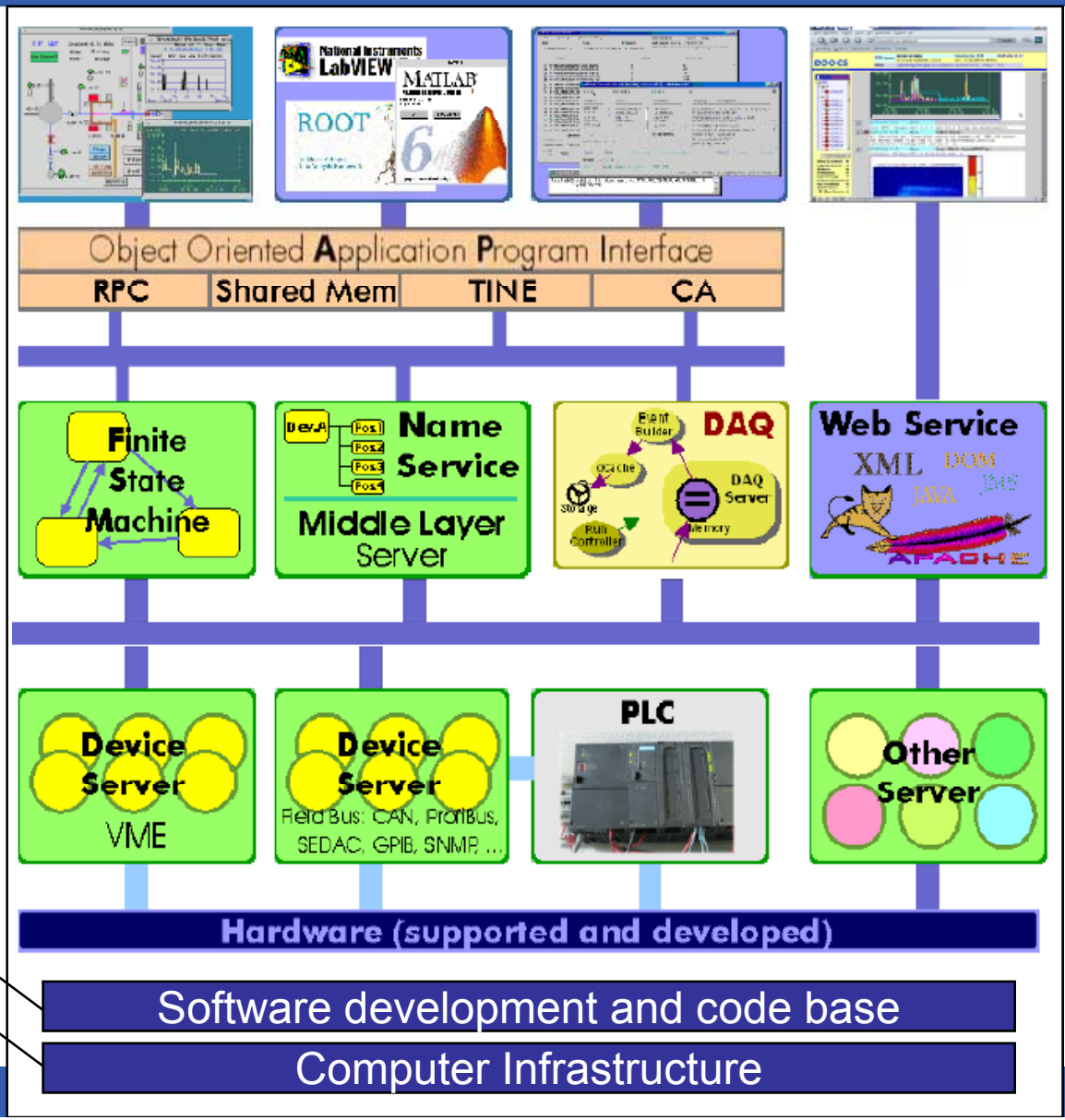
- system status by DAQ PC
- run info by RC PC
- system status by FC

Data Storage

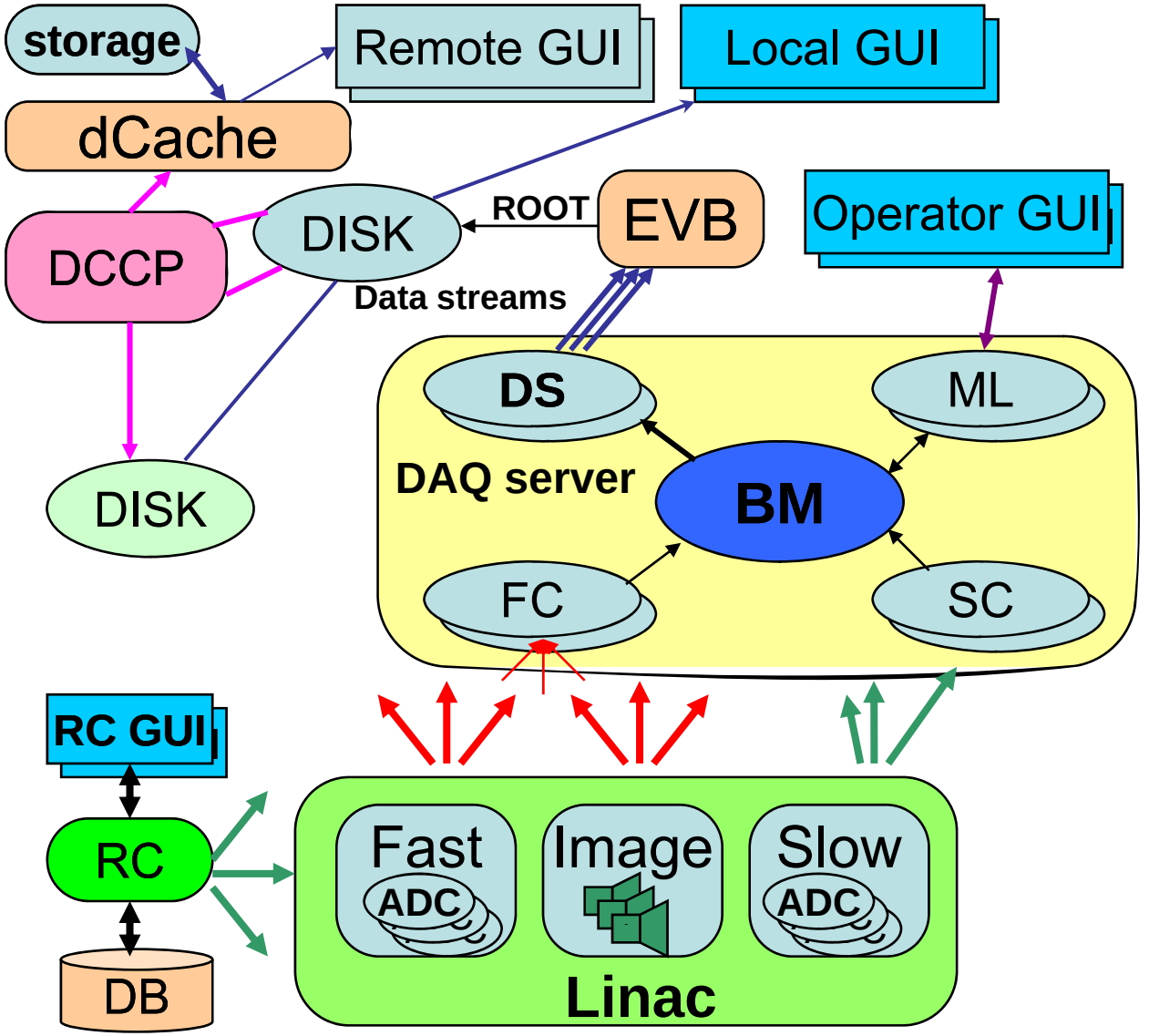


- Which scenario to choose depending on the bandwidth with which the data gets produced: **(1)** up to 200Mbit/sec, **(2)** up to ~1600Mbit/sec, **(3)** from there on
- Estimation of the data rate for the EUDET DAQ prototype has to cope with ~400Mbit/s, however it depends on the detector and the choice of VFE.

DAQ Software: **DOOCS framework**



DAQ Software of DOOCS



FC/SC:
Fast/Slow
Collector

BM:
Buffer Manager

EVB:
Event Builder

DS:
DAQ Server

Adapting DOOCS to EUDET DAQ

- Modeling hardware card via device server
  - Existing: VME, Sedac, Profi-Bus; ***ODR/LDA/DIF/ASICs***
- **Equipment Name Server** (ENS):
  - Facility(**F**) / Device(**D**) / Location(**L**) / Property (**P**)
  - e.g. *CALICE.ECAL*/*ODR*/*ODR1*/*Status*
    - F: CALICE.ECAL, CALICE.AHCAL, CALICE.DHCAL
    - D: ODR, LDA, DIF, ASICs;
    - L: ODR1,ODR2,ODRX; LDA1,LDA2,LDAX; DIF1,DIF2,DIFX;
    - Property: X X X ?
- Build interface talking to hardware (ODR) as a starting point;
- Classify the properties and functionalities of each device for our EUDET DAQ system (DIF, LDA, ODR, etc.)

Future plans

- Classify the necessary properties and functions of all hardware components;
- Continue their building & testing, debugging & improving meanwhile;
- Continue to develop interface to hardware (ODR) talking to DOOCS;
- Investigate & define the DIF→LDA→ODR links
- How to deal with (a)synchronization for C&C?
- Putting (all) components together, test…

Summary

- Off-detector Receiver has been built for receiving, event building & data storage; its performance has been testing;
- Clock & Control instead of triggers, the board will be built soon;
- DOOCS framework is reusable & suitable for our DAQ system.
- DAQ software is in designing phase…

DAQ architecture

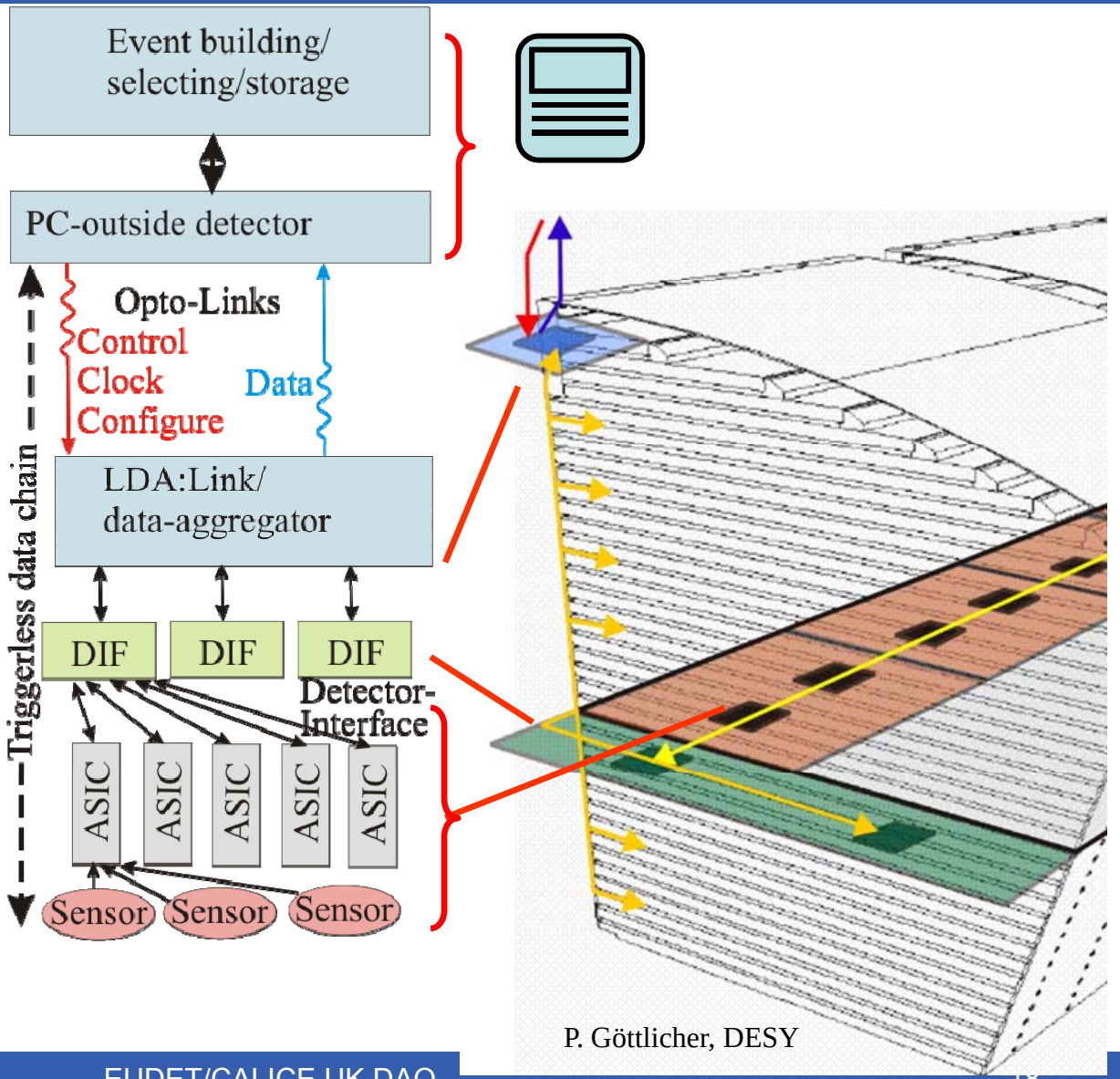
DAQ software

Off Detector Receiver (ODR)

Link Data Aggregator (LDA)

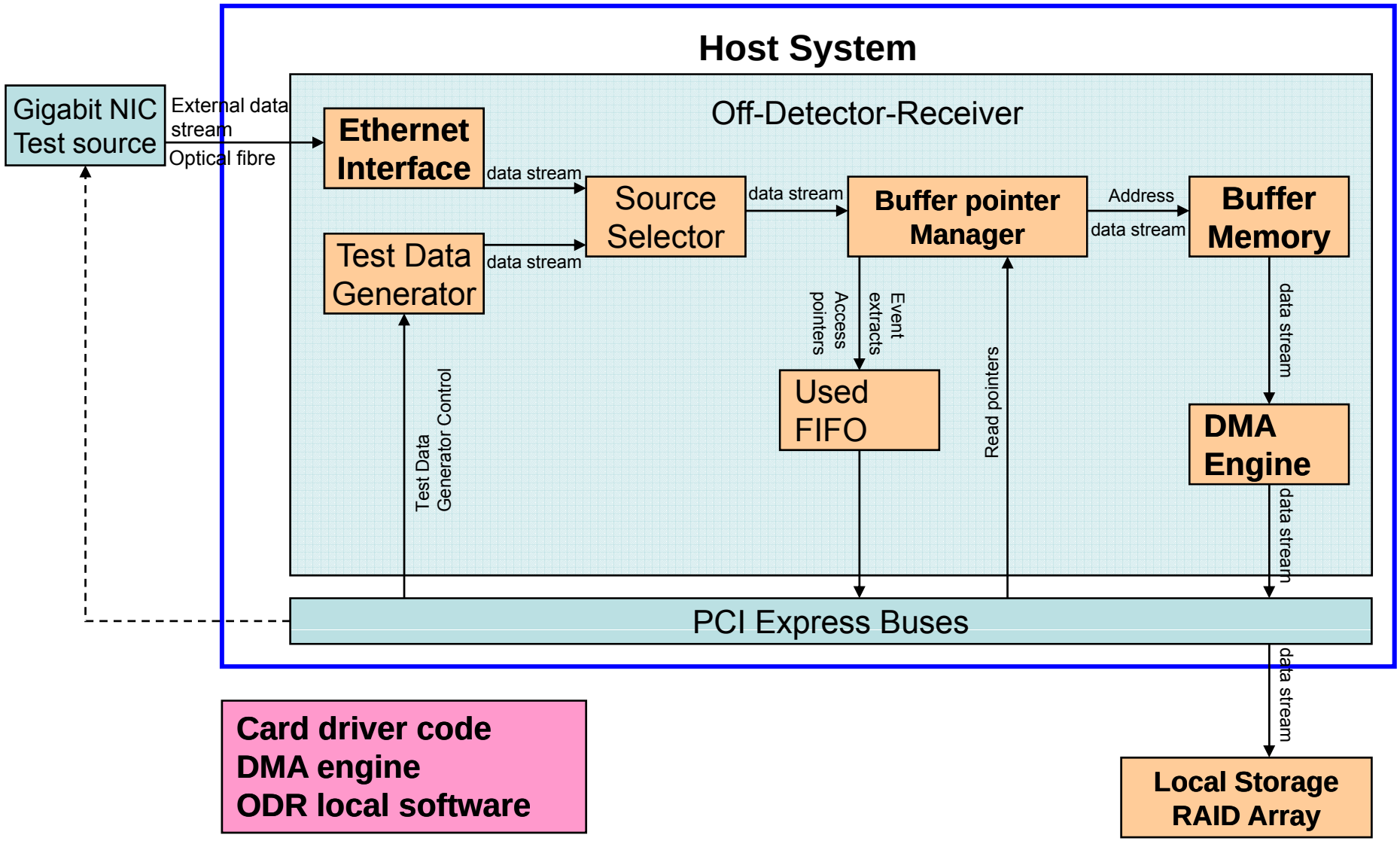
Detector Interface (DIF)

Detector Unit ASICs



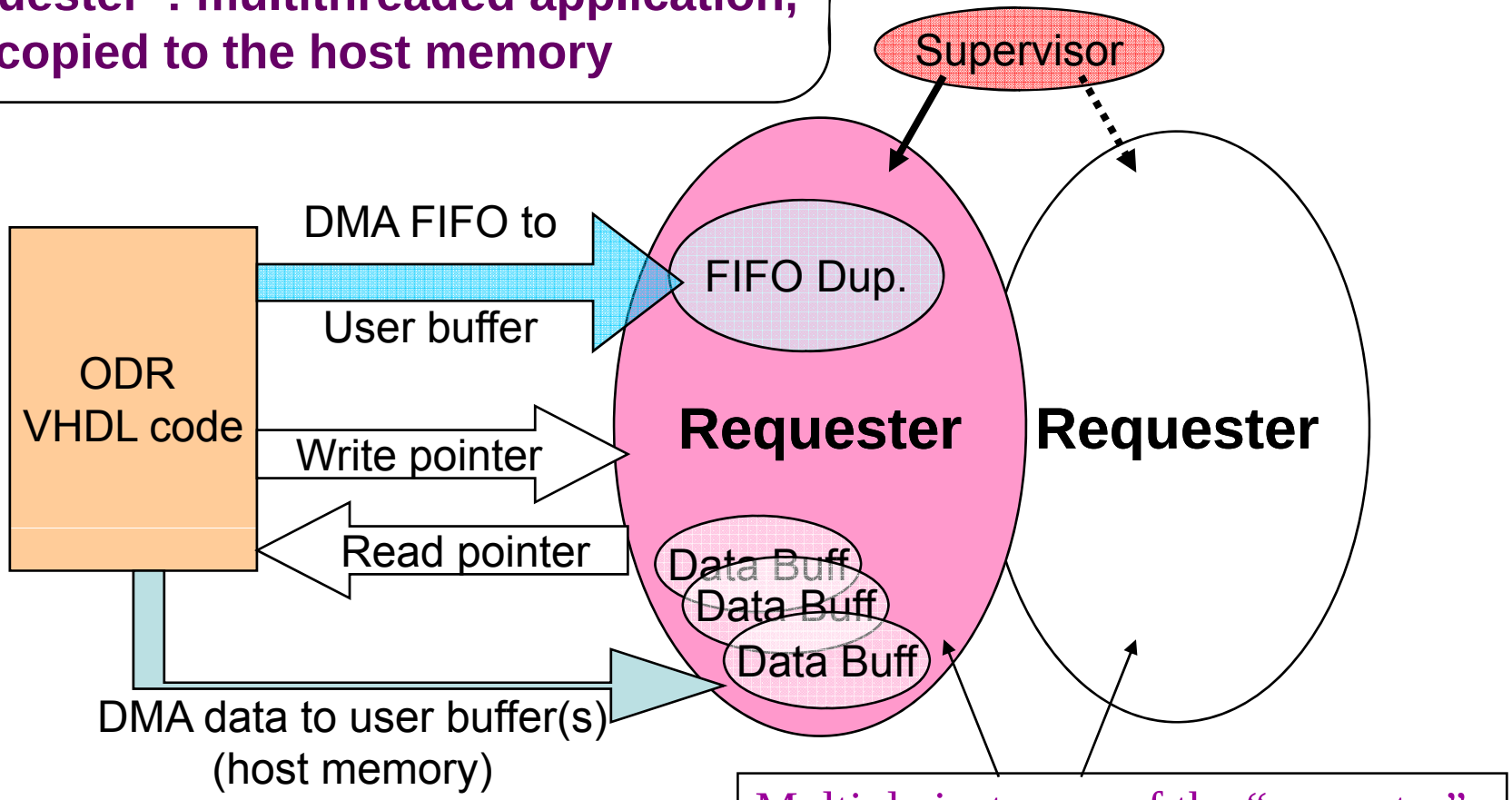
P. Göttlicher, DESY

Current ODR Prototype



Current ODR Prototype

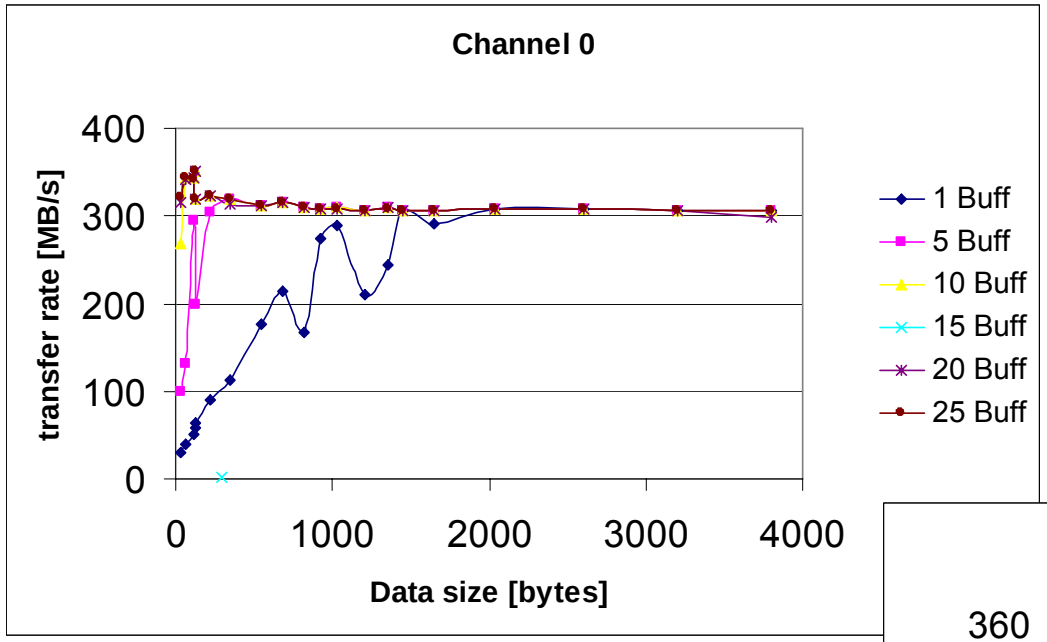
“Requester”: multithreaded application, data copied to the host memory



DMA transfer in maximum 4 k (page size) blocks.

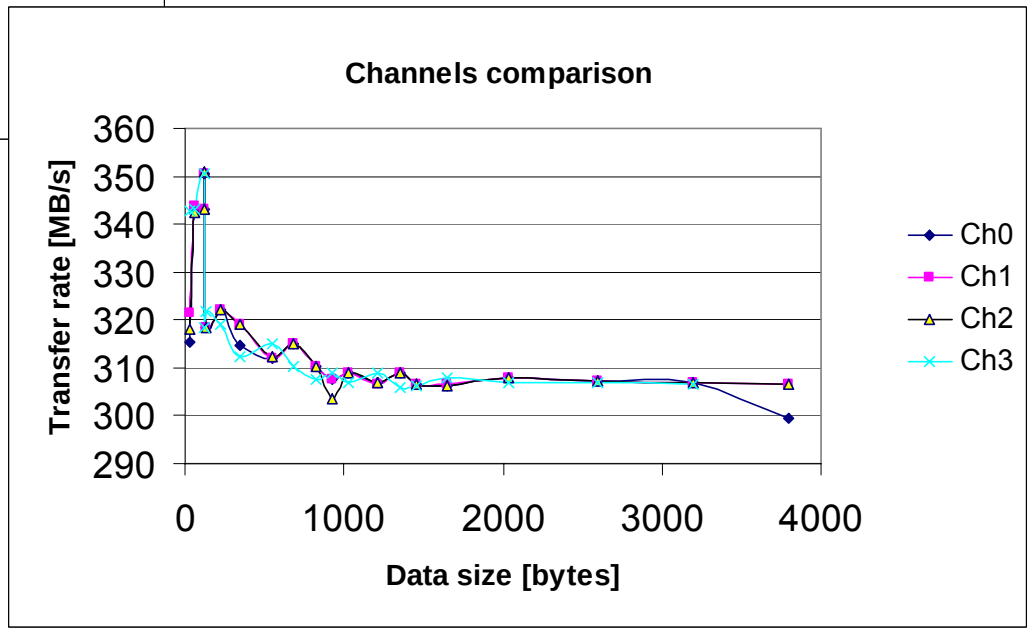
Multiple instances of the “requester” thread. Each accessing different ODR card or different channel.

Performance (Int.Data Gen)

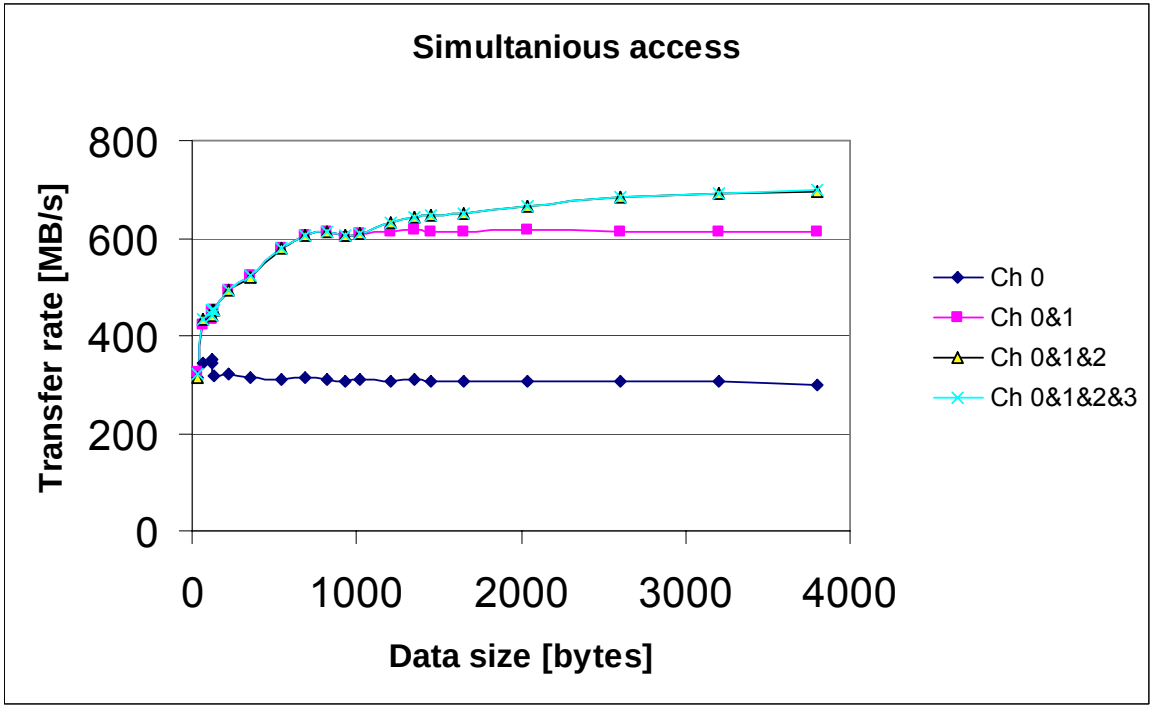


Establishing optimum number of user-defined DMA buffers. No performance improvement above 20 allocate buffers,

Comparison of all channels. Number of data buffers: 20

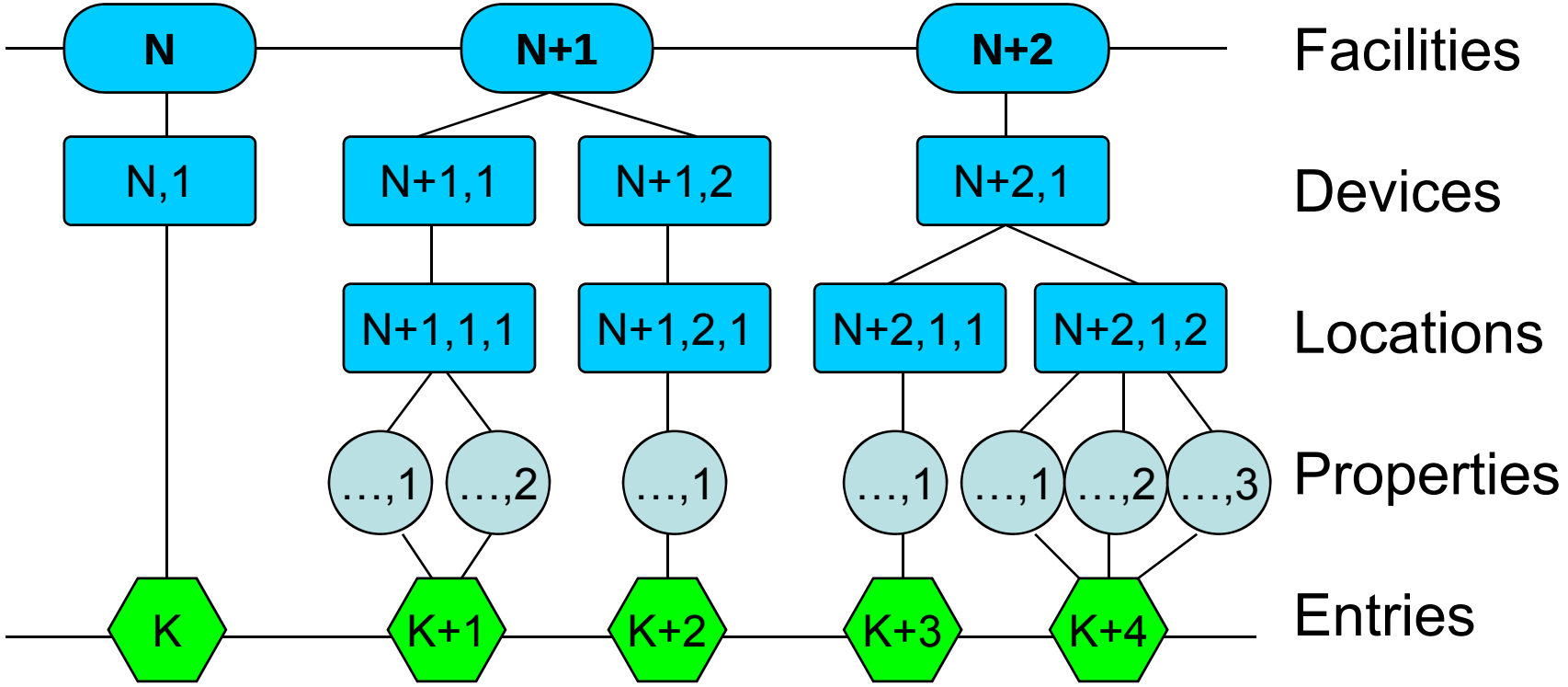


Performance (continuation)



Improvements in performance when accessing more then one channel. The maximum performance achieved for 3-channels access. Adding additional Channel (4-channel access) does not yield improvement in transfer rate.

Equipment Name Server (ENS)



- Select between devices of the same type in different facilities in on-line addressing of the control system.
- Provide the resolution of the names of the devices used in the control system with one entry per device server.
- Define user authentication parameters which are used by the control software to restrict the access to the specified control devices

ENS

- Facility: CALICE.ECAL, CALICE.AHCAL, CALICE.DHCAL
- Device: ODR, LDA, DIF, ASIC1, ASIC2, ASIC3
- Location: ODR1, ODR2, ODRX;
  LDA1, LDA2, LDAX; DIF1, DIF2, DIFX
- Property: X X X ?

ENS can **signal connections** by additional properties, e.g. for device DIF:
CALICE.ECAL/DIF/DIF1/ODR_CON
CALICE.ECAL/DIF/DIF1/LDA_CON
CALICE.ECAL/DIF/DIF1/DEBUG_MODE