Outline of DAQ workpackage

- **Groups: UCL, Imperial,...?**
- **Scope: develop realistic readout for ILC calorimeter. Speed, number of channels, transfer of data, calorimeter design (e.g. Si-W, MAPS).**
- **Hardware and costs:**
  Fibres to transport digitised data from VFE to off-detector receiver (chip-to-chip)?
  FE to off-detector, use fibre but could use dedicated point-to-point or direct connection to network?
  Off detector receiver - PCI card (PCI Express) in standard PC with switches to route to an alive PC?
  £50k prototyping, £100k for larger scale tests.
- **UCL people: (J. Butterworth), M. Lancaster (20%), M. Wing (30%), M. Postranecky, M. Warren, New RA (significant hardware contribution)**
- **Effort: Engineering - M. Warren (30+50+50)% and M. Postranecky (30+30+50)%. 6 $\times$ £25 = £150k. For fabrication of boards (at MSSL?).**
  RA for three years £40k $\times$ 3 = £120k (share with simulation w/p)
- **Travel: Low(?) as mainly within the UK; (same as Paul) £5k per year, £5k for beam test travel, total £20k**

Simulation/case studies needed for proposal

Decide what can/needs to be done and assign names to do this. (NB. not much LC simulation experience at UCL and IC.)

- **Data rates? UCL can look at rate of $\gamma\gamma$ events per bunch crossing.**
- **Data rates? Other processes should be looked at?**
- **Threshold suppression of data; C. Fry has looked at this... IC/UCL/Cambridge?**
- **Something else?**