WP2: DAQ

- **Task 2.1: Readout multiple VFE ASICs (Imperial)**
- **Task 2.2: Understand data transfer on 1.5 m PCB (Cantab)**
- **Task 2.3: Options for network switching (Manchester, UCL)**
- **Task 2.4: Transport of configuration, clock and control data (UCL)**
- **Task 2.5: Prototype off-detector receiver (Cantab, RHUL, UCL)**
- **EUDET: Readout module-0 (mainly Task 2.5)**

Task 2.1

Linked to ASIC production schedule. So no work as yet, but have a schedule along with French collaborators

- **next ASIC version mid-2006 and used in CERN test-beam. Use current DAQ with firmware changes. Power pulsing straight-forward, using their ADC more demanding.**

- **the ASIC after that in mid/end 2007 will require hardware.**

Task 2.2

Preliminary design work of 5 boards stitched together to form a slab.

Possibility of multiple/single readout lines, lines for clock, control and configuration.

Using copper paths still not easy.

Power budget looks okay, but studies to continue.

To feed into module-0 to be built.

Task 2.3

R. Hughes-Jones has previously done extensive studies of throughput for PCI-X standard.

These tests will be re-done using PCI-Express.

Major delay (6months) for delivery of PCI card which has now just arrived. Work to start properly next week.

Task 2.4

M. Warren has started literature survey on SEU - difficult to isolate relevant work for our needs. SEU 1 in 25 years; flash based much more reliable (but expensive); to continue.

Relevance in 5-10 years time? Test a chip now and have a "test setup/procedure" document.

Need to know environment around the FPGA - C. Targett-Adams started to simulate this.

Consider putting FPGAs in test-beam to measure the rate of SEU.

Approach companies for large numbers?

For clock, control and configuration issues, set-up from Task 2.2 can be used.

Task 2.5

Card has to have flexibility for bench tests we want to do, but will also be used for EUDET prototype.

Probably don't need to design and build PCI card - off-the-shelf products look okay. Will assess their capabilities - survey done, buy soon.

Block design (B. Green) of functionality: each represents a self-contained task. Task list and allocation available.

First step: have the capability to read data into host (and out) and measure throughput.

EUDET

Award of EU money means a prototype module will be built: 1 instrumented layer and 1 instrumented tower $\mathcal{O}$ 10^4 channels.

UK providing DAQ which is essentially Task 2.5.

Project started 01/01/06 and runs to 31/12/09. Contracts signed. Money almost there.

UK awarded:

- **Staff: £94,500**
- **Consumables: £59,850**
- **Travel: £7,500 + £9,100 (networking)**

Some division amongst institutes needed.

The Staff is essentially three years of an RA. Institutes doing the work (Cantab, RHUL, UCL) need the extra staff and also need to cover until 31/12/09.

Propose:

- **Extend UCL RA until 31/12/09 - 12 months**
- **Bring forward RHUL RA to 01/10/06 and extend to 31/12/09 - 15 months**
- **Re-instate networking expert from UCL cut by PPARC - 9 months**
- **Cantab? Not working in DAQ.**

EU money would pay for UCL RA and sub-contract some PPARC money to RHUL.