Single Event Upset Studies on the APV25 Front End Readout Chip

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Abstract

The microstrip tracker for the CMS experiment at the LHC will be read out using radiation hard APV chips. During high luminosity running of the LHC the tracker will be exposed to particle fluxes up to 10^7 cm^{-2} s^{-1}, which introduces a concern that the APV25 could occasionally suffer from Single Event Upset (SEU). To evaluate the expected upset rate under these circumstances the APV25 was run under controlled conditions in a heavy ion beam. Upset cross-sections of the digital parts of the chip have been measured at 13 values of incident Linear Energy Transfer (LET). A theoretical prediction of both threshold LET and cross-section is presented along with experimental measurements. These data are used to predict the upset rate for the APV25 in the CMS tracker.

I. Introduction

The high radiation environment of the LHC demands that the electronics in the central regions of the CMS detector must be designed to withstand large doses of ionizing radiation. One result of such high rates is to introduce susceptibility to Single Event Upset (SEU).

The CMS collaboration has adopted a readout system based around the APV chip series[3]. During the research and design phases of the APV chip, much care was taken to ensure a high degree of total dose radiation tolerance. There are three versions of the chip; the APV6, fabricated in the Harris AVLSI-RA Bulk CMOS process[1], the APVD, fabricated in the DMILL process[2] and the APV25, fabricated in a deep sub-micron process[3]. Both the APV6 and APVD have feature sizes of approximately 1.2 microns, with the APV25 much smaller at 0.25 microns. Results of SEU tests on the APV6 have been presented[4]; results of the APV25 tests are in this paper.

With a view to predicting the upset rate in the final CMS Tracking system, a full evaluation of the digital circuits in the APV25 has been performed by exposing the chip to a beam of heavy ions in the SIRAD[9] irradiation facility at the 15-MV Tandem accelerator of the INFN Laboratory of Legnaro, Italy.

A. The APV25

The APV25 front-end chip consists of 128 channels, each of which made up of a pulse amplifier and shaper that feeds a 192 deep analogue pipeline capable of storing input pulses for up to ~4.8 μs. On an external T1 trigger the data are retrieved from the pipeline and then output, via a 128 : 1 multiplexer. The output stream consists of a set of analogue levels retrieved from all 128 channels and a digital header. This header comprises an error flag and an eight-bit address that indicates which one of the 192 pipeline locations had been marked for readout by the trigger pointer. Control of the various chip operation modes and bias settings is achieved via a standard I^2C serial bus link.

The vulnerable parts of the chip are the digital circuits. In the APV these comprise the digital pointers of the pipeline, the FIFO address memory, the I2C control logic and data registers and other main control logic. The upset cross-sections have been measured for the pipeline logic, FIFO, Control logic and the I2C data registers.

II. Theory

A. The SEU Phenomenon in APV25 Circuits

SEU is a non-destructive phenomenon, which affects both dynamic and static memory registers that temporarily store logic states. It manifests itself as a soft error appearing in a device and is caused by a large local deposition of charge, by an ionizing particle, near to a sensitive circuit node[5].

Three types of digital memory element are used within the APV25. They are the D Flip-Flop (DFF), D Flip-Flop with set (DFF-set) and the D Flip-Flop with reset (DFF-reset) and have been designed, using closed geometry transistors, at CERN[6]. Each of these circuits responds differently to deposited charge with characteristic upset thresholds and cross-sections, but the mechanisms by which SEU is manifested are identical in each case. SEUs can be induced in both the master and slave sections of each type of DFF, depending on whether the clock is high or low. Since the bias registers in the APV25, which are made up of simple DFFs, are normally un-clocked, we only need to consider the slave of the DFF in order to predict the behavior of this part of the APV25. Similar investigations have been performed for master and slave in each of the three types of DFF.

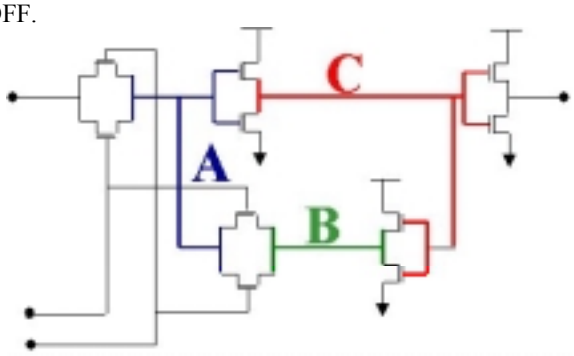

Figure 1 Schematic of slave section of a DFF memory cell

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There are three nodes in which charge collection can give rise to an upset, these are labeled A, B and C in Figure 1. Each node has two critical charges, one for each state transition, 1 to 0 and 0 to 1. For an upset to occur two basic criteria must be met: the incident particle must provide a high enough LET[1] (Linear Energy Transfer) in order to create a charge deposit larger than the critical charge Q_{crit}. The particle must also strike a part of the circuit that is capable of collecting ionized charge while also providing an upset-inducing path for the charge to flow.

The sensitive parts of these nodes are the depletion regions surrounding the highly doped n^+ and p^+ implants, which form the drains and sources of the FETs. The n^+ implants are capable of collecting electrons, therefore charge collected here can only cause an upset if the state of the node, to which the implant belongs, is high. The opposite is true for the p^+ implants. In total there are 5 sensitive n and 5 sensitive p implants, which are shared by the three nodes in the following way: nodes A and B contain 2 of each, and node C contains one of each. The surface area of each of these implants is known precisely, enabling an estimate of the normal incidence upset cross-section to be made by summing these areas in the correct way. Table 1 shows these cross-sections, along with the simulated critical charge, for each mode of upset, and the implant type in which the charge must be collected.

SPICE simulations have been performed for all upset modes in the three types of DFF, establishing the critical charges. EVEREST[7] simulations have been performed in order to investigate the charge collection efficiency of both the n and p implants, and have shown that the p implants have ~50% the efficiency of the n implants. This work has also provided a realistic charge pulse shape, which was comparable to the simple piecewise linear current pulse used in the SPICE simulations (50ps rise and 100ps fall). Ongoing work will include more Spice simulations with a more realistic pulse shape, but this should not affect the predicted critical charges to a large degree. A full description of this work will be published at a later date.

Table 1: Sensitive areas and critical charge for six modes in a DFF

	Upsets from 0-1			Upsets from 1-0		
	Q_{crit} [fC]	n or p	σ [μm^2]	Q_{crit} [fC]	n or p	σ [μm^2]
Hit on A	442	p	9.94	206	n	7.7
Hit on B	638	p	4.73	319	n	1.3
Hit on C	274	n	0.65	592	p	2.77
Total	-		15.32	-		11.77

Clearly, the lower charge collection efficiency increases the critical charge for the 'p-modes'. If one converts the critical charges into equivalent LET values for ions in silicon, it is possible to predict the shape of the heavy ion upset cross-section curves.

[1] LET is a measure of a particle's rate of energy transfer in a particular material and is given by $LET = \frac{dE}{dx}.\frac{1}{\rho}$, where ρ is the density of that material. All values of LET in this paper refer to energy transfer in silicon.

B. Total Sensitive Area of APV25

By summing the sensitive areas in each of the DFFs, one can make a rough estimate of the saturated upset cross-section. Table 2 shows the total number of DFFs and an estimation of the sensitive area, using an average of 14μm^2 for each bit.

Table 2: Sensitive bits in APV25 and their cross-sections

	Pipeline logic	FIFO	I2C Registers	Control logic
No. of Flip-flops	768	40	109	167
Sensitive Area (cm^2)	1.1 e-4	5.6e-6	1.5e-5	2.3e-5

The main contributor to the sensitive area is the pipeline logic.

C. Threshold LET

Using 3.6 eV per electron-hole pair, the critical energy required is given by:

$$E_{crit} = \frac{Q_{crit}}{e} \times 3.6 \qquad [1]$$

We can convert this value into a measure of LET using equation 2. The depth z is a variable and represents the sensitive depth of the implants; this is the sum of the depletion region depth and the ion impact resultant funnel length. This value can be determined by fitting a theoretical curve to the data and extracting the threshold LET. LET_{th} is the minimum LET for which upsets of a particular mode can occur.

$$LET_{th} = \frac{E_{crit}}{z\rho} \qquad [2]$$

D. Upset Cross-section

The cross-section, σ, for SEU's is defined at normal incidence as in equation 3.

$$\sigma = \frac{N_{events}}{\Phi}\left[cm^2\right] \qquad [3]$$

Where Φ is the total incident particle fluence, and N_{events} is the number of events (SEUs) counted during the test. If one ignores the existence of modes with different upset thresholds, it is reasonable to expect that a typical cross-section curve would look like a Heavyside function, with a value of 0 for LETs below the threshold and then a constant for all values after that, assuming that we ignore any possible increase in σ due to charge collection around the edge of the sensitive volume as the deposited charge density becomes larger. However, experimental evidence to date shows that σ increases up to a plateau more slowly than would be expected. Various explanations have been offered as to the reason for this, but the overwhelming evidence from the work carried out in this test suggests that the main reason for the slow increase is in fact 'switching on' of different modes of upset at different LET thresholds. Previous studies have measured σ of a single device, and some have even separated the results into upsets from 1 to 0 and those from 0 to 1. However, it has not been

possible to distinguish, any further, the exact mode that caused the upset, since each mode has the same resultant digital effect.

By ignoring the existence of modes, it was assumed that there was just one characteristic critical charge. Previous measurements of σ have been fitted with a smooth curve such as the Weibull function[5], which gives the impression that σ rises slowly as the incident LET increases. From Table 1 it is clear that there should be six distinct modes of upset each with a different threshold LET. If we now go back to the initial assumption of a more abrupt step-like function for each mode, and take the threshold values directly from Table 1, using equation 2 with a sensitive depth of 1μm, a sensible estimate[5], one can create the theoretical cross-section curves for upsets from both 0 to 1 and 1 to 0, by summing σ for each mode.

It is easy to see from Figure 2 that any steps in the experimental curves, could quite easily be lost due to statistical errors, and reproducing a curve like this, in practice, would require a very thorough scan of incident LET, which is not a trivial thing to achieve in an small amount of time. However, Figure 2 shows a more distinctive step, which may provide us with a better chance to see the structure experimentally.

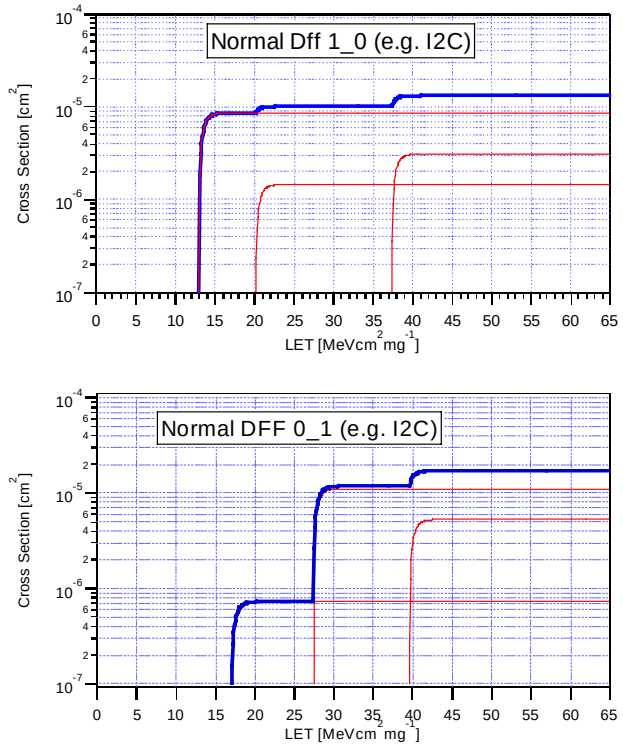


Figure 2: Theoretical cross-sections for simple DFF

Previously, by fitting the experimental data with a single Weibull curve, it has been possible to use the fitted curve to interpolate predictions of the upset rate for other forms of radiation. In the case of the CMS tracker, the required calculations are complicated since the incident particles are typically of single charge and therefore only cause large enough ionization by virtue of interactions with silicon lattice sites. Monte-Carlo simulations are required and have been developed at CERN[8]. If the experimental data exhibits the predicted behavior, it would improve the accuracy of such calculations. Using the same method one can predict σ of the DFF-set, which is used in the pipeline.

In this case, both the slave and the master sections of the circuit have been included, assuming that each is sensitive for half of the total time, thus halving σ. The first three steps are all n-modes with the initial mode at ~3x10^{-5} cm^2. The fourth step is the first p-mode, which increases σ to ~ 7x10^{-5} cm^2 an increase of 4x10^{-5} cm^2.

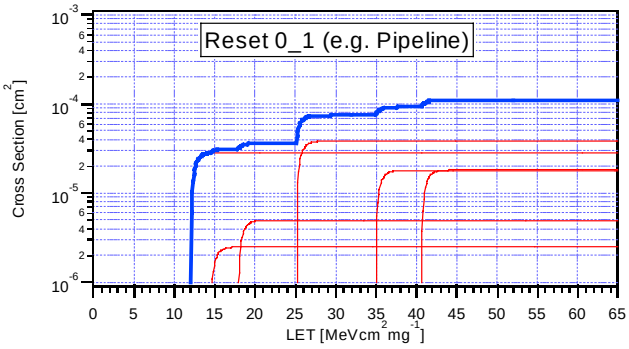


Figure 3: Theoretical cross-section for pipeline logic

III. TESTING THE APV25

A. Hardware

The test beam setup was effectively identical to the APV readout chain in the lab. Control was performed by a PC running LabVIEW, which communicated with the VME crate via a PCI VME interface. The trigger sequence for the APV was provided by a SEQSI sequencer, and control of the APV performed by a VI2C slow control interface. The output from the APV was digitized by a flash ADC.

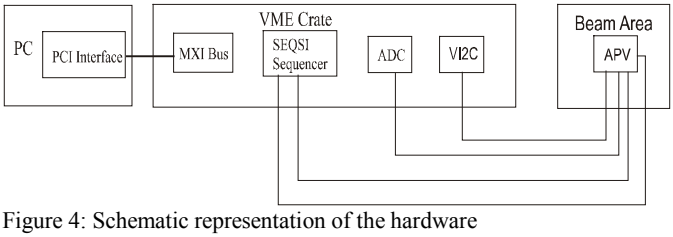


Figure 4: Schematic representation of the hardware

B. Software

The control and data acquisition was carried out by custom designed software developed in LabVIEW. The main tasks were to provide resets and triggers, via the SEQSI, to capture the digitized APV output data frame, via the ADC, to perform rudimentary on-line analysis and to save data to disk. The on-line counting of events was necessary for fine-tuning of the sensitive time in order to ensure that event counting was non-

saturated (see section 3.5). Other on-line information included an overall count of upsets and a total sensitive elapsed time counter. The software also included I2C control for testing the APV static registers.

C. Masking APV Sections

One of the requirements of the system was the ability to mask off sections of the APV. The masks were precision engineered to expose specific predetermined areas of the chip. With four chips in the beam at the same time, it was possible to have four different masks, which enabled selection without the necessity to break the vacuum. Figure 5 shows the location of the four digital parts of the APV25, which were isolated by the masks.

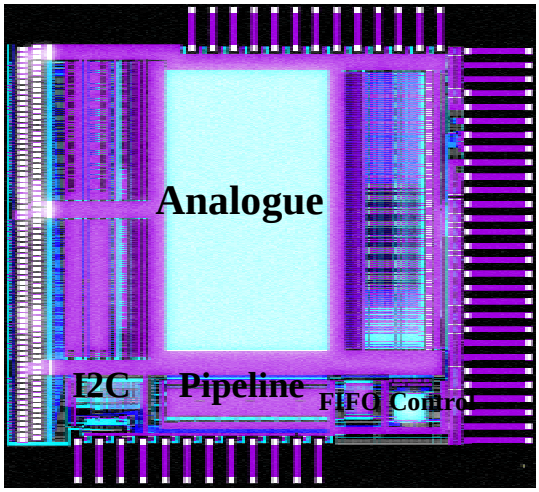


Figure 5: Location of tested circuits.

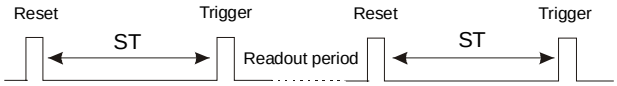
D. Seeing Upsets

In the event of an upset in the pipeline logic or FIFO, there are two possible outcomes: either the error bit in the output data frame is set, or the pipeline address in the output data frame is corrupt. The error bit is set if an upset in the pointer logic causes the latency of the trigger pointer to change. Only a small proportion of upsets produce both outcomes simultaneously.

One can also test for events in the I2C registers by writing defined values, reading out the values after a set period of time, and comparing them with initial values. In this case it is possible to detect the individual cells, which have been upset. Upsets in the control logic block can have a more drastic effect, These errors will be picked up by incorrect pipeline addresses, loss of digital header, or loss of entire data frame. When measuring upsets in the pipeline and FIFO, one only needs to reset the chip using a soft 101 reset[3]. However, when measuring upsets in the control logic one requires a hard power-on reset, since upsets in the control logic can cause the chip to lock up and subsequent data frames all exhibit errors, caused by the original upset, thus making it impossible to distinguish further upsets.

A power-on reset recovers the operation of the control logic. Following this one must apply a soft reset and then readout. It is important that the average number of upsets per time interval is less than one (see section III-E). The running time per measurement, when the chip is sensitive to upsets, is defined as the sensitive time (ST). When measuring the upset rate, following each ST there is a readout period, this is repeated many times to measure a reasonable number of upsets. For the pipeline, FIFO and control logic a typical run consists of 100,000 STs, and for the I2C, 100. In the case of the I2C test, instead of a reset and trigger, one writes a simple pattern followed by the ST and then a read. The pattern can be varied to establish the cross-section for both 1 to 0 and 0 to 1.

Figure 6 shows the definition of ST and $T_{sensitive}$ the total sensitive time for one run.



$$T_{sensitive} = N_{triggers} \cdot ST$$

Figure 6: Definition of ST for the pipeline logic FIFO and control logic

E. Non-saturated Measurements of Upsets

One important issue is undercounting of events in the pipeline, FIFO and control logic. Only one error can be detected within each sensitive time interval, as more than one error would still only produce symptoms consistent with one error. If we lose events by undercounting then the measured upset rates begin to saturate, hence one must ensure that the number of events is less than half the number of sensitive time intervals. In order to achieve this condition one can adjust the length of the sensitive time interval.

F. Irradiation at the TANDEM Accelerator

Thirteen values of LET were provided, by a range of ions at various energies. The irradiation was performed at room temperature under a vacuum of 10^{-6} mbar. The typical beam flux was in the range 10^{4}–>10^{5} cm^{-2} s^{-1}. For each ion this value was set to a constant.

IV. RESULTS AND CONCLUSIONS

Measurements were made for the SEU cross-section of the pipeline, FIFO, control and I2C logic. The results in Figure 7 show the cross-sections for the I2C logic. As expected, it is difficult to see any structure in the curve for upsets from 1 to 0. However the overall shape is similar to expectations. The clear steps that are visible in the second curve display a very close likeness to the predicted curve.

Figure 8 shows the results for the pipeline logic. The statistics gathered for this circuit were much better, because of the large cross-section, and even though the steps in the curve are quite small, it is possible to fit the experimental data to the theory.

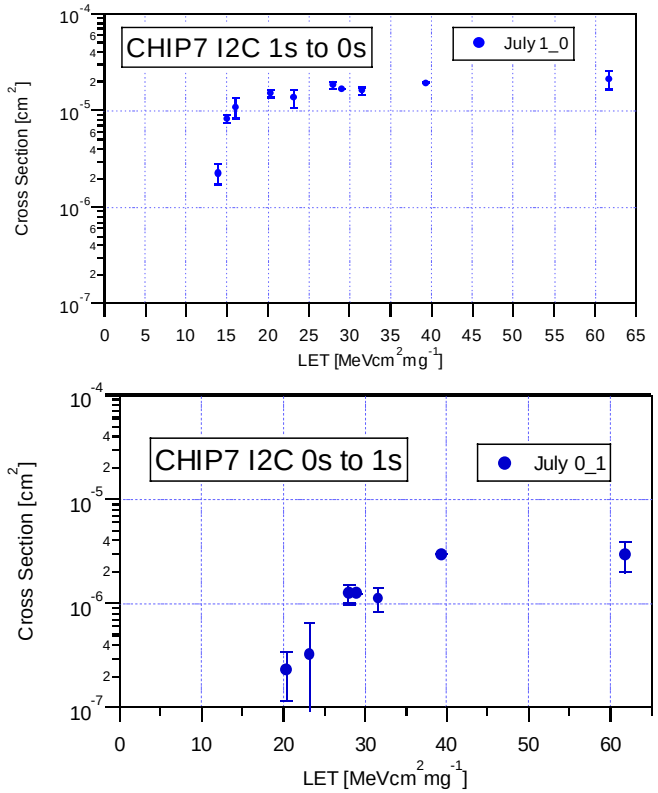


Figure 7: Measured cross-sections for I2C logic

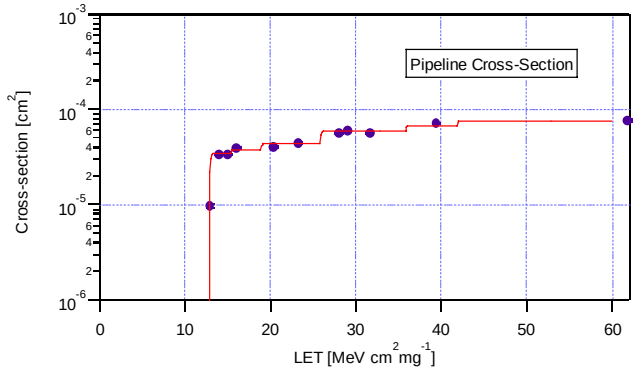


Figure 8: Cross-section with fitted curve

This fit is performed by varying four parameters: LET_{th} and σ_{sat} for both n and p modes. The thresholds were extremely close to those predicted. However σ for the p modes was slightly lower than expected. The first p-mode increases σ to $5.5x10^{-5}$ cm^2, an increase of $2x10^{-5}$ cm^2, less than the expected $4x10^{-5}$ cm^2. Similar curves were measured for the FIFO and control logic, all the extracted values of σ_{sat} are shown in Table 3 along with the geometrical predictions.

Table 3: Comparison of predicted and measured cross-sections

σ_{sat} [cm^2]	Pipeline	FIFO	I2C (1-0)	I2C (0-1)	control
Predicted	$1.5x10^{-4}$	$8x10^{-6}$	$1.3x10^{-5}$	$1.7x10^{-5}$	$2.3x10^{-5}$
Measured	$9x10^{-5}$	$2.5x10^{-6}$	$2x10^{-5}$	$3x10^{-6}$	$8x10^{-6}$

A. Effect on CMS

Table 4 gives a breakdown of the predicted upset rates in the CMS tracker. These figures have been calculated using the method described in [8], and summing the effect of the four circuits to produce a prediction of the behavior of the whole chip. These upset rates are very low and should pose no threat to the operation of the tracker.

Table 4: Upset rates in the CMS tracker

Tacker region	No. APVs	No. SEU/Layer/s	Time per SEU	No. SEU/hour	Fraction chips/hour
IB	14400	$1.46x10^{-2}$	68.6	5246	0.36%
OB	29232	$4.1x10^{-3}$	243.7	1477	0.05%
IE	4416	$5.15x10^{-3}$	194.2	1854	0.42%
FE	30208	$8.58x10^{-3}$	116.5	3090	0.10%
Total	78256	$3.24x10^{-2}$	30.9	116.67	0.15%

V. ACKNOWLEDGEMENTS

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