APV25 Production Testing and Quality Assurance

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Abstract

The APV25 is the 128 channel chip for silicon tracker readout in CMS. The production phase is now underway, and sufficient wafers have been produced to allow significant conclusions to be reached on yield and performance based on data acquired during the wafer probing phase. The wafer probe tests are described and results used to make comparisons between chips, wafers and wafer lots.

Chips sampled from wafers after dicing are mounted in a custom setup enabling more detailed quality assurance measurements, and some of these are also irradiated to confirm radiation hardness. Details of measurements and results are presented.

I. INTRODUCTION

The APV25 is the 128 channel CMOS chip for the CMS silicon micro-strip tracker readout, fabricated on 8 inch wafers in 0.25 μm technology. A more detailed description of the chip can be found in [1] and a user manual is available [2]. The main features are:

1) Low noise CR-RC amplifier with 50 ns time constant.

2) 192 cell pipeline allowing a level 1 latency of up to 4 μs plus buffering for events awaiting readout.

3) Peak or deconvolution operating modes: In peak mode only 1 sample/channel is read from the pipeline (timed to be at the peak of the analogue pulse shape). In deconvolution mode three samples are sequentially read and the output is a weighted sum of all three, resulting in an effective short pulse shape to achieve single bunch crossing timing resolution.

4) The 128 analogue samples are multiplexed onto a single differential current output line.

5) Operational modes of the chip are programmed using an I^2C interface, which is also used to set up operating points of the analogue stages via on-chip digital to analogue converters.

Testability of the APV25 is enhanced by the programmable nature of the chip, with read/write access to all registers defining operational modes and bias settings. The on-chip calibration pulse generator and the digital header preceding the analogue samples in the output data stream are particularly useful test features. The calibration pulse generator allows charge injection to all 128 channels in groups of 16, with programmable amplitude and delay, allowing analogue pulse shapes to be measured and tuned. The APV25 output frame digital header contains the pipeline column address from which the analogue samples were taken. Agreement between the actual value and the value expected is a strong check on synchronization and correct operation of the pipeline control logic.

A total of ~100,000 chips are required for CMS (including spares). A high yield of multi-chip hybrids requires comprehensive testing of chips on the wafer. Time limits restrict the amount of testing possible during wafer probing, so more detailed quality assurance (QA) tests (including measurements after irradiation) are carried out on chips sampled from the production wafers. This paper describes the wafer probe and QA tests and results.

II. WAFER PROBE TESTING

The wafer test hardware consists of a Micro-manipulator 8 inch semi-automatic probe station controlled (via RS232) by a PC running LabVIEW. A VME based control and DAQ system instruments the APV25-PC interface. The probe card (figure 1) is designed in-house to allow buffering, termination and decoupling as close as possible to the probe needles.
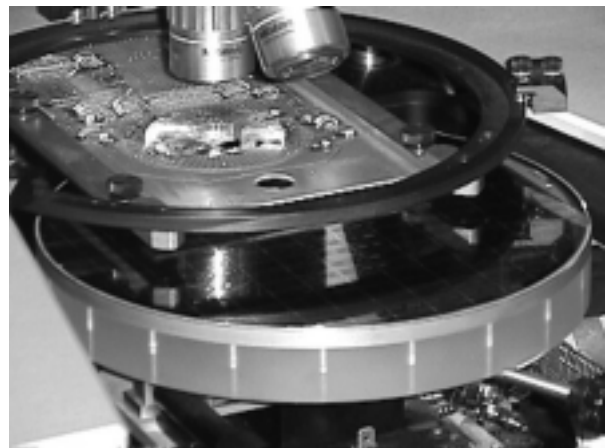

Figure 1. Probe card with APV25 wafer underneath.

The wafer test software is LabVIEW based and is designed to cover potential failure modes as exhaustively as possible within the permissible test duration. A more detailed description of the test procedures can be found in [1]. The front panel of the LabVIEW virtual instrument (VI) executed for each APV25 site is shown in figure 2. Comprehensive tests of digital functionality are included as well as analogue measurements of pulse shape, gain, pedestals, noise, pipeline integrity and power consumption.
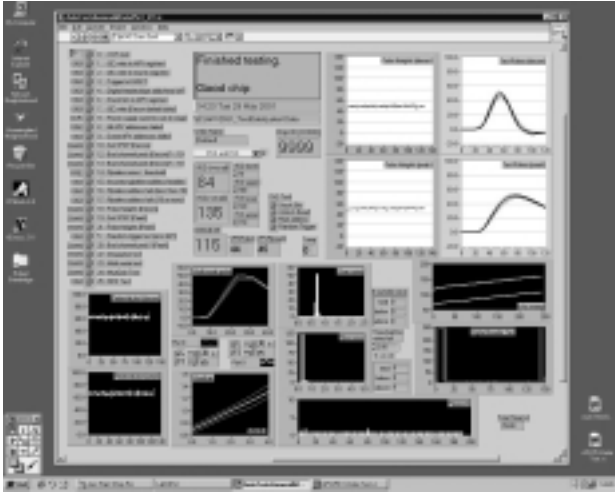
Figure 2. Front panel of the APV25 wafer test LabView VI.

The VI shown in figure 2 is called by a supervisory VI which controls the site-to-site probe station movement, the generation of the pass/fail wafer map and the storage of the individually identified chip test data file. The time required to test one wafer APV25 site and move on to the next is ~70 seconds. There are 360 viable APV25 sites/wafer, allowing a throughput of 2 wafers/day which is sufficient to keep pace with module production.

III.   WAFER PROBE TEST RESULTS

The numbers of wafers delivered and tested so far are listed in table 1. Lot 0 was the engineering run delivered in September 2000. Lots 1 to 5 are production lots delivered since January 2002. A production problem was identified with lots 1 and 2 (see section IV) and all these wafers were replaced by lots 4 and 5. Not all wafers from lots 1 and 2 were probed, but the results for good chips are still included here. Not all the wafers from lots 4 and 5 had been probed at the time the analysis of results was carried out. Consequently the results here are from a total of 88 wafers from which 13,225 chips passed all tests, a substantial sample of the final production volume.

Table 1:   Wafers delivered and tested.

Lot #	Type	Delivered	Tested	Average yield [%]
0	engineering	10	10	82
1	production	24	13	27
2	production	21	12	10
3	production	25	25	79
4	production	25	13	33
5	production	20	16	47

A. Supply Currents

Figure 3 shows histograms of the supply currents for all chips which were passed by the wafer probe procedure. VDD and VSS are the currents in the +1.25 and –1.25 Volt

rails respectively. All production lot testing (lots 1 to 5) was performed with a fixed set of values programmed into the on-chip bias generator registers. The wider spreads for the distributions for lot 0 are due to ongoing hardware/software developments during the test phase for these wafers. Figure 3 illustrates a relatively small spread of supply current values within lots, with systematic, but still small, lot to lot variations.
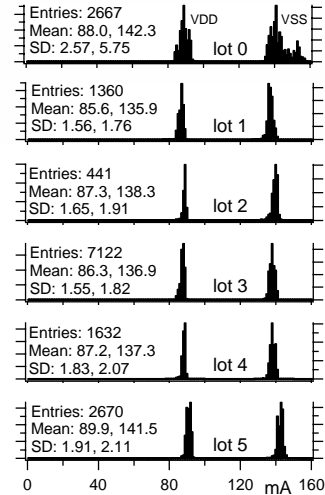

Figure 3. Power supply currents for all pass chips from all lots.

B. Gain

Figure 4 shows histograms of the gains (average peak mode calibration pulse heights) measured for all pass chips. Once again a wider spread can be seen for lot 0 for the reason previously explained. The gain matching between lots is quite good, but the results here are probably not representative of the true gain matching as the calibration pulse amplitude is not well controlled due to the poor tolerance of the charge injection capacitance implemented by parasitic capacitance between two metal layers.
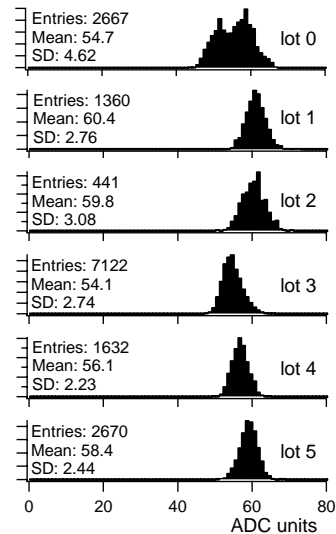

Figure 4. Average Peak mode calibration pulse gains for all pass chips from all lots.

C. Noise

Figure 5 shows histograms of the average bare channel noise in deconvolution mode measured for all pass chips. Low noise has been found to be difficult to measure accurately in the probe test environment due to electrical interference and non-ideal decoupling on the probe card. A rough calibration can be applied using the assumption that the APV25 digital header amplitude corresponds to 8 mips (1 mip = 25,000 electrons). The results in figure 5 show values in the range 500 – 600 rms electrons, which are close to the expectation value of ~ 430 electrons from individual chip measurements.
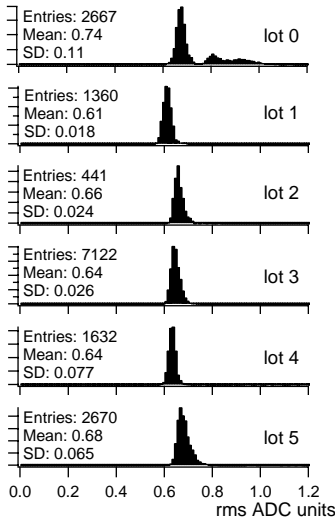

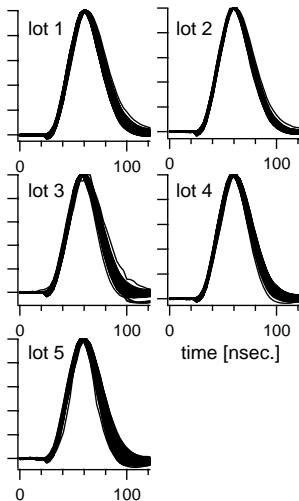Figure 5. Average bare channel deconvolution mode noise for all pass chips from all lots.

Figure 6. Average deconvolution mode pulse shapes for all pass chips from the production lots.

D. Pulse shapes

Figure 6 shows the average pulse shape in deconvolution mode for all pass chips from all 5 production runs, normalised to the maximum pulse height. Good pulse shape matching is evident with little wafer or lot dependence.

Since all chips have been programmed with the same bias parameters it is clear that it is possible to provide a single set of parameters for subsequent multi-chip hybrid and module tests that will enable satisfactory performance to be achieved, and fine tuning of the pulse shape need only be performed if it is necessary to achieve the best possible performance.

IV.   YIELD

The yields of all the wafer lots tested so far are included in table 1. Unfortunately the high yield achieved for the engineering run wafers (lot 0) has not been maintained consistently throughout the production lots. Figure 7 shows a wafer map for one of the wafers from production lot 1, where good chips are shown white, and chips which have failed any test are shown grey. There are some good chips around the periphery and also a central patch of good chips, but this wafer has an overall yield of only 23%, and the average yield of lot 1 is 27%. Production lot 2 showed a lower average yield, with a similar circular pattern to the wafer map.
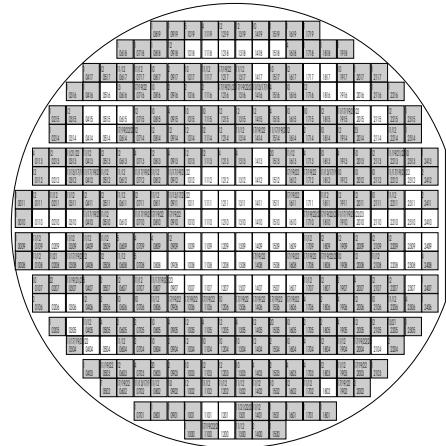

Figure 7. Wafer map example from lot 1.

To improve the processing yield for APV chips it is necessary to understand the cause of the variable yields observed. A significant effort has been devoted to this, led by the CERN microelectronics group with substantial support from the manufacturers. Early investigations did identify some defects in the silicide layer for lots 1 and 2 and the wafers in these lots were replaced by lots 4 and 5. These lots were monitored for silicide defects during processing and no problems were observed, but the yields for these lots are still low, and it now seems likely that the silicide explanation does not account for all the failures in lots 1 and 2. The picture is not consistent, however, in that lot 3 shows a good average yield, although some wafers do have a small patch of failing chips in the centre.

The exact cause of the variable yield is still not clear. There is evidence that other HEP designs have experienced similar effects (although with smaller statistics) and it is possible that there are common features in the metal layers that differ from those in the higher volume production in

the process. One example is long metal tracking which gives enhanced sensitivity to ESD effects during production, although the design rules are not violated. To investigate the problem further some re-probing of low yield wafers will be undertaken, with additions to the software designed to associate failures with the physical location of the failing circuit in the chip, looking for correlations with specific layout features (e.g. long metal tracks). The CERN microelectronics group are also submitting a test structure specifically designed to test the metal layer low-yield theories.

V. QUALITY ASSURANCE

The objective of the QA testing is to perform more detailed tests on chips sampled from the production wafers. The amount of testing that can be performed during wafer probe is limited by the throughput requirement, and the accuracy is limited since injection of a known calibration charge into any of the chip inputs is not possible. Noise measurements are also difficult during wafer probe because of electrical interference, and it is only possible to measure the noise for unbonded channels, without additional external added capacitance. It is also impossible to perform radiation hardness QA measurements.

The APV25 production QA plans are to perform more detailed electrical tests on a chip sampled from every wafer, to irradiate a subset of these to 10 Mrads, followed by repeat measurements before and after annealing for 1 week at 100 ^{o}C. The sample size for radiation test is eventually expected to reach ~ 20%, i.e. chips from ~ 5 wafers/lot, but the coverage will initially be higher until confidence is established.

In the QA test setup the APV25 is mounted on a small daughter card (~ 25 mm x 25 mm), which plugs into a motherboard which interfaces control signals, power and outputs. Some of the APV25 inputs are bonded to allow external charge injection and additional capacitive loads.

The fully automated test procedure includes pulse shape tuning to achieve a best fit to an ideal 50ns CR-RC pulse shape, followed by the following measurements:

1) Power consumption.
2) Pulse shape, gain and linearity for calibrated external signal.
3) Noise measurements for bare channels and those with added capacitance.
4) Internal calibration response.

These tests are repeated after irradiation and again after annealing. Identical X-ray irradiation facilities are available at Padova University and Imperial College. The chips are irradiated with X-rays with an energy spectrum which peaks at 10 keV. Dosimetry is performed using silicon diodes with an estimated accuracy of ~ 10%. The dosimetry has been cross-checked between Padova and Imperial College with a relative accuracy of better than 1%. The chip is positioned in the radiation field such that the dose is

uniform to within 10% across the chip. Irradiation to 10 Mrads(SiO$_2$) takes ~15 hours. The chip is biased, clocked and randomly triggered during both irradiation and annealing phases.

The QA results to be presented are based on measurements on chips from each of the 10 engineering wafers, and on chips from 13 of the wafers from production lot 3. The remaining wafers have yet to be diced. If the wafer showed any low yield patches the QA chip was sampled from the centre or adjacent to any such patch. All 23 chips have been irradiated, and 7 now annealed (4 from the engineering lot, 3 from lot 3).
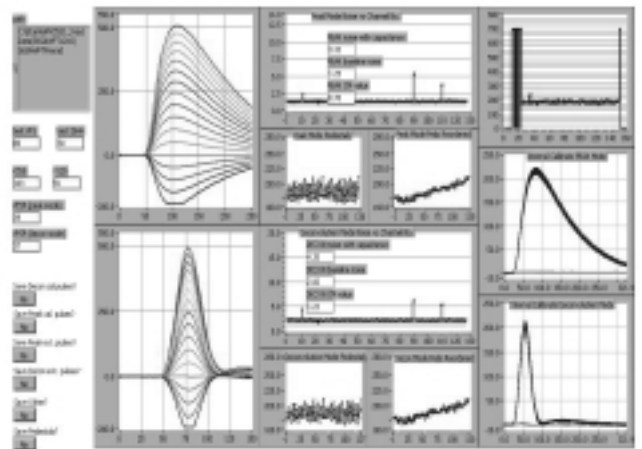

Figure 8. Front panel of the Quality Assurance Labview VI.

Figure 8 shows the front panel of the LabView VI which performs the QA procedure. The pulse shapes in peak and deconvolution modes can be seen both with external charge injection and the on-chip calibration circuit. Other panels show noise and pedestal measurements, and the APV25 output frame.
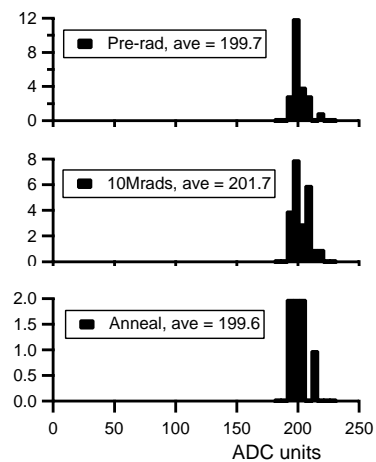

Figure 9. QA gain measurements.

Figure 9 shows the gain measured with the externally injected charge, pre-radiation, after 10 Mrads and after

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annealing (for the 7 chips which have been annealed so far). No significant changes in gain are observed.

Figure 10 shows the average noise for the unbonded channels and for the channels with added capacitance. There is no significant difference after irradiation or anneal, implying that neither the noise slope (with added capacitance) nor the intercept is affected.
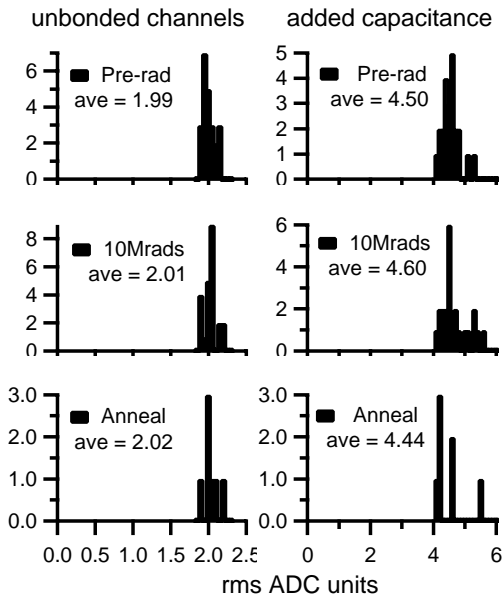

Figure 10. QA noise measurements.

Finally figure 11 shows a typical linearity plot in peak and deconvolution mode for the signals acquired using the external charge injection, where no significant effects can be observed. Signals are injected in 0.5 mip steps from –2 to 6 mips as can be seen in figure 8.

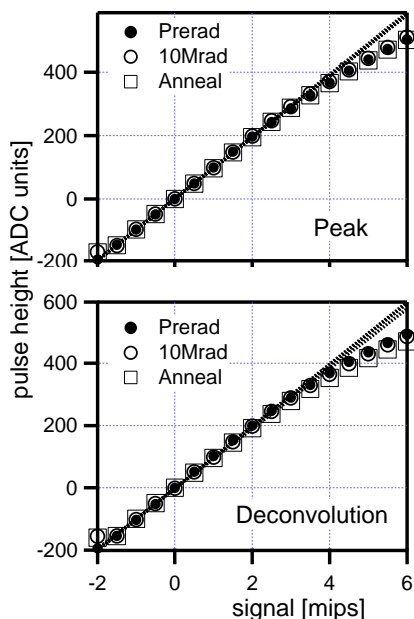

Figure 11. QA linearity measurements.

VI.   CONCLUSIONS

A production wafer probe test system for the APV25 CMS micro-strip tracker readout chip has been developed and is working well with a throughput of 2 wafers/day. Approximately 100 wafers have been tested so far and data from the analysis of 13,000 chips which pass the wafer tests have been presented here. The test data analysis of performance parameters such as power consumption, gain, noise and pulse shape shows good matching between chips, wafers and lots.

The yield of good chips/wafer has been variable during the production phase. The cause of this is still unclear and work is in progress to improve understanding.

An automated setup and protocol for quality assurance of the APV25 wafers has been developed, where detailed characterisation measurements are made on chips sampled from the production wafers before and after 10 Mrads and again after an annealing step. Results from all chips tested so far show good quality and no significant radiation effects, as expected.

VII.   ACKNOWLEDGEMENTS

VIII.   REFERENCES

[1] The CMS Tracker APV25 0.25 μm CMOS Readout Chip, M.Raymond et al, Proceedings of the 6th workshop on electronics for LHC experiments, CERN/LHCC/2000-041, 130-134.

[2] APV25s1 user manual, http://www.te.rl.ac.uk/med/