Single Event Upset Studies on the CMS Tracker APV25 Readout Chip

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Abstract

The microstrip tracker for the CMS experiment at the CERN Large Hadron Collider will be read out using APV25 chips. During high luminosity running the tracker will be exposed to particle fluxes up to 10^7 cm^{-2} s^{-1}, which raises concerns that the APV25 could occasionally suffer Single Event Upsets (SEUs). The effect of SEU on the APV25 has been studied to investigate implications for CMS detector operation and from the viewpoint of detailed circuit operation, to improve understanding of its origin and what factors affect its magnitude. Simulations were performed to reconstruct the effects created by highly ionising particles striking sensitive parts of the circuits, along with consideration of the underlying mechanisms of charge deposition, collection and the consequences. A model to predict the behaviour of the memory circuits in the APV25 has been developed and data collected from dedicated experiments using both heavy ions and hadrons have been shown to support it.

Keywords: SEU; Single Event Upset; CMS Silicon Tracker; APV25; Radiation Tolerance; Front-end electronics.

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1. Introduction

The Compact Muon Solenoid (CMS) [1] experiment is a general purpose detector designed for the Large Hadron Collider (LHC), which is a new CERN accelerator now under construction. LHC should begin operation in 2006 with collisions between counter-rotating beams of protons with a maximum combined energy of 14 TeV. Experimentation at the LHC presents unprecedented challenges. The intense proton beams intersect at 25 ns intervals, with multiple collisions per crossing. As a consequence of high particle fluxes, radiation damage to detectors and electronics could lead to degradation of performance, particularly in the regions close to the beam.

The interior region of CMS contains concentric layers of silicon microstrip detectors designed to measure trajectories of charged particles which emerge from proton collisions and follow helical paths in the 4 T magnetic field. The CMS silicon tracker contains 10 million microstrips read out by around 80,000 custom CMOS integrated circuits called the APV25 [2] & [3]. The APV25 will be exposed to ionising doses up to 10 Mrad during LHC operation and, during the design and development phase, much care was taken to ensure a high degree of total dose radiation tolerance. Another concern is that the high particle fluxes in the experiment will give rise to Single Event Upsets (SEU). A previous version of the chip fabricated in a 1.2 μm bulk CMOS process [4] has been tested for SEU [5]. The APV25, fabricated in a 0.25 μm CMOS process, has now been tested and results are presented in this paper.

To predict the upset rate in the complete CMS Tracking system, a full evaluation of the digital circuits in the APV25 has been performed by exposing the chip to a beam of heavy ions at the INFN Laboratory of Legnaro, Italy, and to 300 MeV/c pions at the Paul Scherrer Institute (PSI) in Switzerland. Extensive simulations of SEU in the APV25 were carried out and a model was developed to predict upset cross-sections, extending ideas reported in [6]. The model provides an alternative to the widely used Weibull fit to SEU data, based on the concept of multiple upset modes within a sensitive storage cell.

1.1. The APV25

The APV25 is a 128 channel readout chip. Each channel consists of a low-noise amplifier, the output of which is sampled at the 40 MHz LHC bunch crossing frequency into a 192 element deep analogue pipeline memory. The pipeline enables storage of tracker data for up to four μs (trigger latency) while decisions are taken as to whether an interesting physics event has taken place, limiting the trigger rate to 100 kHz. When the chip receives an external trigger, analogue samples are retrieved from the pipeline, processed and fed to a single output via a 128:1 analogue multiplexer. The output data stream contains these 128 analogue samples, preceded by a digital header which contains an error bit and the pipeline column address (location of one of the 192 "time-slices") from which the data were retrieved.

The APV25 has fast and slow control interfaces. Slow control uses the I^2C industrial protocol [7] and is used to program registers which define operational modes of the chip and on-chip DACS to define currents and voltages required by the analogue circuits. The fast control signals consist of the 40 MHz LHC clock and a trigger.

Only the digital functionality of the chip can be compromised by SEU events. Effects are expected in the analogue circuitry but they cannot cause logic errors which affect chip operation. The areas which can be upset consist of pipeline control logic, I^2C registers, FIFO memory, which stores addresses of pipeline columns awaiting readout, and the main control logic block, which handles external communication and controls readout sequencing. The digital functionality of the chip can be illustrated by considering operation of the chip after power-on.

(i) Following power-on, a reset signal is applied to initialise the main control logic and communication interfaces.

(ii) The I^2C registers are programmed with their 8-bit operational values via the slow control interface.

(iii) Once the 40 MHz clock is present, a fast synchronous reset (Reset101) is transmitted on the trigger line. A write pointer is produced which circulates in the pipeline logic at the 40 MHz clock frequency, controlling sampling of signals into pipeline memory cells.

(iv) After a programmed number of clock cycles, defined by the I^2C latency register, a trigger pointer is produced which also circulates in the pipeline logic. The distance in time between write and trigger pointers should always remain at the fixed latency value. This is monitored on-chip and the error bit in the next output frame header is set if a discrepancy is detected, which can occur if the pipeline logic suffers an SEU.

The chip is now fully initialised and normal triggers can be applied. When a trigger occurs, the pipeline cell at the current location of the trigger pointer is reserved for readout and its address loaded into the FIFO. The write pointer will subsequently skip over columns marked for readout until they have been read out. The readout of all 128 channels plus digital header information takes 7 μs.

SEU effects in the APV25 pipeline logic under irradiation can be detected by observing the triggered pipeline column address and comparing with the expected value, or by observing the header error bit while masking other areas of the chip which, if upset, could cause the same symptoms. Upsets in the FIFO can be detected in a similar fashion. Sending the chip a Reset101 can clear these error states. SEU effects in I^2C registers can be studied by comparing data written with values read back. Upsets to the main control logic can be observed in the output data frame, but can only be recovered by issuing a hard reset.

1.2. The SEU phenomenon

SEU is a non-destructive phenomenon that affects both dynamic and static memory registers storing logic states. It manifests itself as temporary error appearing in a circuit and is caused by deposition of charge by an ionising particle. Fig. 1 shows a circuit for a 1-bit memory element, which is designed to have two stable states. In each state two transistors are on and two off. An upset occurs when a sufficient injection of charge at points 1 or 2 causes the state of the cell to invert. For this to occur two basic criteria must be met: the charge collected from an incident particle strike must be larger than a critical value Q_{crit}, which is the minimum required to cause the state to invert, and the particle must strike close enough to a sensitive circuit node where sufficient charge can be collected fast enough. The sensitive volume (SV) of one memory element is defined as that volume in which the incident particle must strike to cause an upset.

An energetic particle travelling through the SV can generate a spurious electrical signal by depositing charge along its path. The magnitude of the charge is dependent on Linear Energy Transfer (LET)[2] of the ionising particle, as well as the path length over which the charge is collected.

2. Measuring SEU

In order to measure accurately the upset cross-section of a specific memory device it must be exposed to a beam of known particle species and energy. In general there are two experimental measurements that can be made to test susceptibility to SEU. One is to measure the upset rate by placing the device in radiation equivalent to the expected working environment. The other is to place the device in a beam of heavy ions and evaluate the dependence of upset cross-section on incident LET.

The ideal measurement is the SEU rate in the final system which can be made by irradiating in an experiment equivalent to the expected radiation environment. Commonly used particles for LHC applications are low energy protons and pions, where upsets occur through nuclear interactions between the beam and silicon lattice, as knock-on silicon ions within the device may deposit enough energy to cause upsets. However, it is often difficult to reproduce the radiation environment in a controlled experiment. Another disadvantage can be that a low SEU rate yields poor statistics in reasonable exposure times.

The LHC radiation environment has a spectrum of energy deposition that covers a wide LET range. SEUs could be caused by small charge deposits just sufficient to cause an upset or by extremely heavily ionizing particles where the charge is collected with a magnitude well in excess of Q_{crit}. By measuring the response over a range of LET values, one can predict the behaviour in any environment by convoluting the resulting distribution with the relevant LET spectrum.

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[2] LET is a measure of a particle's rate of energy transfer in a particular material and is given by $LET = \frac{dE}{dx} \bullet \frac{1}{\rho}$, where ρ is the density of that material. All values of LET in this paper refer to energy transfer in silicon and unless otherwise stated they are the value at the surface of the chip before any energy has been lost to the silicon.

Therefore, in order to predict SEU rates, it is necessary to know the upset probability for precise values of deposited charge. This is achieved by using mono-energetic heavy ion radiation containing a single ion species with a well-known surface LET, thus allowing an accurate calculation of the deposited charge [8]. By selecting different ion charge states or adjusting the beam energy, it is possible to irradiate a device with a range of LET, giving rise to a corresponding upset cross-section. The cross-section, σ, is defined at normal incidence as:

$$\sigma = \frac{N_{events}}{\Phi}\left[cm^2\right] \qquad [2.1]$$

where Φ is the total incident particle fluence, and N_{events} is the number of SEU events counted during the test.

3. LET dependence of SEU cross-section

Fig. 2 shows typical heavy ion SEU data where the upset cross-section σ of the device is plotted as a function of normally incident ion LET and is fitted with the widely used Weibull function. The cross-section has a distinct threshold and then a relatively slow rise to saturation.

The Weibull function has no underlying physical significance but has provided a convenient method for parameterising data and extracting the threshold LET and saturated cross-section. It is given by:

$$\sigma = \sigma_{sat}\left\{1-\exp\left[-\left(\frac{LET-LET_{th}}{W}\right)^{S}\right]\right\} \qquad [3.1]$$

where s, σ_{sat} , W and LET_{th} are free parameters. LET_{th} is the minimum LET for upsets to occur and σ_{sat} is the saturated cross-section for high values of LET.

The simplest possible explanation for the variation of cross-section with LET assumes identical memory cells in a circuit where charge deposited by normally incident ions is always contained within an infinitesimally small volume around the ion trajectory. The sensitive volume is taken to be a cuboid so the cross-section is expected to be a step function, since any ion traversing the sensitive volume will deposit a

fixed charge. Therefore if this charge is greater than the critical charge, an upset will always be caused. This is not the case in reality as can be seen from Fig. 2.

Peterson et al. initially attributed the cross-section behaviour to a distribution of memory cell sensitivities and cell-to-cell variations in critical charge resulting from processing [9]. Massengill et al. have modelled cross-sections of SOI memories based on statistical variations of parasitic bipolar gain and critical charge distributions [10]. On the other hand, Langworthy has been able to model upset cross-sections for several technologies by ignoring critical charge variations altogether [11]. This model assumes the cell has a range of collection depths, which leads to the concept of an LET-dependent sensitive volume size. Another model is based on the variation of the collection volume with LET due to the influence of the deposited charge on the local electrical field, this influence on the electric field being more pronounced for higher LETs [12] & [13]. Only a small proportion of the slowly rising cross-section could be attributable to such variations, since the continuing increase in saturation cross-section can be as much as one order of magnitude. A recent study of SEU demonstrates that the sensitive volume varies as a function of LET, with simulations showing a double-hump structure in the cross section curve as first the n-channel, then the p-channel drains of a given cell become SEU sensitive with increasing LET [14].

In their work on SEU in a static register cell (amongst other types of cells), Faccio et al. identified four different modes of upset, each having a different critical charge and corresponding to a different critical area [6]. Simulations presented in this paper extend the ideas of [6], demonstrating that in the case of normally incident ions, the variation of SEU cross-section with LET can be attributed to the switching on of different modes of upset within one cell. Each mode is defined as a unique source of SEU within one circuit, with a distinct threshold LET and cross-section. A number of such modes then combine to give the observed structure. Furthermore, different types of cell possess different numbers of modes and a unique cross-section structure.

4. Simulations of SEU in the APV25

4.1. Sensitive circuits

In the APV25 the sources of SEU are digital pointers of the pipeline memory, the FIFO address memory, the I^2C control logic and data registers and main control logic. They comprise three types of digital memory element: simple D Flip-Flop (DFF) (Fig. 3), D Flip-Flop with set (DFF-set) and D Flip-Flop with reset (DFF-reset). Each circuit responds differently to deposited charge with characteristic upset thresholds and cross-sections, even though underlying physical mechanisms are identical in each case.

SEUs can be induced in both master and slave sections of each type of DFF, depending on whether the clock is high or low. Both master and slave of the DFF are two cross-coupled inverters with two transmission switches. For example, the I^2C registers in the APV25 are made up of simple DFFs which are clocked only during chip set-up procedure. Consequently only the slave need be considered when predicting the behaviour of the I^2C registers. Similar investigations have been performed for master and slave in each of the three types of DFF, but it is necessary here to consider only one circuit, since the principles are identical for all.

In the simple DFF, there are three nodes where charge can give rise to an upset, which are labelled A, B and C in Fig. 4. Each node has two critical charges, one for the state transition 1 to 0, the other for 0 to 1. The sensitive parts of these nodes are the depletion regions surrounding the highly doped n^+ and p^+ implants, which form the drains and sources of the FETs. The n^+ implants are capable of collecting electrons, therefore charge collected here can only cause an upset if the state of the node is high. The opposite is true for the p^+ implants. In total there are 5 sensitive n- and 5 sensitive p-implants, shared by the three nodes in the following way: nodes A and B contain 2 of each, and node C contains one of each. Table 1 summarises the sensitive implants, the transistor and node to which they belong, and their surface area. By summing the appropriate combination of areas, an estimate of the normal incidence upset cross-section can be made.

4.2. SPICE Modelling

To establish the critical charge for each mode the circuit was modelled in SPICE and the injection of a simple piecewise linear current pulse (50 ps rise and 100 ps fall) in the three nodes was used to simulate the collection of charge deposited by an incident ion within a given circuit. To find the critical charge one must inject pulses with an increasing amount of charge, checking the response of the circuit after each.

The SPICE simulation was performed for all upset modes in the three types of DFF. Table 2 shows, for the simple DFF slave and each mode of upset, the simulated critical charge, the sensitive areas and the implant type in which the charge must be collected.

4.3. Sensitive area of APV25

The total sensitive areas for both 1-0 and 0-1 transitions in the master of both DFF-set and DFF-reset are found to be similar, being $\cong 23\ \mu m^2$. However, it is important to note that there is some difference between the 1-0 and 0-1 transitions in each of the slaves. Therefore, to make an accurate prediction of the cross-section of a particular circuit made up of a number of either of these DFFs it is necessary to know the number of bits normally at 1 and 0.

The simple DFF is only used in the un-clocked registers of the APV25, so no upsets can occur in the master except when the memory is being loaded. The time it takes to load is only one clock cycle (25 ns), so it is not necessary to consider the DFF master in the analysis of the APV25. However, the pipeline logic and control logic are continually clocked and therefore both master and slave are sensitive to upsets. Simulations of master and slave in both the DFF-set and DFF-reset have also been performed and the results are used in the calculations of total cross-section. The number of modes is slightly larger for these circuits since they are more complicated and have more sensitive nodes and implants. The circuits in the APV25 are made up of combinations of the different types of DFF. By summing the sensitive areas for 1-0 and 0-1 transitions and weighting according to the normal state of each bit, one can estimate the saturated upset cross-section for each circuit.

The I^2C registers are programmable and therefore their state is known and the appropriate cross-section can be calculated. The experiments performed on the APV25 were done with a total of 29 bits set to 1 and 80 bits set to 0, so it follows that:

$$\sigma_{registers} = 29 \times 11.8 + 80 \times 15.3 = 1566 \mu m^2 \qquad [4.1]$$

Similar calculations have been carried out for the pipeline logic, the FIFO and the control logic leading to the results given in Table 3. The main contributor can be seen to be the pipeline logic.

4.4. LET dependent cross-section

Previous measurements of σ have been fitted with the Weibull function, which implies that σ rises slowly in the plateau region as the incident LET increases. From section 4.2 it is clear that there should be a number of distinct modes of upset each with a different threshold LET.

To predict the heavy ion upset cross-sections, a conversion of critical charge obtained from the SPICE simulations into an equivalent LET is required. It is therefore necessary to understand what happens between the deposition of charge by a heavy ion and the subsequent collection of this charge. EVEREST, a semiconductor simulation package, was used to simulate the charge collection process in simple transistor structures [15]. The EVEREST simulations were based on assumptions about the transistor structure, doping densities and doping profiles since access to the process details was restricted by the manufacturer. The charge collection efficiency was found to be almost 100% for the n-type implants and roughly 50% for the p-type implants. The critical charge obtained from the SPICE simulations was combined with the charge collection efficiency from the EVEREST simulations to derive values for the equivalent LET. Since 3.6 eV is required to generate an electron-hole pair, the critical energy is given by:

$$E_{crit} = \frac{Q_{crit}}{\alpha e} \times 3.6 \qquad \text{and} \qquad LET_{th} = \frac{E_{crit}}{z\rho} \qquad [4.2]$$

where Q_{crit} is the critical charge from the SPICE simulations, α is the charge collection efficiency from the EVEREST simulations, ρ is the density of silicon and the variable z represents the sensitive thickness of the implants, which is the charge collection depth [16]. The value of z can only be determined

experimentally from the data by measuring LET_{th} as it is technology dependent. The low charge collection efficiency for the p-modes increases their LET_{th}.

Using the initial simple assumption of an abrupt step-like function for each mode, the total SEU cross-section can be obtained by summing cross-sections for each mode:

$$\sigma = \sum_{i=0}^{Nn} \sigma_n^i (LET) + \sum_{i=0}^{Np} \sigma_p^i (LET) \qquad [4.3]$$

where N_n is the number of n-modes and N_p is the number of p-modes. 1-0 and 0-1 transistions must be considered separately. Each component of σ_n^i and σ_p^i can be represented by a single Weibull function, Equation [3.1]. Each mode has its own values of LET_{th} and σ_{sat}.

Cross-section predictions for a simple DFF for both 0-1 and 1-0 transitions are shown in Figs. 5 and 6 assuming a sensitive depth of 1 μm [17]. Variations in the true sensitive depth will have the effect of modifying the value of LET_{th} without changing the overall structure.

Fig. 6 shows that, in some cases, steps in the experimental data could quite easily be obscured due to statistical errors. Observing this behaviour in practice would require a complete scan of incident LET, which is not normally possible. Fig. 5 shows more distinctive steps which should improve the chance of seeing structure experimentally.

Circuits such as the control logic would exhibit a smoother rise to saturation because of the large number of modes present, including contributions from master and slave, and both 1-0 and 0-1 transitions.

5. Heavy ion beam tests

5.1. SIRAD irradiation facility at Legnaro

The irradiation was performed at the SIRAD irradiation facility [18] located at the 15 MV Tandem accelerator of the INFN Legnaro National Laboratory (LNL). During irradiation the particle flux and uniformity are monitored by an array of silicon diode detectors read out with pulse counting electronics. Fluxes from a few 10^4 to $2x10^5$ $cm^{-2}s^{-1}$ with a uniformity better than a few percent on the chip area were

delivered during the tests. Table 4 shows the full range of ion species chosen for these tests along with their energies and effective LETs which will be discussed in section 6.

5.2. Experimental set-up

Control of the experimental set-up was performed by a PC running LabVIEW [19], which communicated with a VME crate via a PCI interface. The trigger sequence for the APV25 was provided by a sequencer, and control of the APV25 performed by a slow control interface. The APV25 output was digitised by a flash ADC.

The test board for the APV25 is shown in Fig. 7. It had to be capable of withstanding vacuum in excess of 10^{-7} mbar, with no significant out-gassing. Aluminium masks, ~1 mm thick, were machined to expose specific areas of the four chips in the beam. The location of these areas is shown in Fig. 8. The heavy ions used in the tests are easily stopped by a thin sheet of metal since ion range depends on species and kinetic energy, up to a maximum of 50 μm for 145MeV incident silicon.

To provide visual real-time evidence that SEUs were occurring, events were counted on-line. The software also included I^2C control for testing the APV25 static registers and a hard reset for testing the control logic.

5.3. Measuring errors in the APV25

In the event of an upset in the pipeline logic or FIFO, there are two possible outcomes: either the error bit in the output data frame is set, or the pipeline address in the output data frame is incorrect. The error bit is also set if an upset in the pointer logic causes the latency of the trigger pointer to change. Only a tiny proportion of upsets produces both outcomes simultaneously. When measuring upsets in the pipeline and FIFO, the chip is reset using only a soft 101 reset.

SEU events in the I^2C registers can be observed by writing defined values, reading back after an interval, and comparing with initial values. In this case it is possible to detect individual bits which have been upset.

Upsets in the control logic block can have a more disruptive effect, such as incorrect pipeline addresses, loss of digital header, or loss of entire data frames. When measuring upsets in the control logic a hard reset is required to restore the chip to normal operation mode since this fault condition would make it impossible to distinguish further error. A hard reset recovers the operation of the control logic, following which a soft reset must be applied before further readout.

It is important that the average number of upsets per time interval is small such that multiple errors do not occur within the same time interval and cause undercounting. Observations of SEU events were made during an interval defined as the sensitive time (ST). For the pipeline and FIFO, the ST is the period between a reset and subsequent readout, Fig. 9. In the case of the I^2C test, instead of a reset and trigger, one writes a simple 8-bit pattern followed by the ST and then a read. The bit pattern can be varied to establish the cross-section for both 1 to 0 and 0 to 1 transitions. In the case of the control logic sequence, the hard reset occurs just prior to the soft reset and ST is measured from the hard reset. The total sensitive time for one run is given by the product of the number of triggers and ST.

6. Heavy ion test results

Results in this section refer to measurements of the SEU cross-section for the pipeline and control I^2C registers. All cross-sections are plotted against effective LET. The effective LET in the sensitive volume (SV) takes into account the slight loss of energy in the material above the SV. Since the ion energy is well known (within 0.01%), the error in this value is essentially associated with the estimation of the charge collection depth. Although the true SV depth is unknown, an extra 1μm of inactive material would contribute only a 1% error in the effective LET.

Fig. 10 shows the SEU cross-section for the pipeline and Figs. 11 and 12 show the SEU cross-sections in the I^2C registers for 0-1 transitions and for 1-0 transitions respectively. The I^2C registers illustrate clearly the effects predicted in section 4. As expected, it is difficult to see any structure in the data for upsets from 1 to 0. However comparing Fig. 6 and Fig. 12, it can be seen that the overall shape is similar to expectations. The data for 0-1 transitions display clear steps very close in appearance to predictions (Figs. 5 & 11). Note

that the saturated cross-section of 0-1 transitions is almost an order of magnitude lower than that of 1-0 transitions; reasons for this will be discussed later. The saturated cross-section for the 1-0 transitions is very close to the predicted value, but it should be noted that the prediction depends on the assumption made for p- and n- sensitive depths.

6.1. Model comparisons with data

By fitting both a single Weibull function and the predictions of the model developed in section 4.4, a comparison can be made. The cross-sections from the model are calculated from:

$$\sigma = w_2 \sum_{i=0}^{Nn} \sigma_n^i \left(LET, w_0\right) + w_3 \sum_{i=0}^{Np} \sigma_p^i \left(LET, w_1\right) \quad [6.1]$$

where N_n is the number of n-modes and N_p is the number of p-modes. Each of the $N_{n/p}$ components of σ_n^i and σ_p^i can be represented by a single Weibull function:

$$\sigma_{n,p}^i = \sigma_{nsat,psat}^i \left(1 - \exp\left\{ -\left[\frac{LET - \left(w_{0,1} LET_{nth,pth}^i\right)}{W_{n,p}} \right]^{s_{n,p}} \right\} \right) \quad [6.2]$$

Each mode has its own values of LET_{th} and σ_{sat}, taken directly from the simulations. W_n , W_p , s_n and s_p are fixed parameters whose values were chosen to make the individual Weibull functions close approximations to step functions for computational convenience.

The fitting parameters w_0 and w_1 vary LET thresholds for the n and p modes individually which is attributed to the difference between the true sensitive thickness and assumed value of 1 μm. Therefore the true sensitive thickness, for both n and p modes, can be extracted after fitting and is given by the inverse of w_0 and w_1. w_2 and w_3 perform the same function for the saturating cross-section. The n-mode parameters w_0 and w_2 are different to the p-mode parameters w_1 and w_3 because of differences in the charge collection efficiency.

Using a standard curve-fitting algorithm to vary w_2 and w_3 produced weight values and an associated error. However, it was not possible to use the algorithm to vary w_0 and w_1 because the cross-section is composed of step functions, which prevented convergence. To circumvent this problem the fit was

performed by setting w_0 and w_1 values to position the steps to correspond to observed steps in the data. The error was then defined as the available range between the two nearest points on different plateaus, combining this with the error in the effective LET. In all cases, the error was dominated by the step positioning.

Fig. 10 shows results for the pipeline logic fitted with a standard Weibull function and a function derived from the different modes of upset. The statistical error is small because of the large cross-section and steps in the data, though relatively small, are clearly visible. The χ^2 for the model fit is clearly an improvement on the Weibull description, even though the absolute value is still relatively large. Extracting the sensitive depths from the fit gives 1.69 ± 0.02 μm for the n modes and 1.85 ± 0.09 μm for the p modes.

In Fig. 11 which shows the 0-1 cross-section for the I^2C registers, both Weibull and model fits describe the data with small χ^2 but visually the measured points display clear plateaus which match the theory. Extracting the sensitive depths and using the same considerations for the errors gives 1.47 ± 0.15 μm for the n modes and 1.69 ± 0.09 μm for the p modes, comparing well with those extracted from the data for upsets from 1-0, as would be expected.

Fig. 12 shows the 1-0 cross-section for the I^2C registers fitted with a Weibull function and the model. These data demonstrate that low statistics (due to the low cros-section) combined with expected small steps (section 4.4) can make it difficult to see structure in the data, and in this case neither fit is more convincing. The extracted sensitive depths are 1.33 ± 0.02 μm for the n modes and 1.69 ± 0.09 μm for the p modes.

6.2. Discussion

Predictions of the FIFO and control logic cross-sections can be made in the same way as those of the bias registers and pipeline. However, these circuits are considerably more complicated and uncertainties of order factor 2 should be expected.

The more circuits involved in the upset mechanism, the smoother the cross-section behaviour becomes. In such cases it is easier to fit the data with a simple Weibull function to extract the values of LET_{th} and σ_{sat}. All the extracted values of σ_{sat} are shown in Table 5 along with geometrical predictions, which are taken as

the sum of the sensitive areas from all modes. The pipeline and I^2C σ_{sat} predictions are close to the measured values with the exception of the I^2C 0-1 transitions.

Table 6 summarises the sensitive depths extracted from three data sets, which are in good agreement with each other. The two I^2C measurements are comparable as would be expected since they come from the same circuit. The differences between them and those of the pipeline are small but outside the error range. However, it should be noted that these measurements are for two different circuits. The similarity in the ratio between the n and p modes is encouraging. This indicates a consistency in the fitting of different data sets, which does not apply to the Weibull function.

6.3. Upset rate predictions for the CMS tracker

From the heavy ion cross-section data and CMS simulations of secondary particle energy spectra [20], upset rates for the APV25 during CMS operation can be calculated. Table 7 gives a breakdown of the predicted upset rates in the CMS tracker at full LHC luminosity. The average predicted SEU cross-section of the APV25 in the tracker is ~ 10^{-12} cm^2. It is difficult to give a quantitative estimate of the error in this prediction; the simulation code does not include a treatment of the errors because the region of the spectrum in which LET_{th} lies falls off rapidly with increasing LET. Therefore, to confirm the estimated rate, a measurement of the cross-section in a representative radiation environment was made by exposing APV25 chips to a 300 MeV/c pion beam at the PSI in Switzerland.

7. Pion beam test

7.1. Irradiation facility at PSI

The irradiation was performed at the πE1 beam-line of the PSI in Villigen (Switzerland), which delivers a quasi-continuous beam of positive pions at a momentum of 300 MeV/c. The average flux of 10^9 cm^{-2} s^{-1} covered an FWHM area of approximately 10 x 12 mm^2. A total fluence of almost 2 x 10^{14} cm^2 was accumulated in several runs. The average beam flux was calculated with an estimated error of 15% using the decay of the ^{24}Na activation product in aluminium foils used for calibration.

7.2. Experimental set-up

Unlike heavy ions, 300 MeV/c pions are minimum ionising particles which penetrate several cm of material. Thus, it is not possible to mask chip areas, nor is a vacuum chamber required for the tests. This was exploited by placing a stack of eight APV25S1 chips into the beam. The chips were operated in a cooled environment at –10°C with a dry nitrogen atmosphere for the majority of the measurement time.

The electronic readout hardware used in the pion test was custom-made at HEPHY Vienna [21], providing similar functionality compared with the heavy ion test system.

7.3. Measuring errors in the APV25

The procedure of detecting pion induced single event upsets was slightly different from that used in the heavy ion measurements. Here, all chips were continuously triggered and read out at a rate of several hundred Hz. Each event data was checked online for irregularities such as a set error bit or inconsistent pipeline addresses. Once an error was detected, it was examined in detail and logged before hard and soft resets were applied to all chips followed by a restart of the measurement loop. Different types of measurements were performed in a global loop with a cycle time of one minute (Fig. 13). These included normal events, internal calibration events, the observation of voltages and currents and a dedicated I^2C read-back test.

While the heavy ion tests were performed with a defined sensitive time window (terminated by an unconditional reset) within which SEUs could happen or not, the software used for the pion test was continuously polling for SEUs and only applying a reset when necessary. In total, about 40 million events were analysed for each of the eight chips.

The analogue pipeline, which essentially consists of capacitors, is also sensitive to charge deposition from heavily ionising particles or fragments. However, their effect is less dramatic since these fake signals simply appear as an increase in the noise background. Moreover, no action is required to clear the analogue circuitry, since the pipeline cells are periodically re-written such that affected cell contents disappear automatically. However, fake hits may result when such corrupted cells are read out. Therefore, in addition

to digital effects, analogue signals were also recorded. A threshold of 40 times the individual channel rms noise was applied to the signals in order to safely distinguish fake hits from random electronic noise.

8. Pion test results

In total, about 3000 SEUs were observed on all eight APV25 chips, or approximately one in 10^5 events. From the event analysis, the origin of the upset could be partially reconstructed. However, since masking was not possible and one cannot distinguish between errors in the pipeline or control logic blocks only by analysing the output, we can only state a combined error rate for these units in contrast to the heavy ion tests.

The pion fluence at CMS at a radius of 22 cm, the first silicon microstrip tracker layer, over 10 years of operation is 10^{14} cm^{-2}. At PSI, all eight chips were exposed to levels exceeding the CMS lifetime pion fluence. Each chip contains approximately 200000 transistors, corresponding to a total of 1.6 million transistors. A failure in any one of these transistors would have been visible. The supply current measurements of the chips did not reveal any irregularity during the whole irradiation period. No chip failure was observed indicating that there was no permanent damage such as latch-up or Single Event Gate Rupture.

8.1. Pion induced SEUs

The measured cross-section at a temperature of 20^{o}C is $\sigma = 1.99 \times 10^{-12}$ cm^2 and is $\sigma = 2.25 \times 10^{-12}$ cm^2 at a temperature of -10^{o}C.

The pion cross-section is lower than with heavy ions by a factor of approximately 10^8 due to the fact that only secondary reactions (such as recoil Si atoms) deposit sufficient charge for an upset which the pions themselves are not capable of. In the case of heavy ions however, every particle produces an upset once the threshold energy is exceeded.

96% of all upsets affect the data flow either in the pipeline logic, the FIFO or the control logic. The remaining SEUs were observed in the I^2C registers. Table 8 compares the measured cross-sections for these parts to the sensitive areas.

8.2. Prediction for the CMS tracker

The measurement of the pion SEU cross-section allows easy extrapolation to the CMS tracker. Pions with a momentum below 1 GeV/c are the predominant source of radiation in the inner part of the CMS detector. Due to their high nuclear interaction cross-section (Δ resonance peak) 300 MeV/c pions are believed to be the most damaging type of radiation occurring within CMS. Thus it is a safe assumption to directly extrapolate the pion SEU cross-section to obtain the upset rates in the CMS tracker. Since neither particle types nor energy spectra are taken into account, this simple prediction should be regarded as a worst-case scenario including a considerable safety margin with respect to normal CMS operation. In fact, the numbers shown in Table 9 are significantly higher than the more detailed extrapolation performed with the heavy ion data (Table 7).

The analogue occupancy, i.e. the fraction of channels affected by an analogue transient at any given moment, is negligible compared to the true hit occupancy which is in the order of a few percent.

More details of the single event upset tests with pions including analogue transients are given in [21].

9. Summary and Conclusions

The APV25 has been irradiated by heavy ions to evaluate its susceptibility to SEU. A model based on the detailed analysis and simulation of circuits within the APV25 has been developed and successfully compared with experimental data. Values for the sensitive thickness of the circuits of both n and p modes have been extracted from the data and show consistency between measurements.

The results have been used to predict the upset rates in the CMS tracker giving a value of 0.15% of chips upset per hour, which is well within tolerable limits. This result is supported by recent experimental measurement of the APV25 cross-section in a 300 MeV/c pion beam. The digital errors do not pose a

problem provided that a periodic reset is applied to the APV25 chips with an interval of the order of minutes or less. Ionization in the analogue circuitry leads to fake hits which appear merely as a negligible increase in background noise and since it disappears automatically it does not require any action. No permanent damage, such as latch-up or Single Event Gate Rupture, was observed for a pion fluence exceeding the CMS 10-year fluence.

Acknowledgements

We thank PPARC for financial support, the INFN and all the technicians at the TANDEM for the time in the beam and technical support at Imperial College and the University of Padova. Moreover, we are grateful to K. Gabathuler for his support with the πE1 beamline at PSI.

References

[1] CMS Tracker Technical Design Report. CERN/LHCC 98-6 (1998).

[2] M. Raymond et al., Proceedings of the LHC Electronics-Board Workshop, CERN Report CERN/LHCC/2000-041, 2000, p.130.

[3] L. Jones, "APV25-S1 User Guide version 1.1", http://www.te.rl.ac.uk/med/.

[4] M. Raymond et al., Proceedings of the LHC Electronics-Board Workshop, CERN Report CERN/LHCC/97-60, 1997, p.158.

[5] J. Fulcher et al., Proceedings of the LHC Electronics-Board Workshop, CERN Report CERN/LHCC/99-33, 1999, p.513.

[6] F. Faccio et al., IEEE Trans. Nucl. Sci. NS-46 (1999) 1434.

[7] Philips Semiconductors "The I^2C Bus Specification", http://www.semiconductors.philips.com/acrobat/various/I2C_BUS_SPECIFICATION_3.PDF.

[8] J.F. Ziegler. "Stopping and Range of Ions in Solids", Vol.1, Publisher: Pergamon Press, New York 1985.

[9] E.L. Peterson et al., IEEE Trans. Nucl. Sci. NS-39 (1992) 1577.

[10] L.W. Massengill et al., IEEE Trans. Nucl. Sci. NS-40 (1993) 1804.

[11] J.B. Langworthy, IEEE Trans. Nucl. Sci. NS-36 (1989) 2427.

[12] C. Detcheverry et al., IEEE Trans. Nucl. Sci. NS-44 (1997) 2266.

[13] P. Roche et al., IEEE Trans. Nucl. Sci. NS-45 (1998) 2534.

[14] P.E. Dodd et al., IEEE Trans. Nucl. Sci. NS-48 (2001) 1893.

[15] J.V. Ashby et al., "Everest Version 4.0", Mathematical Software Group, Department for Computation and Information, Rutherford Appleton Laboratory, Chilton, Didcot, December 1998.

[16] J.R. Fulcher, "Radiation Effects in Electronics for the CMS Tracking Detector", PhD Thesis, RAL-TH-2001-007, July 2001.

[17] C. Detcheverry et al., Proceedings of the 1997 RADECS Conference, Palm Beach, Cannes, France, p.537, September 15-19, 1997.

[18] J. Wyss et al., LNL-INFN 163/2000, Nucl. Instr. and Meth. A 462 (2001) 426.

[19] LabVIEW Instrumentation Development Software, National Instruments, http://www.ni.com/.

[20] M. Huhtinen et al., Nucl. Instr and Meth. A 450 (2000) 155.

[21] M. Friedl, "The CMS Silicon Strip Tracker and its Electronic Readout", PhD Thesis, Vienna University of Technology, May 2001 (http://cern.ch/friedl → Dissertation).

FIGURES

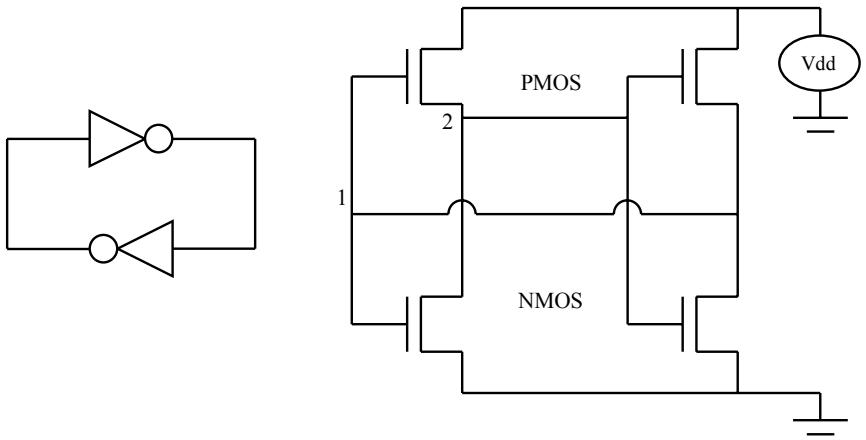

Fig. 1. Schematic representation of a memory cell composed of two cross-coupled inverters, and its circuit description.

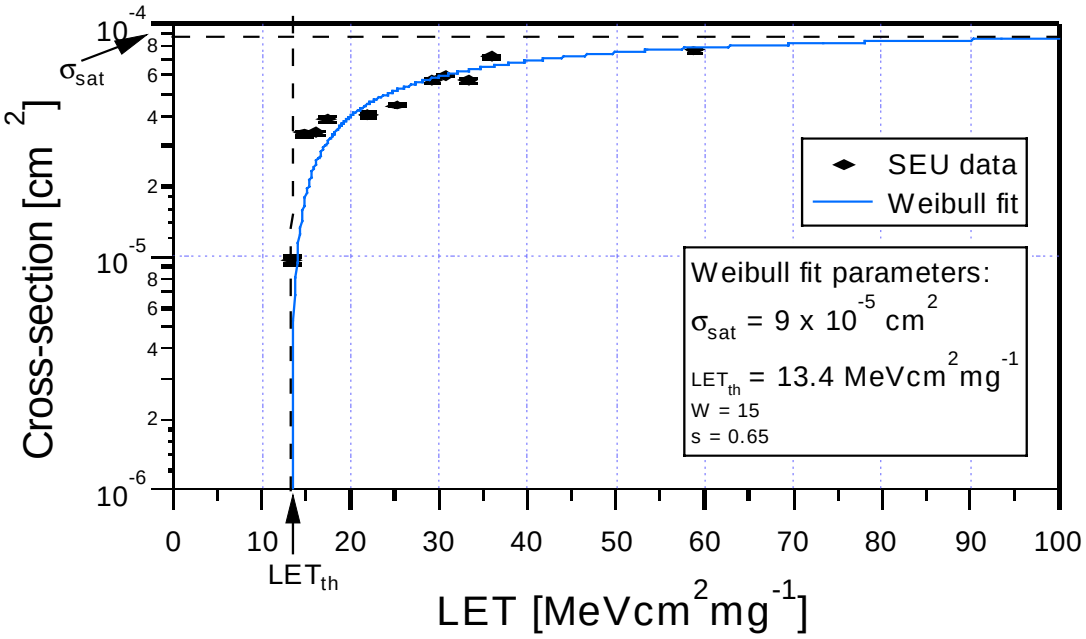

Fig. 2. A Weibull fit to a typical set of experimental measurements of SEU cross-section vs LET.

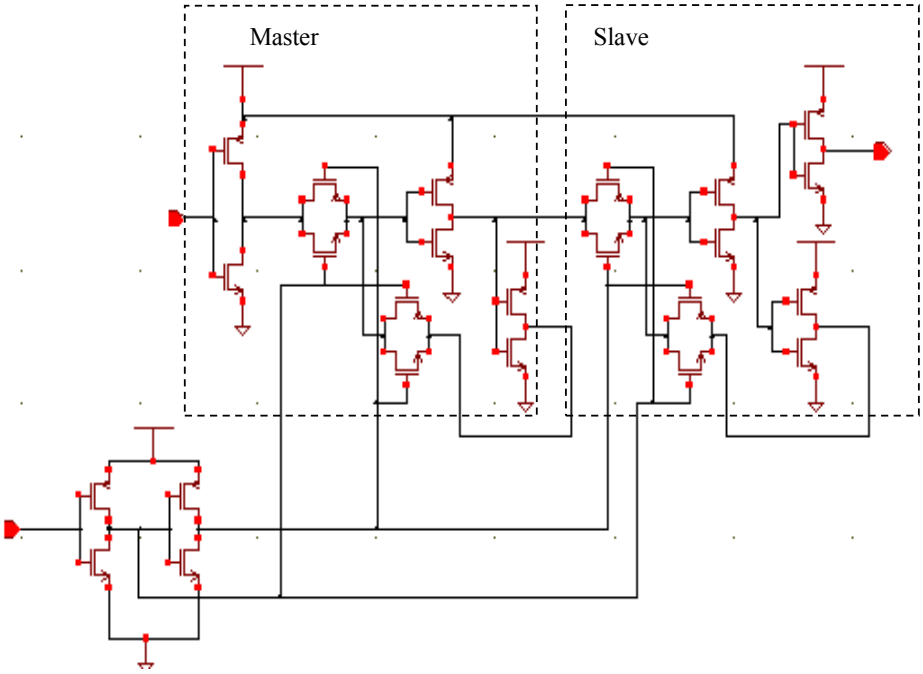

Fig. 3. DFF Schematic.

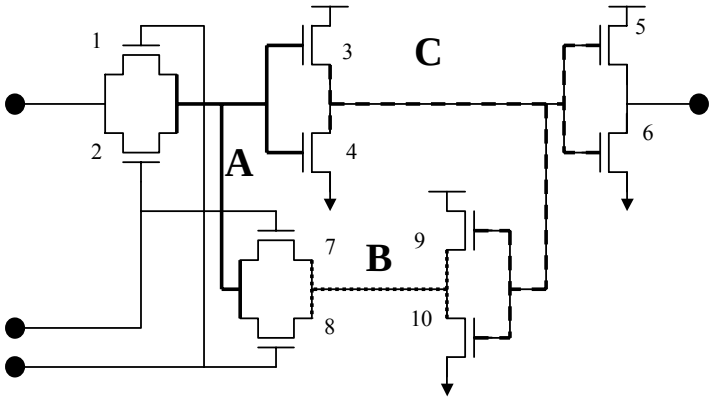

Fig. 4. Schematic of DFF slave.

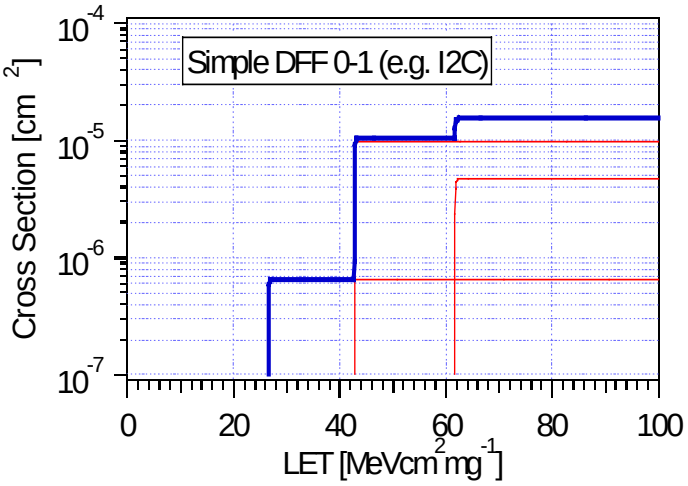

Fig. 5. Cross-sections predicted by the model for 0-1 transitions in a simple DFF.

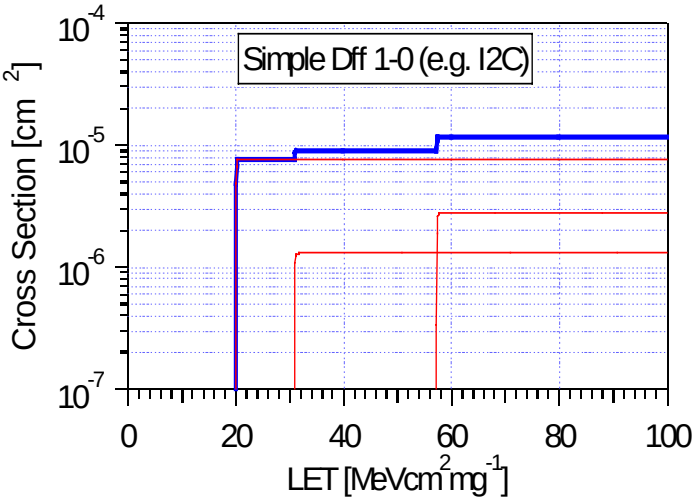

Fig. 6. Cross-sections predicted by the model for 1-0 transitions in a simple DFF.

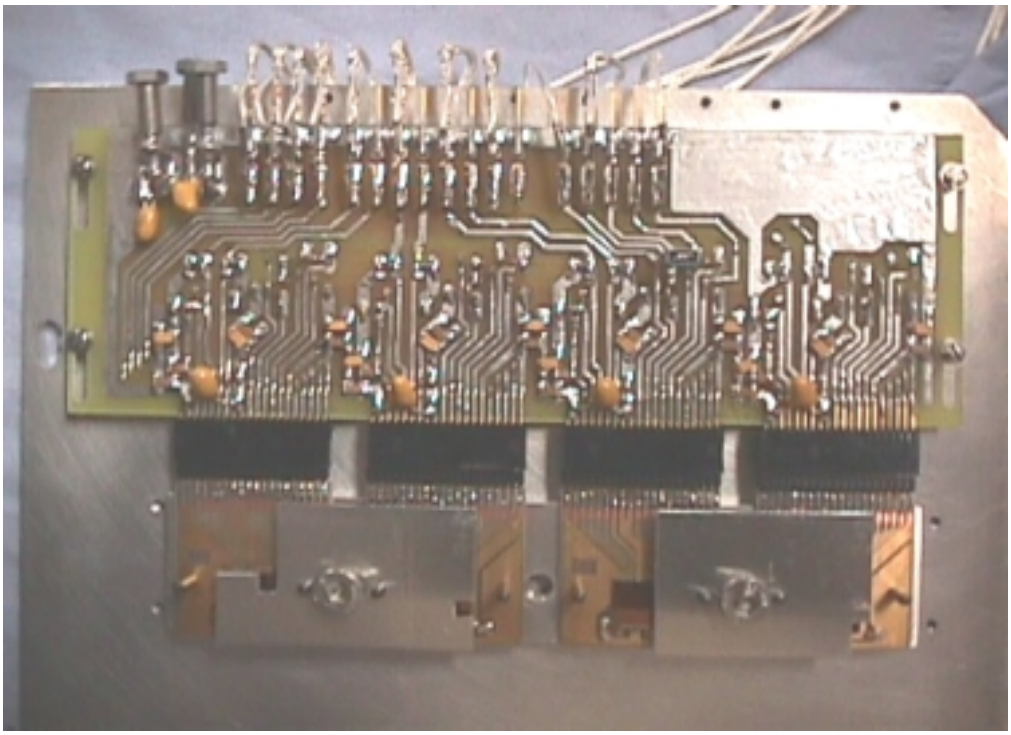

Fig. 7. APV25 SEU test board containing interface electronics, four APV25 chips and precision machined masks which obscure most of the APV25s.

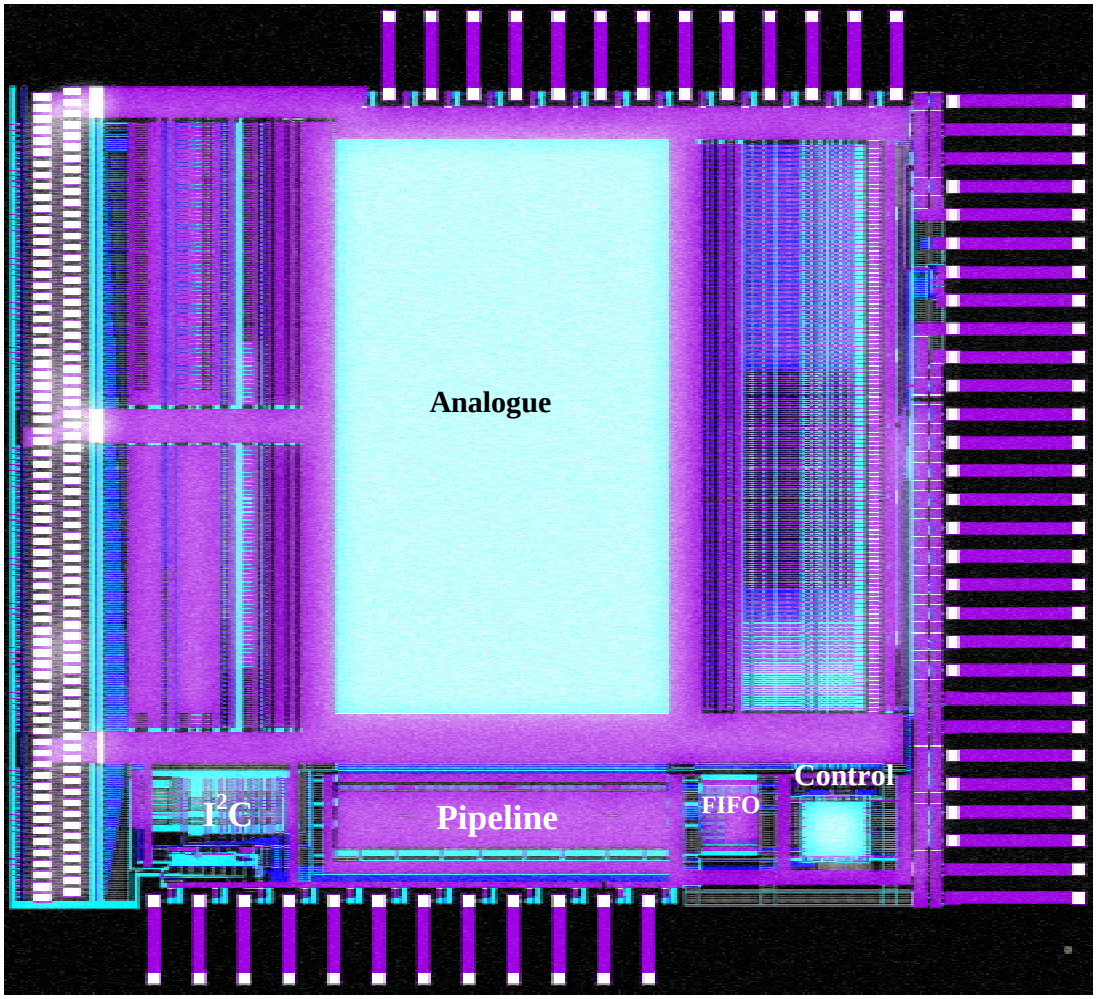

Fig. 8. APV25, showing the location of tested circuits. The dimensions of the chip are 7mm x 8mm.

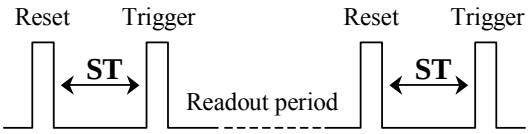

Fig. 9. Definition of the sensitive time (ST) for the pipeline logic.

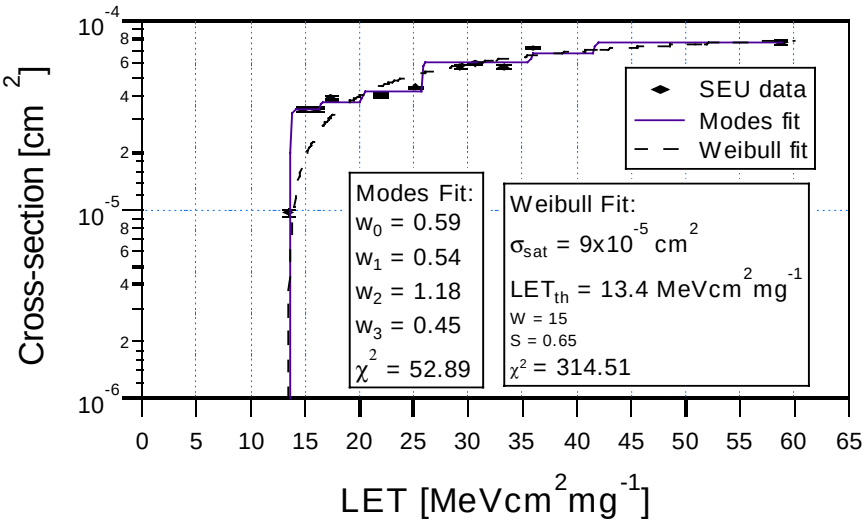

Fig. 10. SEU data for the pipeline circuitry. Both a standard Weibull fit (broken line) and a Modes fit (continuous line) are applied to the data.

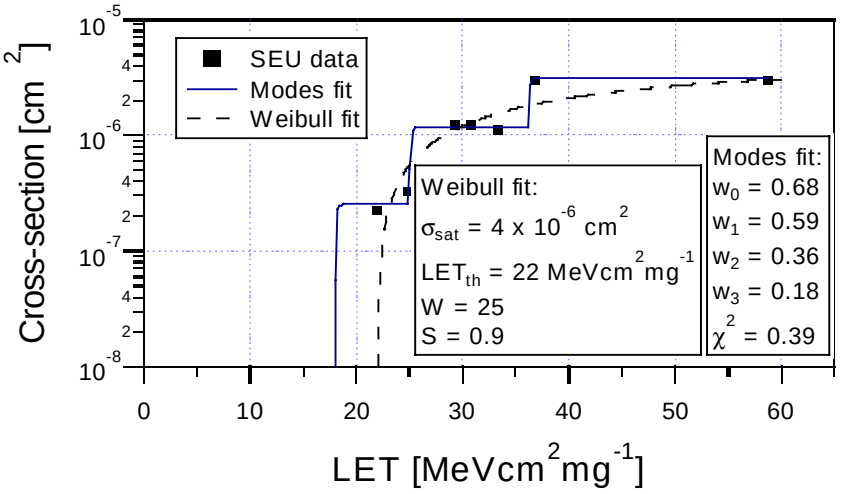

Fig. 11. I^2C registers 0-1 cross-section vs LET, showing Weibull and Modes fits.

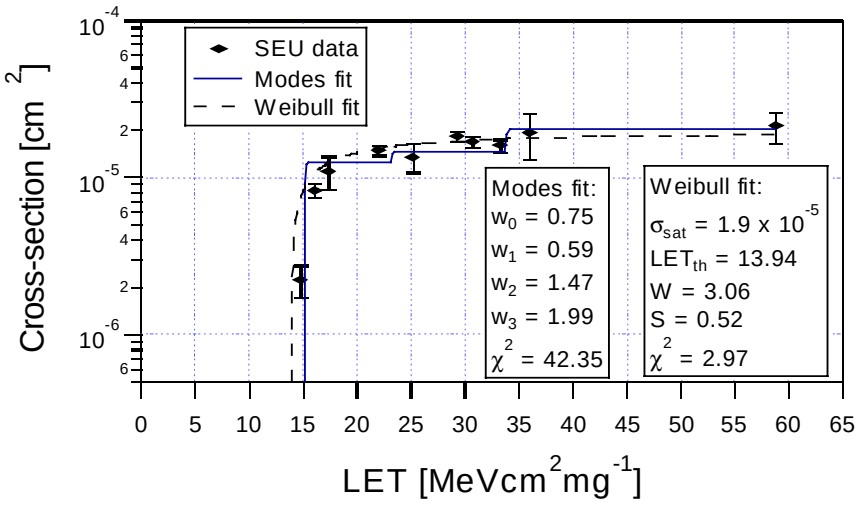

Fig. 12. I^2C registers 1-0 cross-section vs LET, with a Weibull fit and a Modes fit.

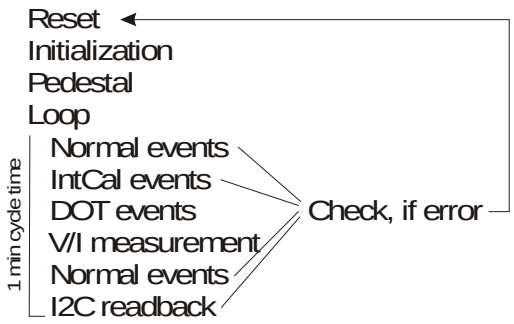

Fig. 13. The principal measurement procedure for the pion SEU test.

Figure name	Software	Magnification factor
Fig. 1	MSWord2000	70%
Fig. 2	Igor Pro 4.04	70%
Fig. 3		80%
Fig. 4	MsWord2000	70%
Fig. 5	Igor Pro 4.04	80%
Fig. 6	Igor Pro 4.04	80%
Fig. 7		50%
Fig. 8		50%
Fig. 9	MSWord2000	100%
Fig. 10	Igor Pro 4.04	70%
Fig. 11	Igor Pro 4.04	70%
Fig. 12	Igor Pro 4.04	70%
Fig. 13		100%

TABLES

Table 1

Sensitive implants of DFF.

Sensitive implant	Implant type	Number of transistor	Associated node	Surface area [μm^2]
1	n-source	2	A	3.85
2	n-drain	4	C	0.65
3	n-drain	8	A	0.65
4	n-source	8	B	3.85
5	n-drain	10	B	0.65
6	p-source	1	A	4.97
7	p-drain	3	C	2.77
8	p-drain	7	A	1.96
9	p-source	7	B	4.97
10	p-drain	9	B	2.77

Table 2

Sensitive area and critical charge from SPICE simulations for six modes in a DFF slave.

	Upsets from 1-0			Upsets from 0-1		
	Q_{crit} [fC]	n or p	σ [μm^2]	Q_{crit} [fC]	n or p	σ [μm^2]
Hit on A	196	n	7.7	212	p	9.94
Hit on B	304	n	1.3	306	p	4.73
Hit on C	284	p	2.77	260	n	0.65
Total	-		11.77	-		15.32

Table 3

Number of sensitive bits in APV25 sub-circuits and the total cross-sections.

	No. of DFFs	Sensitive Area [cm^2]
Pipeline Logic	768	14.9×10^{-5}
FIFO	40	0.6×10^{-5}
I^2C Registers	109	1.6×10^{-5}
Control Logic	167	2.8×10^{-5}

Table 4

Ions used in the APV25 heavy ion tests.

Ion	A	Energy [MeV]	Effective LET [MeVcm^{2}mg^{-1}]
Si	14	145	9.7
		100	11.2
Cl	17	160	13.5
		130	14.8
		107	16.1
		87	17.4
Ti	22	178	22.0
		115	25.2
Ni	28	237	29.3
		200	30.7
		138	33.3
Br	35	100	36.0
I	53	250	58.8

Table 5

Comparison of predicted and measured cross-sections. Statistical errors are smaller than the precision of the values quoted.

	Predicted σ_{sat} [cm^2]	Measured σ_{sat} [cm^2]
Pipeline	$1.1x10^{-4}$	$1.0x10^{-4}$
FIFO	$8x10^{-6}$	$3x10^{-6}$
I^2C (1-0)	$1.3x10^{-5}$	$2.1x10^{-5}$
I^2C (0-1)	$1.7x10^{-5}$	$0.3x10^{-5}$
Control	$2.3x10^{-5}$	$0.7x10^{-5}$

Table 6

Extracted sensitive thickness for n and p modes from three fitted data sets.

	N modes Sensitive Depth [μm]	P modes Sensitive Depth [μm]
Pipeline	1.69 ± 0.02	1.85 ± 0.09
I2C (1-0)	1.33 ± 0.02	1.69 ± 0.09
I2C (0-1)	1.47 ± 0.15	1.69 ± 0.09

Table 7

Upset rates in the CMS tracker.

Tacker region	Radius [cm]	No. APVs	No. SEU/Layer/s	Seconds/ SEU	No. SEU/hour	Fraction chips/hour
Inner Barrel	24-52	14400	1.46×10^{-2}	68.6	52	0.36%
Outer Barrel	60-115	29232	4.1×10^{-3}	243.7	15	0.05%
Inner Endcap	22-41	4416	5.15×10^{-3}	194.2	19	0.42%
Forward Endcap	33-106	30208	8.58×10^{-3}	116.5	31	0.10%
Total	-	78256	3.24×10^{-2}	30.9	116	0.15%

Table 8

Comparison between sensitive area and cross-section of pion SEU on the APV25S1.

	Sensitive Area [cm^2]	Cross-section [cm^2]
Pipeline + Control	$15.9\ 10^{-5}$	$19.1\ 10^{-13}$
FIFO	$0.43\ 10^{-5}$	$0.14\ 10^{-13}$
I^2C Registers	$1.57\ 10^{-5}$	$0.73\ 10^{-13}$

Table 9

Extrapolation of the pion SEU cross-sections to CMS. Due to simplified assumptions, these numbers only indicate the order of magnitude, but can be regarded as a worst-case scenario (see text).

Tracker region	Average Flux [cm^{-2} s^{-1}]	Number of APV25s	Mean SEU time [s]	SEUs/time [h^{-1}]
Inner Barrel	1.04E+06	14400	29.7	121
Outer Barrel	1.80E+05	29232	84.7	43