The MGPA Electromagnetic Calorimeter Readout Chip for CMS

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Abstract

The Multiple Gain Pre-Amplifier is a three gain channel 0.25 micron CMOS chip matched to the noise and linearity requirements of the electromagnetic calorimeter for CMS. A choice of external feedback components to the first stage amplifier allows the chip to be used for both barrel and end-cap regions of the detector. Details of the design and performance measurements are presented.

I. INTRODUCTION

A new architecture has been proposed for the front end readout of the CMS electromagnetic calorimeter (ECAL) using a Multiple Gain Pre-Amplifier (MGPA) chip feeding a multi-channel ADC chip [1,2], both manufactured in a 0.25 micron CMOS process for radiation hardness.

The CMS ECAL detector uses Lead Tungstate scintillating crystals read out using Avalanche Photodiode (APD) and Vacuum Photo-Triode (VPT) photo-detectors in the barrel and end-cap regions respectively.
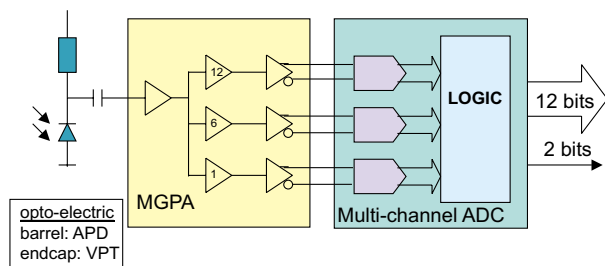

Figure 1. New CMS VFE architecture

The readout and precision performance requirements of the ECAL require that the front end signals are digitised to better than 12 bits. To avoid the requirement for a very high precision radiation hard ADC the approach has been to use multiple gain ranges to span the overall dynamic range, digitising and transmitting the signals only for the highest unsaturated range. Thus a 12-bit ADC is sufficient, but a decision must be made as to which channel is in range at the very front end (VFE). In the previous architecture this decision was made in the preamplifier, which was followed by a single channel commercial 12-bit ADC. The new architecture (figure 1) uses parallel gain channels in the MGPA, coupled to a multi-channel ADC, the channel-in-range decision being taken by digital logic following the conversion stages.

The MGPA and ADC chips have both been developed in 0.25 micron CMOS. This will lead to system simplifications where the chips use only a single 2.5 Volt supply at lower power. Other advantages are radiation hardness, high yield and cheaper mass production, together with short turnaround for design revisions.

The MGPA (and ADC) design has been undertaken on an aggressive schedule. The design phase began in mid 2002, with submission in early 2003. Die have been available since May 2003, and packaged chips since August.

II. DESIGN

The specifications for the MGPA chip are listed in table 1. The full-scale signal, noise level and input capacitance parameters differ for the barrel and end-cap applications owing to differences in the APD and VPT photo-electric conversion efficiencies. The output signal size is determined by the ADC input requirements. The final choice of 3 gain ranges and their ratios was made early in 2003 following a review of the specifications, with a view to maintaining the physics performance while easing the requirements for the MGPA design. The linearity and pulse shape matching requirements are demanding. The pulse shape matching is defined as the ratio of a sample taken on the output pulse 25 ns before the peak to the peak sample itself. The CR-RC pulse shaping time constant is specified to be 40 ns which, when combined with the 10 ns scintillation decay time, results in an overall output pulse peaking time of ~ 50 ns.

Table 1: MGPA specifications.

Parameter	Barrel	End-cap
Full-scale signal	60 pC	16pC
Noise level	10,000 e, 1.6 fC	3,500 e, 0.56 fC
Input capacitance	~ 200 pF	~ 50 pF
Output signals (to match ADC)	Differential 1.8V, +/- 0.45 V around 1.25 V common mode voltage	
Gain ranges	1, 6, 12	
Gain tolerance (each range)	+/- 10%	
Linearity (each range)	+/- 0.1% full-scale	
Pulse shaping	40 ns CR-RC	
Pulse shape matching	< +/- 1%	

A schematic view of the chosen architecture is shown in figure 2. The first stage is a charge sensitive amplifier with external feedback components C_F and R_F chosen to match the barrel or end-cap signal magnitudes. The $C_F R_F$ decay time constant of the first stage output pulse constitutes the differentiation component of the overall 40 ns pulse shaping time. This approach allows the first stage gain to be maximised, which helps to minimise noise contributions from the subsequent stages, while the short decay time avoids pulse pile-up.

The first stage is buffered by source followers to the three gain channels. The resistors R_{G1}, R_{G2} and R_{G3} set the gains and feed common gate stages which provide currents to match the inputs of three differential output stages.

The differential stages have current outputs and terminating resistors R_I and capacitor C_I are chosen to provide the 40 ns RC integrating time constant of the pulse shaping. This has the advantage that the low pass filtering occurs at the end of the signal processing chain and thus acts on all noise sources within the MGPA.
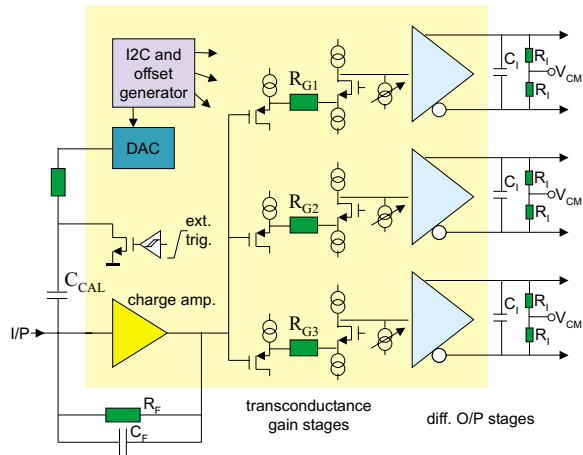

Figure 2. MGPA architecture overview

A calibration facility is included in the chip where charge can be injected into the MGPA input following an external trigger. The magnitude of the charge is produced by a simple DAC circuit which is programmed via an I^2C interface. The calibration facility is not intended for precision measurements but allows functional verification during chip screening and can also be used to verify the full electronic chain in the final system. The I^2C interface is also used to programme the individual offset (pedestal) levels at the outputs by setting the magnitudes of offset currents applied at the differential stage inputs, via a bias generator block.

The dominant noise sources in the MGPA are indicated in figure 3. For the first (charge amplifier) stage the feedback resistor R_{pf} dominates, contributing 4,900 and 2,700 electrons for the barrel and end-cap resistor values

respectively. The input FET dimensions are 30,000/0.36 (width/length ratio in microns), chosen to match the external capacitance for the barrel case, which results in a transconductance of ~ 0.3 A/V for this device. The noise contribution of this transistor is approximately 1,800 and 660 electrons for the barrel (200 pF) and end-cap (50 pF) external load capacitances respectively. The feedback resistor noise dominates and so the overall noise has only a weak dependence on input capacitance.
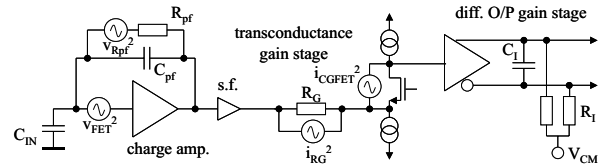

Figure 3. MGPA noise sources

Because the gain of the first stage is limited to accommodate the large full-scale signals, it is difficult to avoid noise contributions from the resistor and common-gate FET in the successive gain stages. For the high and mid-gain ranges the resistor values are low and the additional noise is relatively small. For the low gain range this resistor is 240Ω and the noise of the gain stage dominates. The simulated noise for the low gain channel is 35,400 and 9,800 electrons for the barrel and end-cap respectively, which is roughly three times the specification, but this is acceptable since this range is used for the largest signals and the electronic noise contribution to the overall energy resolution is negligible.
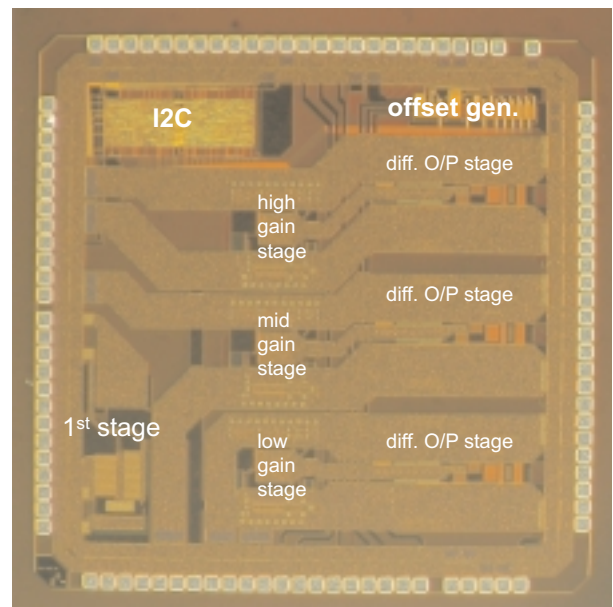

Figure 4. MGPA chip layout

The layout of the MGPA chip can be seen in the photograph of a die in figure 4 where the main circuit blocks are indicated. During layout care was taken to avoid coupling between gain channels since the higher gain channels will go into saturation for large signals. The gain channels are separated as much as possible with individual multiple power pads. The die size is approximately 4 mm. x 4 mm. and the chip is packaged in a 14 mm. x 14 mm. Thin Quad Flat Pack (TQFP) 100 pin package (figure 5).

Figure 5. MGPA chip in 100 pin TQFP package

III. TEST RESULTS

Figure 6 shows the setup used to characterise the MGPA performance. A test pulse is attenuated by a programmable RF attenuator and used to inject charge into the MGPA input via a calibrated capacitor. The MGPA output signals are sampled into a scope using single-ended or differential probes and the waveforms are acquired by a PC running LabVIEW.
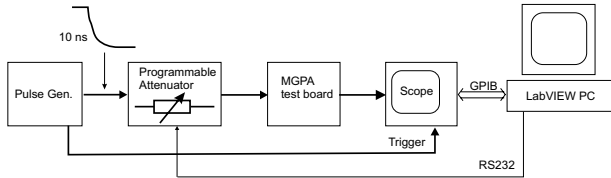

Figure 6. MGPA test setup

Figure 7 shows the MGPA output waveforms acquired differentially for 30 signal steps in the range 0 to 60 pC, corresponding to the full-scale signal range for the barrel case. The steps are not linearly spaced because of the logarithmic nature of the attenuator. The high and mid gain channels saturate while the low gain channel stays within the linear range. The gain ratios are measured to be 1:5.6:11.3 which compare well to the 1:6:12 specification (table 1).

Figure 8 shows linearity measurements for the high gain channel for different values of gain stage bias currents. The linearity is within (or very close to) specification for a range of bias currents, and is therefore not too sensitive to the operating point of the circuit. Linearity measurements for the mid and low-gain channels show similar results.
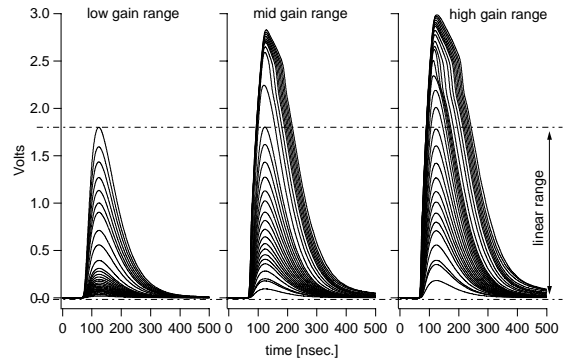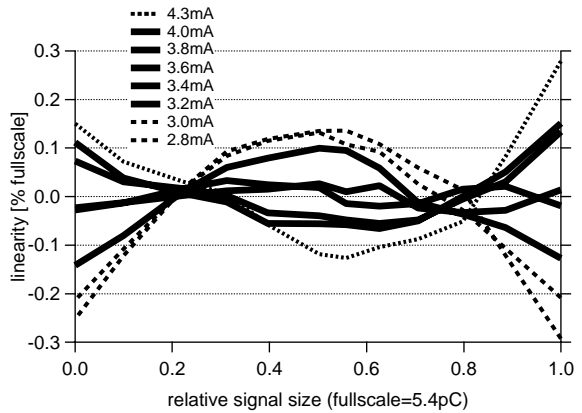

Figure 7. MGPA output pulse shapes

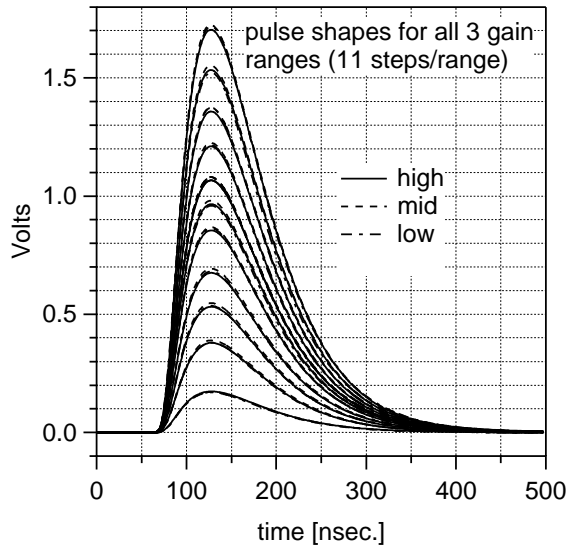Figure 8. Measured linearity for the high gain channel

Figure 9. Pulse shape measurements for all 3 gain channels

Figure 9 shows a range of amplitude pulse shapes for all three gain channels and figure 10 shows the same pulse shapes normalised to the maximum pulse height. Visually

the matching is good, but the specification demands that the pulse shape matching factor (PSMF) matches across and between ranges to +/- 1%, where the PSMF is defined as the ratio of the voltage 25 ns before the peak (Vpk-25) to the peak voltage Vpk. The pulse shape matching displayed in figure 11 is then given by,

$$\text{Pulse shape matching [\%]} = \frac{(\text{PSMF} - \text{Ave. PSMF})}{\text{Ave. PSMF}} \times 100$$

where Ave. PSMF is the average over all pulse shapes for all three gain ranges. Figure 11 demonstrates that the pulse shape matching meets the specification for most of the signal range.
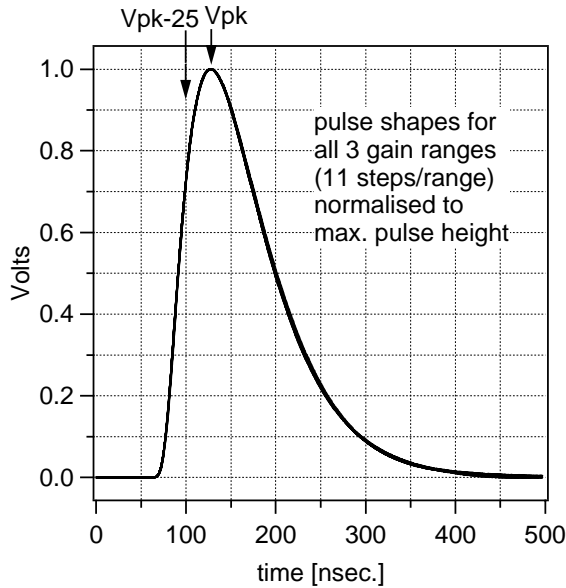

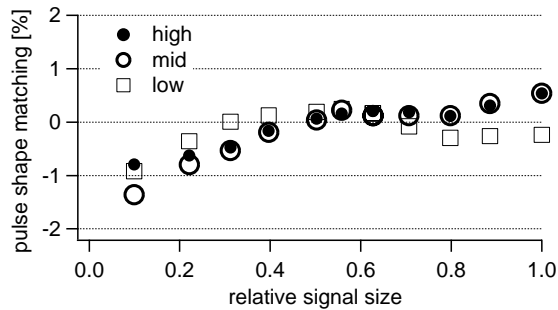Figure 10. Normalised pulse shapes for all 3 gain channels

Figure 11. Pulse shape matching across and between ranges.

The noise is measured using a wide bandwidth true rms meter and the results are given in tables 2 and 3 for the barrel and end-cap cases respectively. The single-ended to differential buffer circuit required contributes additional noise which has to be subtracted, and which dominates for the low gain channel. Errors are estimated to be at the 10 %

level for the high and mid gain ranges, and 20% for the low gain range. There is good agreement between simulation and measurement, comparing the measured noise with added capacitance with that simulated for a similar input capacitance. The noise is within specification for the high and mid-gain ranges as expected and the weak dependence on input capacitance is evident.

Table 2: Barrel noise performance [rms electrons]

gain range	measured noise Cstray (~ 20pF)	measured noise Cstray + 180 pF	simulation (200 pF)
high	7,000	7,850	6,200
mid	8,250	9,100	8,200
low	~ 28,000	~ 28,000	35,400

Table 3: End-cap noise performance [rms electrons]

gain range	measured noise Cstray (~ 20pF)	measured noise Cstray + 56 pF	simulation (50 pF)
high	2,900	3,050	2,700
mid	3,300	3,450	3,070
low	~ 8,500	~ 8,500	9,800

One chip has been irradiated with 10 keV X-rays to a dose of 5 Mrads (+/- 10%), which is twice the worst case dose expected in CMS. The noise performance is unaffected, the only measurable change being a 3 % reduction in gain (figure 12). The dose-rate was ~ 1 Mrad/hour and no annealing has been performed.
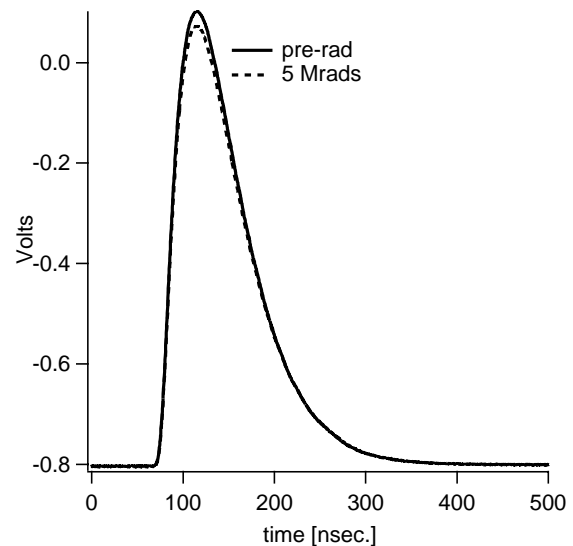

Figure 12. Pulse shape before and after irradiation.

Figure 13 shows the pulse shape response of the MGPA obtained using the on-chip calibration circuit (figure 2). The DAC is simply implemented using a chain of resistors between the supply rails, and the amplitude is programmed via the I2C interface. This allows a range of signal sizes to be produced for each gain range, depending on the value of the external charge injection capacitor C_{CAL}. The value of 10 pF used here allows signals up to 25 pC to be produced, which is why the low range signals in figure 13 do not cover the full linear range.
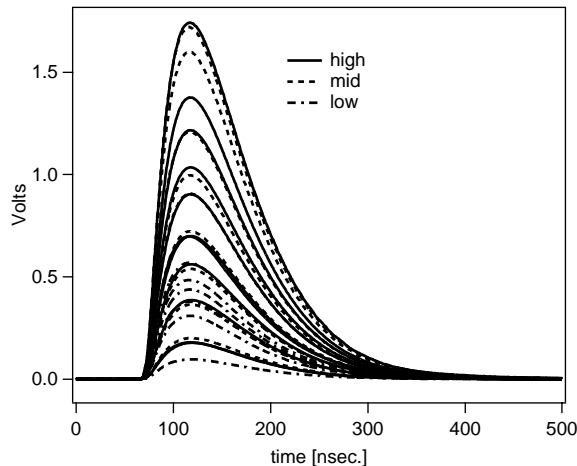

Figure 13. Calibration pulse shapes

The power consumption of the MGPA is approximately 600 mW, set by external bias resistors. The first stage, gain stages and differential output stages consume 150, 300 and 150 mW respectively.

It is premature to draw any conclusions on the yield of good chips but indications are that it is likely to be high. In basic functionality tests on 50 chips only one was found to have a fault in the I^2C interface circuitry.

Only one significant design flaw has been identified, which is a high frequency instability resulting from underestimating the inductance (due to bond wire and package) in the first stage feedback loop, because of the external feedback components. Stability has been achieved by inserting small resistors in series with the package pins to damp the resonance, and by reducing the current in the input transistor to reduce the bandwidth. Further work is underway here to fully characterise the problem, and to confirm that stability can be maintained with sufficient safety margin.

IV.   CONCLUSIONS

The first iteration of the 0.25 μm CMOS MGPA chip for the CMS ECAL has been successful. The analogue performance is within or very close to specification with respect to gain, linearity, pulse shape matching and noise, and performance is maintained after irradiation to 5 Mrads.

It is important that the measured performance is maintained in conjunction with the other components of the system, and tests of the full front end readout chain are underway at CERN.

V. ACKNOWLEDGEMENTS

VI.   REFERENCES

[1] The New Readout Architecture for the CMS ECAL, M.Hansen, these proceedings.

[2] A CMOS low power, quad channel, 12 bit, 40 Ms/s pipelined ADC for application in particle physics calorimetry, G.Minderico et al, these proceedings.