Production testing and quality assurance of CMS silicon

microstrip tracker readout chips

P.Barrillon[1], R.Bainbridge[1], D. Bisello[2], A.Candelori[2], M.French[3], G.Hall[1], A.Kaminsky[2], V.Khomenkov[2], J.Leaver[1], E.Noah[1 a], M.Raymond[1], L.Stefanutti[2], M.Tessaro[2]

[1]Blackett Laboratory, Imperial College, London, UK
[2]Dipartimento di Fisica and INFN Sezione di Padova, Via Marzolo 8, Padova, Italy.
[3]Rutherford Appleton Laboratory, Didcot, UK
[a] now in CERN, Geneva, Switzerland

p.barrillon@imperial.ac.uk

Abstract

The APV25 is the 128 channel CMOS chip developed for readout of the silicon microstrip tracker in the CMS experiment at the CERN Large Hadron Collider. Good radiation tolerance, low noise and reliable operation are required for the readout chips. Therefore, each of them is tested at the wafer stage using an automated procedure. A sample of dies from each wafer is also tested in more detail before and after irradiation. Now the production and testing are complete. The results obtained have proved the quality of the APV25 chips and their excellent performance.

I. Introduction

The APV25 is the readout chip for the CMS silicon microstrip tracker. It is a 128-channel CMOS circuit fabricated on 200mm wafers in 0.25 μm technology by IBM Microelectronics. This technology was chosen mainly for its high radiation tolerance [1]. A more detailed description of the chip can be found in [2] and the user manual [3].

The APV25 analogue chain is represented in Figure 1. The signal from a silicon microstrip detector is successively amplified by an integrating preamplifier, passed through an inverter and shaped by a low noise CR-RC amplifier with 50 ns time constant. The shaper output is stored every 25 ns in a 192 cell pipeline which accommodates a level 1 trigger latency of up to 4 μs plus buffering for events awaiting readout. Each channel of the pipeline is read out by the Analogue Pulse Shape Processor (APSP) which can operate either in *peak* or *deconvolution* modes. In peak mode only 1 sample per channel is read from the pipeline (timed to be at the peak of the analogue pulse shape); in deconvolution mode three samples are sequentially read and the output is a weighted sum of all three, resulting in an effective short pulse shape to achieve single bunch crossing timing resolution. The 128 analogue samples are finally multiplexed onto a single differential current output line.
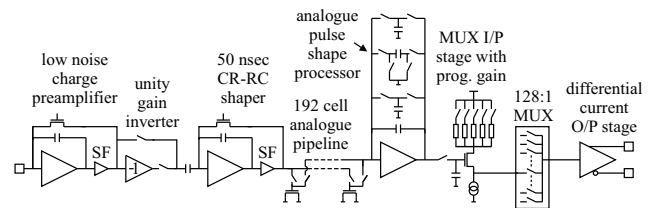

Figure 1: Diagram of the APV25 analogue chain. Each of the 128 channels has its own chain from the preamplifier to the multiplexer stage.

The testing of the chips is simplified by the fact that its operational modes can be programmed using an I^2C interface. This allows read/write access to all registers via software. Moreover, the chips have an internal calibration pulse generator, with programmable amplitude and delay, which allows the reconstruction and the tuning of the analogue pulse shapes by groups of 16 channels. Figure 2 shows a view of APV25 layout with the main blocks labelled.
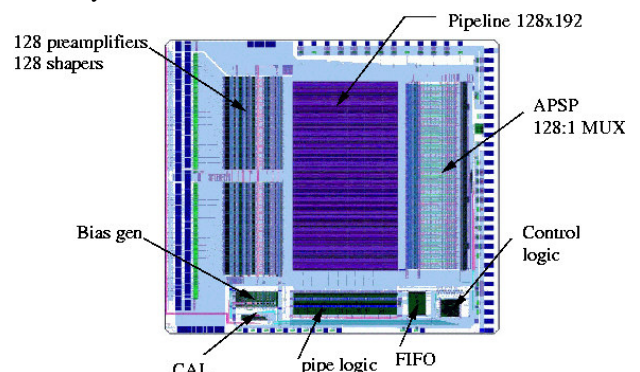

Figure 2: APV25 layout with main blocks indicated (bias gen: bias registers, CAL: calibration, APSP: analogue pulse shape processor).

Around 100,000 APV25 chips (including spares) are required to instrument $\sim 10^7$ detector channels [4]. In order to reach a high yield of multi-chips hybrids, comprehensive testing of the APV wafers was needed. Therefore a station to automate probing was developed to obtain a sufficiently high throughput using minimal manpower. Production has been staged over a period of ~2 years to allow wafer screening to keep pace with production. This also allows to quickly identify any problems that might arise during production, with low yield being a strong indicator of processing problems. Time constraints restrict the amount of testing possible during wafer screening; therefore more detailed quality assurance (QA) tests are carried out on chips sampled from the production wafers. These chips are also irradiated up to 10 Mrad(SiO$_2$)[1], at University of Padova and Imperial College, and their performance checked afterward. The aim of this paper is to describe the wafer probe and QA tests.

II. Wafer Probe Testing

A. Motivations

All APV25 chips must be exhaustively tested before integration into the final system to ensure high quality front-end readout modules and minimize the number of dead channels in the tracker readout system. Only fully functional and highly efficient chips will be used, therefore the wafer screening procedure must identify chips that satisfy stringent selection criteria with the highest possible efficiency and confidence.

B. Experimental Setup

The testing of the wafers is performed, individually, using a test station based around a semi-automatic probe station. The 360 APV sites of each wafer are automatically tested in nearly 7h (~70s per chip) with a minimal manpower (~20 minutes per day) [5]. The experimental setup of the wafer probing is shown in Figure 3, it consists of:

- a Micro-Manipulator 4460, 200 mm semi-automatic probe station controlled (via RS232) by a PC running LabVIEW;

- a VME based control and data acquisition (DAQ) system which instruments the APV25-PC interface;

- a probe card (inset in Figure 4), designed in-house to allow buffering, termination and decoupling as close as possible to the probe needles.

All the elements of the setup are controlled remotely and the programs execute all necessary tasks except the wafers alignment. Figure 4 shows the two main labVIEW Vis.

Two different types of tests are performed:

- digital tests: chip addressing, pipeline control logic…

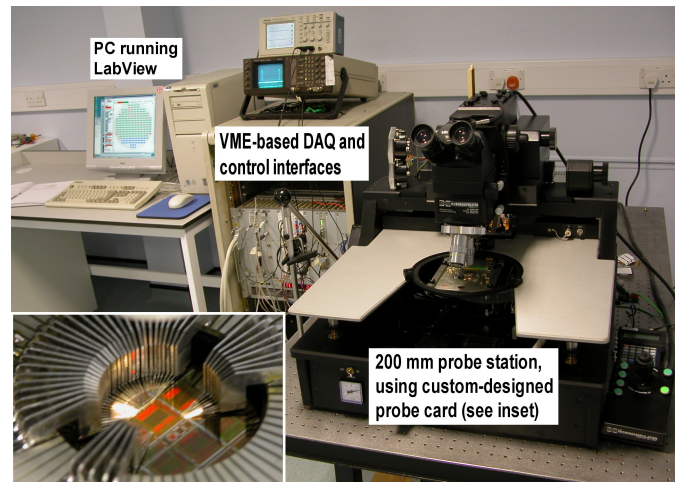- analogue tests: power consumption, pulse shaping, gain, pedestals and noise.

Figure 3: Experimental setup of the wafer probe testing.

Additionally, the chip is subjected to voltage screening tests that are designed to induce failures due to faults, such as weak gate oxides, that would not be identified under normal operating conditions.

At the end of each wafer probing a map is generated. It displays sites containing Known Good Die (KGD), namely chips that have passed all the screening tests.
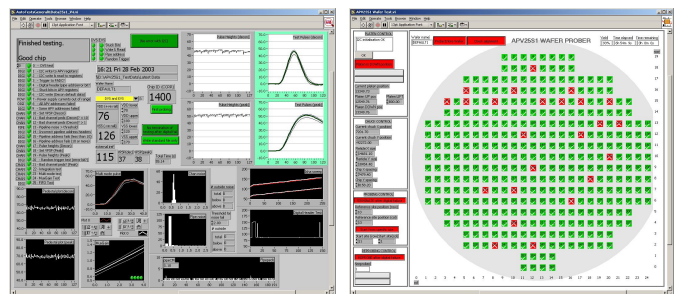

Figure 4: Left: Front panel of the APV25 wafer test LabView program (VI). Right: User interface for wafer probing. It provides a real-time wafer status-map with failed and correct chips.

C. Yield

The yield is the fraction of perfectly working chips per wafer lot[2]. This quantity is useful to estimate the quality and uniformity of the wafers production. A high yield is important not only to minimise chip production costs but also to prove the good quality control in the foundry during manufacture.

Table 1 gives the total number of wafers delivered and tested, as well as the average yield and the number of KGD. Lot 0 was an engineering run delivered in September 2000 by the company (IBM). The high yield (81%) achieved for the engineering run wafers (lot 0) was not maintained for the early production lots 1 – 8 and extensive investigations (summarised below) were required before the yields were returned to the stable and high levels evident for lots 9 - 25, delivered since June 2003. Almost 500 wafers have been probed in total. Figure 5 shows the evolution of yield as a function of lot number for all the lots produced.

---

[1] 1 rad corresponds to 10^{-2} joules absorbed per kilogram of the specified material (SiO$_2$). 1 rad $= 10^{-2}$ Gy = 100 erg.gm^{-1}.

[2] A wafer "lot" is normally a batch of 24 wafers which undergo all foundry processing steps at the same time.

Table 1: List of wafer lots with the number of delivered and tested wafers, the average yield and the total number of KGD (Eng is for engineering lot, Prod for production lot and Exp for experimental lot). The last three lines correspond successively to the total merging all lots, production lots from lot 3 and production lots from lot 9.

| Lot #	Type	Delivered wafers	Tested wafers	Average yield [%]	Number of KGD
0	Eng	9	9	81	2631
1	Prod	24	13	27	1264
2	Prod	21	12	10	432
3	Prod	25	25	79	7096
4	Prod	25	13	33	2532
5	Prod	20	16	47	3493
6	Prod	25	25	0	43
7	Prod	23	23	37	3104
8	Prod	24	24	58	4980
9	Prod	19	19	90	6128
10	Prod	22	22	81	6439
11	Exp	12	12	76	3271
12	Prod	22	22	79	6273
13	Prod	25	25	90	8075
14	Prod	1	1	91	329
15	Prod	24	24	91	7843
16	Prod	25	25	91	7891
17	Prod	25	25	79	7151
18	Prod	23	23	88	7319
19	Prod	24	24	91	7883
20	Prod	24	24	92	7991
21	Prod	22	22	91	7223
22	Prod	25	25	91	8173
23	Prod	1	1	94	339
24	Prod	2	2	94	676
25	Prod	24	24	83	7199
ALL	**-**	**519**	**499**	**70.02**	**125778**
> 2	**Prod**	**453**	**453**	**72.47**	**118180**
> 8	**Prod**	**308**	**308**	**87.42**	**96932**
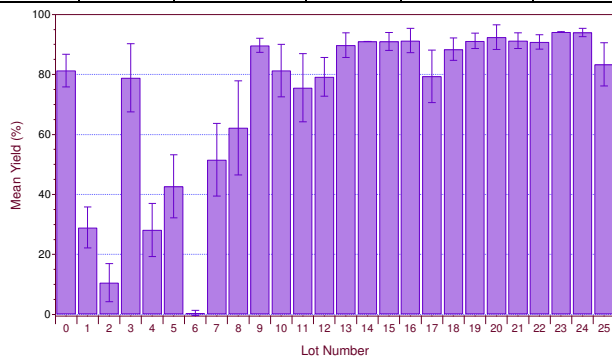
Figure 5: Mean yield as a function of the lot number. Error bars correspond to the standard deviation.

The first production lots (1 and 2) showed an unexpected low yield. A circular pattern was clearly visible, with good chips located at the wafer periphery and close to the center. Investigations at the foundry exhibited few defects in the silicide (TiSi$_2$) layer[3] for both lots. They were replaced by lots 3 and 4. An example of a low yield wafer map is shown in the left side of Figure 6.

---

[3] Silicide provides the contact layer to gates and source or drain implants.
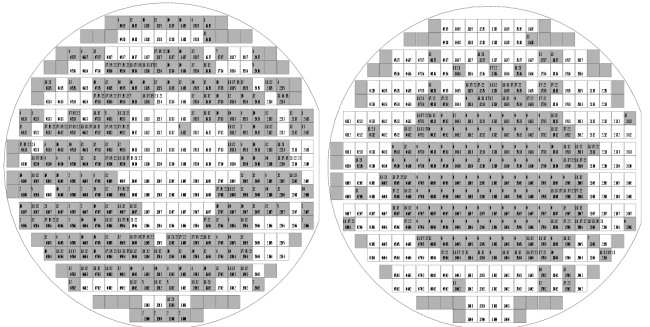

Figure 6: Wafer map example from lots 1 (left) and 5 (right). The white chips correspond to the KGD. Grey ones have failed at least one test.

Lot 3 was processed while the silicide investigations were ongoing. The average yield was high (79%) although a few wafers did show small central patches of failing chips. Similar patterns were observed more frequently on wafers of lot 4 and 5 (right side of Figure 6). The low average yield obtained for these lots (33 and 47 % respectively) and the three following (6-8: <1%, 37% and 58%) led to an important effort in investigating the causes of the variable yields for the APV25 up to mid 2003. The manufacturer's failure analysis (FA) teams and engineers worked in collaboration with CERN, Imperial College and Rutherford Appleton Laboratory. A complete description of the failure analysis carried out on returned APV25 wafers from lots 4 to 7 can be found in [6].

Figure 7 shows the APV25 layer structure. There are three layers of metal tracks (M1, M2 and MZ) connected by vias (V1 and V2) and insulated by an inter-level dielectric ILD. An intermediate layer Q2, separated from M2 with a thin dielectric, allows to realise metal-insulator-metal capacitors (MIMCAPs).
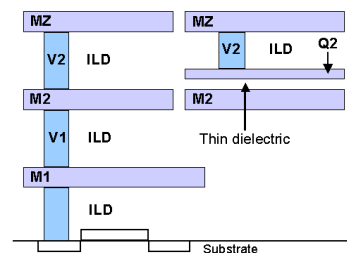

Figure 7: Schematic of the metal layers used in the APV25 chip.

Two types of fabrication problems were discovered:

- Lot 6: shorts, due to extraneous Q2 metal located in areas where it should have been removed, between tracks in the M2 layer were observed. It is now thought that this problem is an isolated example of a rare error occurring in the production line.

- Lots 4, 5 and 7: open circuits between layers (MZ and M2) were observed. A common feature for the wafers analysed from all three lots was that the inter-level dielectric was consistently thicker than normally expected and that etching, used to pattern the vias, therefore did not ensure contact to the M2 layer.

These results have led the company to tune the process for designs including large Q2 areas, such that the ILD thicknesses achieved would be closer to the nominal specified

value. All lots since lot 9 have been processed with this modified procedure.
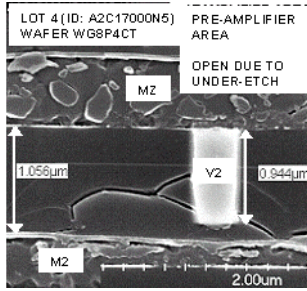

Figure 8: SEM (Scanning Electron Microscope) cross sections in the pre-amplifier (left) and pipeline control logic (right) regions. Under-etching is highlighted (image courtesy of IBM).

The probing performed on wafers from these lots has not highlighted new problems or strange patterns. The yields obtained have been consistently very high. Indeed for all production lots processed after the reduction of ILD thickness, average yields were better than 79 %.

D. Wafer Probe Test Results

Around 126,000 (97,000) chips, out of ~180,000 (111,000), have successfully passed the probing since lot 0 (9). Figure 9 shows the evolution of the number of dies tested and of the KGD as a function of the lot number.
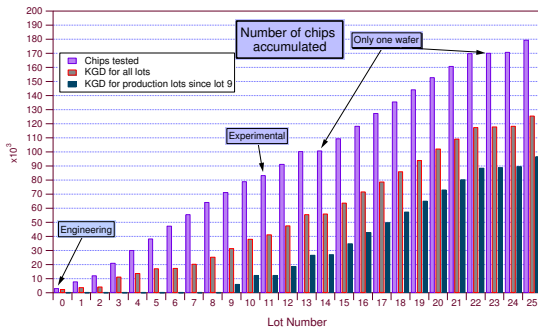

Figure 9: Evolution of the number of dies tested and successfully probed as a function of the lot number.

This paper presents the main results obtained up to the lot 18; a complete summary can be found in [6].

Figure 10 shows the averaged pulse shapes in peak and deconvolution modes, normalised to the maximum pulse height, for 1000 KGD of lots 8 and 13. Good pulse shape matching and uniformity are obtained with little wafer or lot dependence.

Measurements of supply currents, pedestals, gain[4] and noise also showed a nice agreement within lots and between wafers from different lots.

Indeed, the supply currents were found stable from wafer to wafer in the same lot (~2% dispersion) and between lots (~1% variation). Measurements showed a gain dispersion of less than 5% in peak and deconvolution modes for each lot and a 5.7% variation between lots.

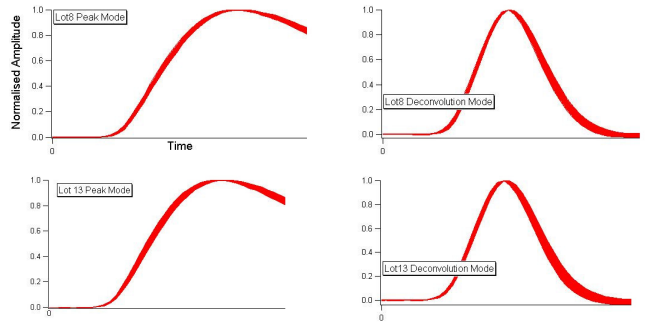[4] The gain is defined as pulse height maximum.

Figure 10: Averaged and normalised pulse shapes for 1000 KGD of lot 8 (top) and 13 (bottom), in peak (left) and deconvolution (right) modes.

Moreover, figures 11a-d symbolized this stability for the pedestals and the noise. Indeed the distributions (a and c) of these parameters, for all KGD of lot 18, exhibit a low dispersion and their evolution as a function of the lot number (b and d) shows a small variation from lot to lot.
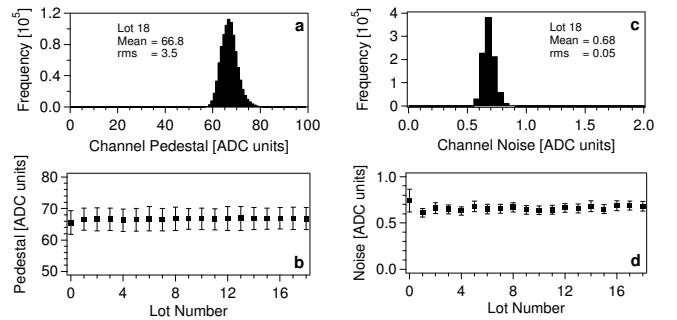

Figure 11: a) Distribution of channel pedestal for all the KGD of lot 18. b) Evolution of the mean pedestal (errors: rms) for KGD as a function of the lot number. c) Distribution of channel noise for all the KGD of lot 18. d) Evolution of the mean noise (errors: rms) for KGD as a function of the lot number.

In addition to these measurements, the pipeline performances have been studied. No problems were observed and a good stability within and between lots was obtained.

III. QUALITY ASSURANCE

A. Setup and procedures

As mentioned before, the objective of QA testing is to perform more detailed and accurate tests on chips sampled from the production wafers. Power consumption, noise and response to external and internal pulses are measured for each APV25 chip selected. In order to check the radiation tolerance of the chips, the same measurements are done after an irradiation up to $10Mrad(SiO_2)$ of each chip. These measu-rements are also performed before and after annealing for one week at $100\,^{o}C$.

In total, around 100 chips have been irradiated and half of them annealed. Since confidence of APV25 radiation hardness has been established with time the sample size has decreased from 100% (1chip/wafer) to 20% (5 wafers/lot).

Each chip to be tested is mounted on a small daughter card (~ 25 mm x 25 mm), which is plugged into a test card. This

card interfaces control signals, power and outputs. Some of the APV25 inputs are bonded to allow external charge injection and additional capacitive loads. Figure 12 gives a view of the daughter card with an irradiated chip. The rest of the equipment is similar to the one used for the wafer testing.
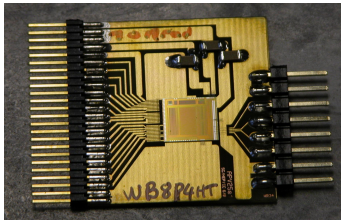

Figure 12: Daughter board with an irradiated APV25 chip.

An X-ray machine is used to irradiate the APV25 chips with an energy spectrum which peaks at 10 keV. Silicon diode detectors are used to perform dosimetry with an estimated accuracy of approximately 10%. Irradiation to 10 Mrad(SiO_2) takes less than 14 hours. During this test and annealing, the chip is biased, clocked and randomly triggered.

B. Results

The main results obtained on 56 chips tested at Imperial College are presented here; complete results can be found in [6].

Measurements performed has not exhibited significant differences after irradiation. As an example, the variation of the power supply currents mean value is less than 2% after irradiation. Figure 13 shows that the baseline and capacitance (channels with added capacitance) noises are also stable after irradiation in peak and deconvolution modes. Moreover the noise is also stable from a chip to another and between lots. After annealing the variation of the average noise is approximately equal to 1% in both modes.
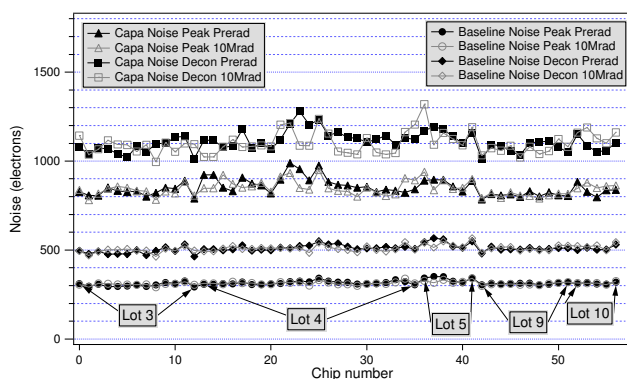

Figure 13: Evolution of capacitance and baseline noises, for peak and deconvolution modes, as a function of the chip number (arbitrary unit); before and after irradiation test.

Concerning the pulse shapes (externally and internally generated), the gain variation, before and after irradiation and annealing, is less than 1% and 2% respectively in peak and deconvolution modes. A good matching is obtained between lots in both gains.

Furthermore, the linearity is satisfactory up to ~3 MIPs and for a range of almost 5 MIPs, even after irradiation, whatever the mode.

IV. CONCLUSIONS

A system for the production test of large volumes of readout chips manufactured in a commercial 0.25 µm CMOS process for the CMS silicon microstrip tracker has successfully been developed. Approximately 126,000 chips have been probed successfully from around 500 wafers. Therefore enough spares are available in case of problem during the construction of the CMS silicon detector.

Unexpected variations in yield observed in early production lots have been studied thanks to an important collaboration between institutes and manufacturer. This close interaction was found to be of great importance in identifying and solving the problem, leading to excellent results with yields approaching 90% regularly on production lots. An excellent matching of all parameters was observed between channels, chips, wafers and lots.

Irradiation studies have also been carried out on samples from the production demonstrating only small changes in the circuit parameters to radiation levels well in excess of those expected during lifetime operation of the CMS silicon tracker.

V. Acknowledgements

VI. References

[1] Proceedings of 4th workshop on electronics for LHC experiments CERN/LHCC/98-36, 40-46, A.Marchioro, "*Deep submicron technologies for HEP*".

[2] Proceedings of the 6th workshop on electronics for LHC experiments, CERN/LHCC/2000-041, 130-134, M.Raymond et al, "*The CMS Tracker APV25 0.25 µm CMOS Readout Chip*".

[3] L.Jones, "*APV25s1 user guide version 2.2*", web site: http://www.te.rl.ac.uk/med/projects/main.htm

[4] CERN/LHCC/94-38, LHCC/P1, 1994, CMS Collaboration, "*The Compact Muon Solenoid Technical Proposal*".

[5] PhD thesis for the University of London, 2000-2004, R. Bainbridge, "*Influence of Highly Ionising Events on the CMS APV25 Readout Chip*".

[6] CMS NOTE 2004-016, R.Bainbridge et al, "*Production testing and quality assurance of CMS silicon microstrip tracker readout chips*".