The MGPA Electromagnetic Calorimeter Readout Chip for CMS

M. Raymond, J. Crooks, M. French, G. Hall

***Abstract*-- The Multiple Gain Pre-Amplifier is a three gain channel 0.25 micron CMOS chip matched to the noise and linearity requirements of the electromagnetic calorimeter for CMS. A choice of external feedback components to the first stage amplifier allows the chip to be used for both barrel and end-cap regions of the detector. Details of the design and performance measurements are presented.**

I. Introduction

THE Compact Muon Solenoid (CMS) experiment will be one of two general purpose experiments at the CERN Large Hadron Collider (LHC). The electromagnetic calorimeter (ECAL) detector is based on Lead Tungstate ($PbWO_4$) scintillating crystals read out by Avalanche Photo-Diodes (APDs), in the high transverse magnetic field of the barrel region, and Vacuum Photo-Triodes (VPTs) in the more severe radiation environment of the end-cap regions [1].

The desired ECAL performance requires that the front end signals are digitized to almost 16-bit accuracy, but using multiple gain ranges in the pre-amplifier, digitizing and transmitting signals only for the highest unsaturated range, 12 bits is sufficient. The decision as to which channel is in range must be made on the detector at the very front end (VFE). In the first version of the VFE readout architecture an analogue decision was made in the preamplifier, the analogue signal in range being digitized by a single-channel commercial 12-bit ADC [1]. More recently a new architecture has been proposed (Fig. 1) that uses parallel gain channels in a Multiple Gain Pre-Amplifier (MGPA) chip, which is coupled to a multi-channel 12-bit ADC. The channel-in-range decision is taken in the ADC chip by digital logic following the conversion stages.

The MGPA and ADC chips have been developed in 0.25 µm CMOS [2], [3] taking advantage of the well known radiation hardness [4]. This also leads to a simple powering scheme where both chips (and all other on-detector chips) are powered from a locally regulated 2.5 Volt power rail. Approximately 80,000 MGPA chips are required to fully instrument the ECAL detector, and experiences with this technology [5] have shown that a very high yield of fully working chips is achievable.

M. Raymond and G. Hall are with the High Energy Physics Group, The Blackett Laboratory, Imperial College, London SW7 2BW, UK (e-mail: m.raymond@imperial.ac.uk; g.hall@imperial.ac.uk).

J. Crooks and M. French are with the Micro-electronics Group, Rutherford Appleton Laboratory, Chilton, Didcot, Oxon 0X11 0QX, UK (e-mail: J.P.Crooks@rl.ac.uk; M.J.French@rl.ac.uk).

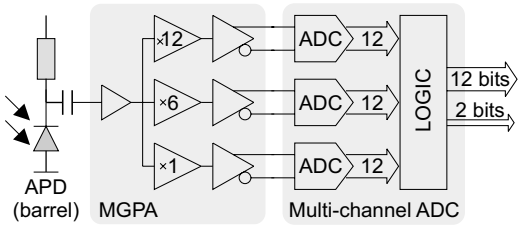

Fig. 1. Schematic representation of one channel of the CMS Very Front End (VFE) architecture, comprising two chips; the MGPA and a 12-bit multi-channel ADC.

The MGPA development has been undertaken on an aggressive schedule. The design phase began mid 2002, with submission of the first version in early 2003. The basic architecture was unchanged for the final version of the chip which was submitted late 2003, the main significant design change being the inclusion of an on-chip current reference circuit. This final version has been available since early 2004.

TABLE I
MGPA TARGET SPECIFICATIONS

	Barrel	**End-cap**
Full-scale signal	60 pC	16pC
Noise level	10000e, 1.6 fC	3500e, 0.56 fC
Input capacitance	~ 200 pF	~ 50 pF
Output signals (to match ADC)	differential 1.8V, ± 0.45 V around 1.25 V common mode voltage	
Gain ranges (tolerance/range)	1 : 6 : 12 (± 10%)	
integral nonlinearity	< ± 0.1% full-scale (each range)	
Pulse shaping	40 ns CR-RC	
Pulse shape matching	< ± 1% (within and across ranges)	

II. Design

The target specifications for the MGPA chip are listed in table I. The full-scale signal, noise level and input capacitance parameters differ for the barrel and end-cap detector regions

because of differences in full-scale energy requirement, the APD and VPT construction and photo-electric conversion efficiencies. The output signal size is defined by the ADC input specification. The final choice of three gain ranges, and their ratios, achieves the physics performance without over-specifying the requirements for the MGPA design. The linearity and pulse shape matching requirements are demanding. The pulse shape matching is defined as the ratio of a sample taken on the output pulse 25 ns before the peak to the peak sample itself. The CR-RC pulse shaping time constant is specified to be 40 ns which, when combined with the 10ns $PbWO_4$ average scintillation decay time, results in an effective output peaking time close to 50 ns.

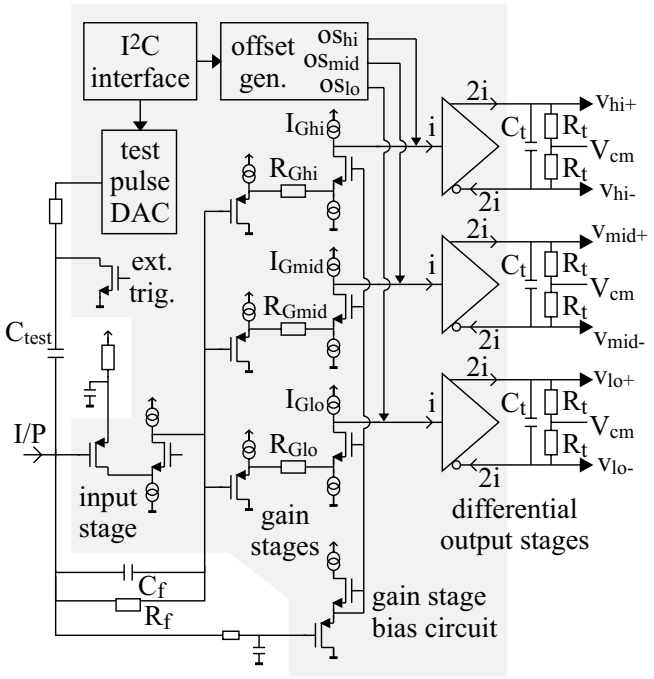

Fig. 2. MGPA architecture overview. Components inside the shaded area are on-chip, those outside are external

A. Electronic Architecture

A simplified schematic view of the MGPA architecture is shown in Fig. 2. The input stage is a folded-cascode configuration with external feedback components C_f and R_f chosen to match the barrel (39pF//1kΩ) or end-cap (8.2pF//4.7kΩ) full-scale signal sizes. The C_fR_f decay time constant implements the differentiation component of the overall 40 ns pulse shaping time. This allows the gain to be maximized, helping to minimize noise contributions from subsequent stages, while the short decay time avoids pile-up.

The output of the input stage is buffered by source followers to the three gain channels. Internal (on-chip) resistors R_{Ghi}, R_{Gmid} and R_{Glo} set the gains and feed common-gate stages which deliver currents to three differential output stages. The source followers introduce a DC level shift between the first stage output and the gain resistors. The gain stage bias circuit derives the gate voltages of the common-gate stages from the first stage input voltage, allowing the DC voltage across the gain resistors to be closely matched, thus avoiding any significant DC current flow.

The three differential output stages are all identical single-ended input to differential output current circuits. The output stage resistors R_t (200Ω) provide current to voltage conversion and are terminated to V_{cm}, the 1.25 Volt common mode voltage. Capacitors C_t (100 pF) are chosen to provide the 40ns RC integrating time constant of the pulse shaping. A significant advantage of realizing the low pass filtering in this way, at the end of the signal processing chain, is that it acts on all noise sources within the chip.

An I^2C interface is used to programme the individual offset (pedestal) levels at the outputs by setting the magnitudes of offset currents applied at the differential stage inputs, via the offset generator block. This is needed because without it the differential output stages will naturally bias up at the mid-point of their dynamic ranges where the magnitudes of the individual output currents are zero.

A test pulse facility is included on the chip where charge can be injected into the MGPA input following an external trigger. The magnitude of the charge is determined by a simple DAC circuit, implemented by a resistor chain between the power supply rails, with switches to allow different DC levels to be selected under I^2C control.

B. Noise Sources

The dominant noise source in the input stage of the MGPA is the feedback resistor R_f, which contributes 4900 and 2700 electrons for the barrel (1.2kΩ) and end-cap (4.7kΩ) values respectively. The input FET dimensions are 30,000/0.36 (width/length ratio in μm), chosen to achieve close to the one third optimum capacitance matching condition for the external input load capacitance in the barrel case (200pF), which results in a transconductance of ~ 0.3 A/V, and a gate capacitance of ~ 60pF. The simulated channel noise voltage v_{FET} of this transistor is 0.23 nV/√Hz, which gives a noise contribution of approximately 1800 and 660 electrons for the barrel (200pF) and end-cap (50pF) input capacitances, C_{IN}, respectively. The total input stage noise is 5220 electrons for the barrel and 2780 for the end-cap, with only a weak dependence on C_{IN}.

Because the gain of the input stage is limited to accommodate the full-scale signals, it is not possible to avoid noise contributions from the gain resistor and common-gate stages. The overall simulated noise for all three gain channels for both barrel and end-cap cases is given in table II. For the high and mid-gain ranges the gain resistors are relatively small (R_G=14 and 34Ω) and noise is within specification. For the low-gain range R_G becomes 240Ω, the gain stage noise

completely dominates, and the simulated noise is approximately three times specification, but higher noise can be tolerated for this range because it is used for larger signals where the electronic noise contribution to the overall ECAL energy resolution is negligible.

TABLE II
SPICE SIMULATED NOISE PERFORMANCE [RMS ELECTRONS] FOR BOTH BARREL AND END-CAP INPUT CAPACITANCES (C_{IN})

gain range	barrel (C_f/R_f=33pF/1k2) C_{IN} = 200 pF	end-cap (C_f/R_f=8.2pF/4k7) C_{IN} = 50 pF
high	6,200	2,700
mid	8,200	3,070
low	35,400	9,800

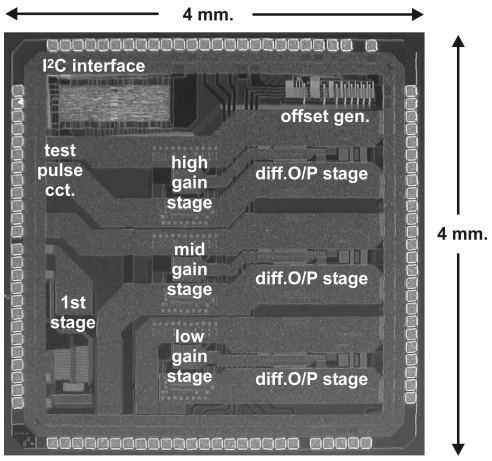

Fig. 3. Photograph of an MGPA die with internal circuitry locations indicated.

C. MGPA layout

The layout of the MGPA chip can be seen in the photograph of a die in Fig. 3 where the main circuit blocks are indicated. Care was taken to avoid inter-channel cross-talk problems, when the higher gain ranges saturate, by physically separating channels as much as possible, providing each with individual multiple power pads. The die size is approximately 4 mm. x 4 mm. and the chip is packaged in a 14 mm. x 14 mm. Thin Quad Flat Pack (TQFP) 100 pin package (Fig. 4).

III. MEASURED PERFORMANCE

The MGPA chip draws approximately 240 mA from a single 2.5 Volt rail. The input, gain and differential output stages consume approximately 150, 300 and 150 mW respectively. A number of peripheral passive components are required for correct operation [6], to provide decoupling and set operating currents, as well as those required for the input stage feedback network and output stage termination. A careful circuit layout is required to minimize differences in parasitic capacitance at the differential outputs to obtain the pulse shape matching performance. The VFE board layout in Fig. 4 achieves this, where some of the MGPA peripheral components can be seen (others are mounted on the back surface of the board), as well as the multi-channel ADC chip to the right of the MGPA.

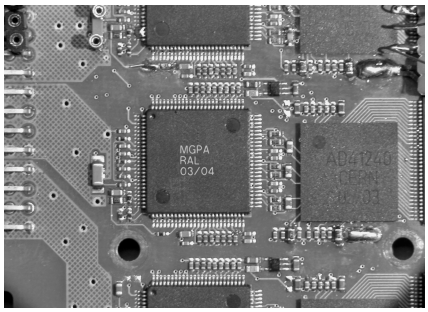

Fig. 4. Photograph of an MGPA chip on the 5-channel ECAL VFE board. Two neighbouring channels can be seen above and below. The multi-channel 12-bit ADC chip can be seen to the right of the MGPA.

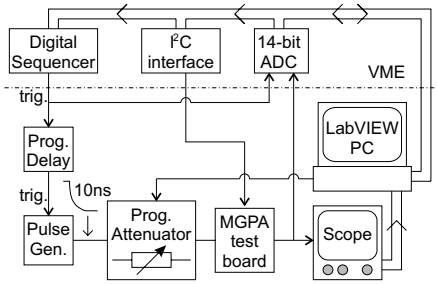

Fig. 5. Schematic diagram of MGPA test set-up

Fig. 5 shows a diagram of the automated set-up used to characterise the MGPA performance. A VME crate contains a programmable digital sequencer and a 14-bit ADC (SIS model 3301). The sequencer provides a 40 MHz clock, a trigger to the ADC, and a trigger to a pulse generator after a programmable delay (0 – 250 ns in 1 ns steps). The programmable delay allows the pulse shape to be re-constructed, by sweeping the charge injection time relative to the ADC trigger. The pulse generator produces a test pulse with 10 ns rise-time to simulate the $PbWO_4$ scintillation decay time. This is passed through a programmable RF attenuator and used to inject charge into the MGPA input via a calibrated capacitor. Many of the tests have been performed using a test board where the MGPA can be mounted in a socket, to allow comparisons between a significant number of chips. To obtain best performance, however, a compact layout is required, such as that in Fig. 4, and some of the tests have also been performed using the VFE card itself as the MGPA test board.

A. Pulse shapes

Fig. 6 shows the measured output pulse shapes in true differential form, where the negative output has been

subtracted from the positive and the baseline offset has also been subtracted. Pulse shapes are shown for 30 signal steps in the range 0 to 60 pC, the full-scale signal range for the barrel case. The steps are not linearly spaced because of the logarithmic nature of the attenuator. The high and mid-gain channels saturate while the low gain channel stays within the linear range. The average gain ratios for 10 chips from each iteration are measured to be 1:5.6:11.0 and 1:5.4:10.8 for versions 1 and 2 respectively, which compare well to the 1:6:12 specification (table I). There are no signs of distortion in the lower gain channels as the higher ranges saturate.

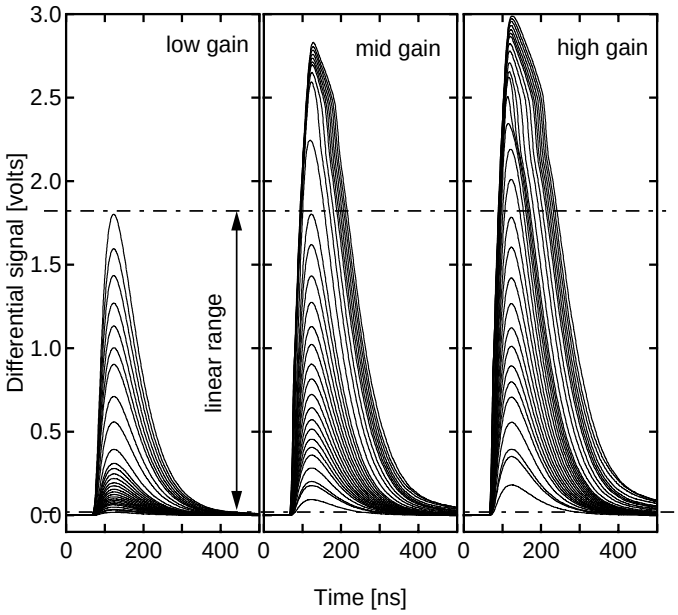

Fig. 6. Differential (V_+ - V.) output pulse shapes for all three gain channels. The same range of signal sizes, 0 – 60 pC, is displayed for each gain.

B. Nonlinearity

To measure nonlinearity experimentally a set of pulse shapes are acquired for a range of input signal amplitudes spanning the full range of the particular gain channel. If *pk.ht.(A)* is the measured peak height of the pulse shape acquired for input signal amplitude A, and *fit(A)* is the corresponding value from the linear fit to the peak height data set, then the nonlinearity for each value of A is given by:

$$nonlinearity[\%\, fullscale] = 100.\left\{\frac{pk.ht.(A) - fit(A)}{A_{fullscale}}\right\} \qquad (2)$$

where $A_{fullscale}$ is the input signal amplitude that would generate a full-scale output.

The nonlinearity has been measured using the test set-up in Fig. 5. The 14-bit VME based ADC nonlinearity contribution was negligible. Fig. 7 shows the measured nonlinearity to be close to specification for all three gain channels for 10 chips from both of the MGPA iterations, demonstrating good matching between chips and iterations.

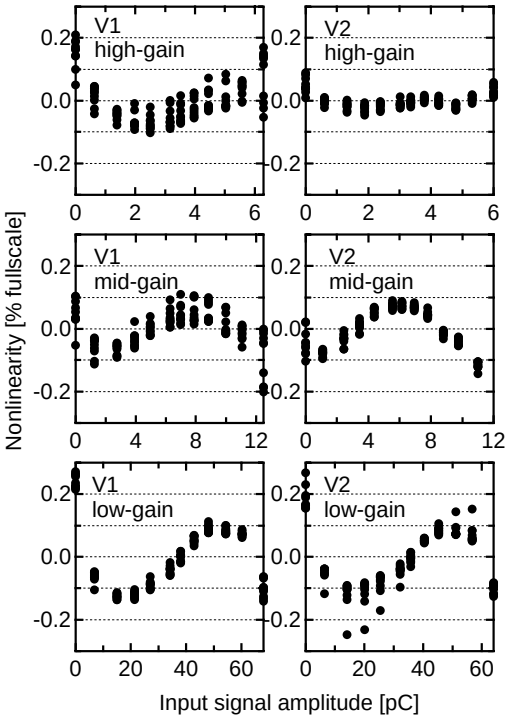

Fig. 7. Nonlinearity measurements for all three gain ranges for 10 chips from both (V1 and V2) MGPA iterations.

C. Pulse Shape Matching

Fig. 8 shows the result if all pulse shapes in the full-scale range of each channel are superimposed, normalized to the maximum pulse height in each case. The results shown are for a chip mounted on a VFE card. The pulse shape matching factor is defined as the ratio of the voltage 25 ns before the peak (Vpk-25) to the peak voltage Vpk. Pulse shape matching (PSM) is then given by,

$$PSM[\%] = 100.\left\{\frac{PSMF - Ave.PSMF}{Ave.PSMF}\right\} \qquad (3)$$

where *Ave.PSMF* is the average over all pulse shapes for all three gain ranges. Fig. 9 shows the PSM calculated for the pulse shapes in Fig. 8 is well within the ±1%, specification.

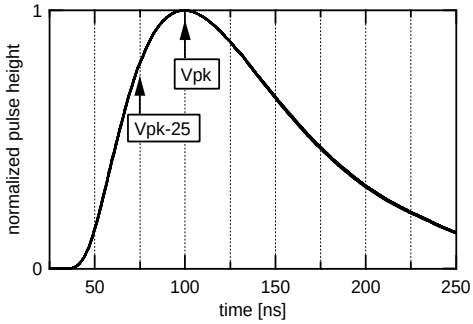

Fig. 8. Thirty-three normalized output pulse shapes superimposed, 11 spanning the full range for each gain channel.

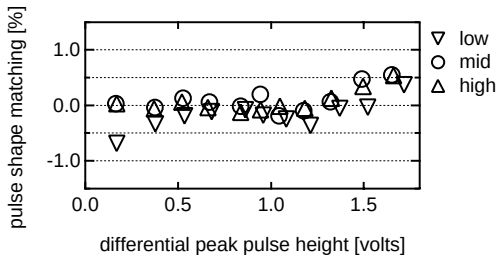

Fig. 9. Pulse shape matching for the pulse shapes in Fig. 8.

D. Noise

Fig. 10 shows the measured MGPA noise dependence on added capacitance for the high and mid-gain channels for both barrel and end-cap input stage gains. The noise was measured using a wide bandwidth (10 kHz – 500 MHz) true rms milli-voltmeter. The expected weak noise dependence on input capacitance is evident. Table III shows the measured noise for all three gain channels at the specified input capacitance for the barrel and end-cap cases. The values for the high and mid-gain channels are similar and within specification, the values for the low gain channel being much larger where the noise from the gain stage dominates as expected. The measured results in table III are quite close to the values predicted by simulation in table II.

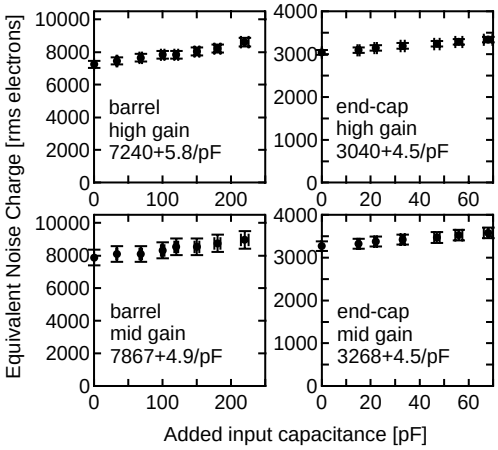

Fig. 10. High and mid-gain noise dependence on added input capacitance for barrel and end-cap cases. Noise intercepts and slopes are indicated for each case. Error bars represent estimated experimental errors.

TABLE III
MEASURED NOISE PERFORMANCE [RMS ELECTRONS] FOR BOTH BARREL AND ENDCAP (ADDED CAPACITANCE C_{ADD}=200PF AND 50PF RESPECITVELY).

gain range	barrel noise for C_{add} = 200 pF	end-cap noise for C_{add} = 50 pF
high	8390 ± 250	3263 ± 66
mid	8850 ± 265	3496 ± 122
low	27340 ± 3280	8230 ± 905

E. Radiation Hardness

The radiation hardness of the 0.25μm process is well known [4]. Nevertheless, it was felt necessary to confirm expectations so one chip has been irradiated with 10 keV X-rays to a dose of 50 kGy (±10%), which is twice the worst case dose expected in CMS, at a dose-rate of ~ 10 kGy/hour. The only measurable difference in performance after irradiation was a 3% reduction in gain for all three channels. It is common to follow a high dose-rate irradiation by an annealing step, but since the damage effects were so small this was not considered necessary.

IV. CONCLUSIONS

The MGPA, a three gain channel preamplifier chip, has been developed in 0.25μm CMOS to match the readout requirements of the CMS Electromagnetic calorimeter. By a suitable choice of external feedback components for the input stage, both barrel and end-cap regions of the detector can be read out using the same chip. The chip has been finalized in two iterations, only minor changes being required for the second version.

Details of the design have been described and the measured performance presented. The critical performance specifications of linearity, pulse shape matching and noise have all been met, and there is no significant performance degradation after irradiation to 50 kGy.

V. ACKNOWLEDGEMENTS

We would like to thank the technical support group at Imperial College, and the UK Particle Physics and Astronomy Research Council for supporting this work. Thanks also to Lubo Djambazov and Marc Dejardin at CERN for the VFE card.

VI. REFERENCES

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